PRELIMINARY

51C259H
HIGH PERFORMANCE STATIC COLUMN 64K × 4 CHMOS DYNAMIC RAM

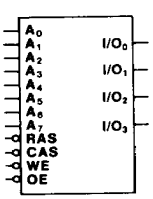
	51C259H-10†	51C259H-12	51C259H-15	51C259H-20
Maximum Access Time (ns)	100	120	150	200
Maximum Column Address Access Time (ns)	40	55	65	85

- **Static Column Mode Operation**
  - **Continuous data rate over 20 MHz**
  - **Random access from address within row**
- **Low Input/Output Capacitance**
- **Low Operating Current — 50mA (max.)**
- **Fast "Usable Speed"**
  - **t_{CAC} = 25 ns**
  - **t_{OAC} = 25 ns**
- **Fully TTL Compatible**
- **High Reliability Plastic — 18 Pin DIP, 22 Pin PLCC**

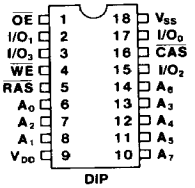
The Intel 51C259H is a high speed 65,536 × 4 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C259H offers features not provided by an NMOS dynamic RAM: Static Column Mode for high data bandwidth and fast usable speed. All inputs and outputs are TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

Static Column Mode operation allows random or sequential access of all 256 bits within a row simply by changing the column address. Because column address access time is as fast as 40 ns, a continuous data rate of over 20 million 4 bit nibbles per second can be achieved. The 51C259H offers high performance while relaxing many critical system timing requirements for fast usable speed. These features make the 51C259H ideally suited for graphics, digital signal processing, and high performance systems.

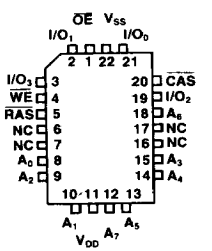
LOGIC SYMBOL



PIN CONFIGURATION



DIP



PLCC

PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_7	ADDRESS INPUTS
I/O_0-I/O_3	DATA IN/DATA OUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

† Available 1986

JUNE 1985
Order Number: 280033-003

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature
Under Bias . . . . . −10°C to +80°C
Storage Temperature . . Plastic −55°C to +125°C
Voltage on Any Pin except Input/Output (I/O)
Relative to V_{SS} . . . . . −1.0V to 7.5V
Voltage on I/O Relative to V_{SS} . . −1.0V to V_{DD} + 1V
Data Out Current . . . . . 50 mA
Power Dissipation 1.0W

†COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1]

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C259H			Unit	Test Conditions	Notes
		Min.	Typ.[2]	Max.			
I_{DD1}	V_{DD} Supply Current, Operating			80	mA	$t_{RC} = t_{RC(min)}$, for -10 specification	3, 4
				75	mA	$t_{RC} = t_{RC(min)}$, for -12 specification	
			49	60	mA	$t_{RC} = t_{RC(min)}$, for -15 specification	
			40	50	mA	$t_{RC} = t_{RC(min)}$, for -20 specification	
I_{DD2}	V_{DD} Supply Current, TTL Standby		1	4	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, all other inputs and outputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, RAS-Only Refresh			80	mA	$t_{RC} = t_{RC(min)}$, for -10 specification	4
				75	mA	$t_{RC} = t_{RC(min)}$, for -12 specification	
			45	60	mA	$t_{RC} = t_{RC(min)}$, for -15 specification	
			36	50	mA	$t_{RC} = t_{RC(min)}$, for -20 specification	
I_{DD4}	V_{DD} Supply Current, Static Column Mode			80	mA	Minimum Cycle for -10 specification	3,4
				75	mA	Minimum Cycle for -12 specification	
			23	60	mA	Minimum Cycle for -15 specification	
			21	50	mA	Minimum Cycle for -20 specification	
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		2	6	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ and $\overline{OE}$ at V_{IL}, all other inputs and outputs ≥ V_{SS}	3
$\lvert I_{LI} \rvert$	Input Load Current (any pin)			10	μA	$V_{IN} = V_{SS}$ to V_{DD}	
$\lvert I_{LI/O} \rvert$	I/O Leakage Current, High Impedance State			10	μA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, $D_{OUT} = V_{SS}$ to V_{DD}	
V_{IL}	Input Low Voltage (all inputs)	−0.3		0.8	V		5
V_{IH}	Input High Voltage (all inputs)	2.4		V_{DD} + 1	V		5
V_{OL}	Output Low Voltage (all outputs)			0.4	V	I_{OL} = 4.2 mA	6
V_{OH}	Output High Voltage (all outputs)	2.4			V	I_{OH} = −5 mA	6

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are at T_A = 25°C and V_{DD} = +5V.
3. I_{DD} is dependent upon output loading when the device output is selected. Specified $I_{DD(max)}$ is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions. Specified $I_{DD(max)}$ is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Static Column Mode.
5. Specified $V_{IL(min)}$ is steady state operation. During transitions, V_{IL} may undershoot to −1.0 V for periods not to exceed 20 ns. All A.C. parameters are measured with $V_{IL(min)} \geq V_{SS}$ and $V_{IH(max)} \leq V_{DD}$.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured as noted in the A.C. Characteristics section.

CAPACITANCE†

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address	4	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	3	5	pF
$C_{I/O}$	Data In/Out	4	6	pF

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable Hewlett Packard capacitance meter.

A.C. CHARACTERISTICS[1,2,3]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

No.	Symbol	Parameter	51C259H-10		51C259H-12		51C259H-15		51C259H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	150	75000	200	75000	ns	
2	t_{RC}	Random Read or Write Cycle Time	170		200		245		315		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	60		70		85		105		ns	
4	t_{CSH}*	$\overline{CAS}$ Hold Time	100		120		150		200		ns	
5	t_{CAS}*	$\overline{CAS}$ Pulse Width	25		30		30		35		ns	
6	t_{WRP}	$\overline{Write\ Enable}$ To $\overline{RAS}$ Precharge Time	10		10		10		10		ns	
7	t_{RWH}	$\overline{RAS}$ To $\overline{Write\ Enable}$ Hold Time	15		15		20		25		ns	
8	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RAH}	Row Address Hold Time	20		20		20		25		ns	
10	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ To Output High Impedance		25		30		30		30	ns	4,5
11	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ To Output Low Impedance	0		0		0		0		ns	4,5
	t_{REF}	Time Between Refresh		4		4		4		4	ms	
	t_T	Transition Time (Rise and Fall)	1	25	1	25	1	25	1	25	ns	6

NOTES:
* This parameter not applicable if operated with $\overline{CAS}$ grounded.
1. All voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).
3. A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with $V_{OL} = 0.8V$ at $I_{OL} - 2.2$ mA, $V_{OH} = 2.4V$ at $I_{OH} = -2.0$ mA with a 50 pF load, $V_{IL(min)} \geq V_{SS}$ and $V_{IH(max)} \leq V_{DD}$.
4. Assumes three state test load (5 pF and a 380 ohm Thevenin equivalent).
5. At any given temperature and voltage combination, coincident deselection/selection is permissible for wired-OR devices.
6. t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

A.C. CHARACTERISTICS (Continued)
Read Cycle

No.	Symbol	Parameter	51C259H-10		51C259H-12		51C259H-15		51C259H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
12	t_{RAC}	Access Time From $\overline{RAS}$		100		120		150		200	ns	7
13	t_{CAC}	Access Time From $\overline{CAS}$		25		30		30		35	ns	
14	t_{OAC}	Access Time From $\overline{OE}$		25		25		25		30	ns	
15	t_{CAA}	Access Time From Column Address		40		55		65		85	ns	
16	$t_{RSH(R)}$*	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		10		10		ns	
17	t_{RCS}*	Read Command Setup Time	0		0		0		0		ns	
18	t_{CAR}	Column Address To $\overline{RAS}$ Setup Time	40		55		65		85		ns	
19	t_{ARR}	Column Address Hold Time From $\overline{RAS}$ (Read)	95		115		145		195		ns	
20	t_{RCH}*	Read Command Hold Time Ref. To $\overline{CAS}$	5		5		5		5		ns	
21	t_{RRH}	Read Command Hold Time Ref. To $\overline{RAS}$	10		10		10		10		ns	
22	t_{ARH}	Column Address Hold Time To $\overline{RAS}$	0		0		0		0		ns	
23	t_{RAD}	$\overline{RAS}$ To Column Address Delay Time	25	60	25	65	25	85	30	115	ns	8
24	t_{OHA}	Output Hold Time From Address Change	5		5		5		5		ns	
25	t_{OH}	Output Hold Time From $\overline{OE}$ or $\overline{CAS}$	0		0		0		0		ns	

Write Cycle

No.	Symbol	Parameter	51C259H-10		51C259H-12		51C259H-15		51C259H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
26	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	25		30		35		40		ns	
27	t_{WDR}	$\overline{RAS}$ To Write Command Lead Time	25	70	25	85	30	110	35	155	ns	
28	t_{RWL}	Write Command To $\overline{RAS}$ Lead Time	25		30		30		35		ns	
29	t_{CWL}*	Write Command To $\overline{CAS}$ Lead Time	25		30		30		35		ns	
30	t_{WP}	Write Command Pulse Width	10		10		10		15		ns	
31	t_{WCP}	Write Command Precharge Time	10		10		10		15		ns	
32	t_{WCS}*	Write Command Setup Time	0		0		0		0		ns	9
33	t_{WCH}*	Write Command Hold Time	20		25		30		35		ns	
34	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	50		60		70		80		ns	
35	t_{AWS}	Column Address To Write Command Setup Time	0		0		0		0		ns	
36	t_{AWH}	Column Address To Write Command Hold Time	20		25		25		30		ns	

NOTES:
* This parameter not applicable if operated with $\overline{CAS}$ grounded.
7. Assumes that $t_{RAD} \leq t_{RAD(max)}$. If $t_{RAD} > t_{RAD(max)}$, then t_{RAC} will increase by the amount that t_{RAD} exceeds $t_{RAD(max)}$.
8. t_{RAD} is specified for reference only.
9. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{OWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is a $\overline{CAS}$ controlled write cycle and the data out pin will remain in high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{OWD} \geq t_{OWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle.

A.C. CHARACTERISTICS (Continued)

Write Cycle (Continued)

No.	Symbol	Parameter	51C259H-10		51C259H-12		51C259H-15		51C259H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
37	t_{ARW}	Column Address Hold Time From $\overline{RAS}$ (Write)	50		60		60		70		ns	
38	t_{DS}	Data-In Setup Time	0		0		0		0		ns	
39	t_{DH}	Data-In Hold Time	20		25		25		30		ns	
40	t_{OWS}	$\overline{OE}$ Setup Time From End of Write	20		25		30		35		ns	
41	t_{COH}	$\overline{OE}$ Hold Time From $\overline{CAS}$	20		20		25		30		ns	

Read-Modify-Write Cycle[10]

No.	Symbol	Parameter	51C259H-10		51C259H-12		51C259H-15		51C259H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
42	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	230		270		315		395		ns	
43	t_{RRW}	$\overline{RAS}$ Pulse Width (RMW)	160	75000	190	75000	220	75000	280	75000	ns	
44	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	85		100		100		115		ns	
45	t_{AR}	Column Address Hold Time From $\overline{RAS}$ (RMW)	155		185		215		275		ns	
46	t_{RWD}	$\overline{RAS}$ To $\overline{WE}$ Delay	130		155		185		240		ns	11
47	t_{AWD}	Column Address To $\overline{WE}$ Delay	70		90		100		125		ns	11
48	t_{CWD}*	$\overline{CAS}$ To $\overline{WE}$ Delay	55		65		65		75		ns	11
49	t_{OWD}	$\overline{OE}$ To $\overline{WE}$ Delay	25		30		30		35		ns	11

Static Column Mode[12]

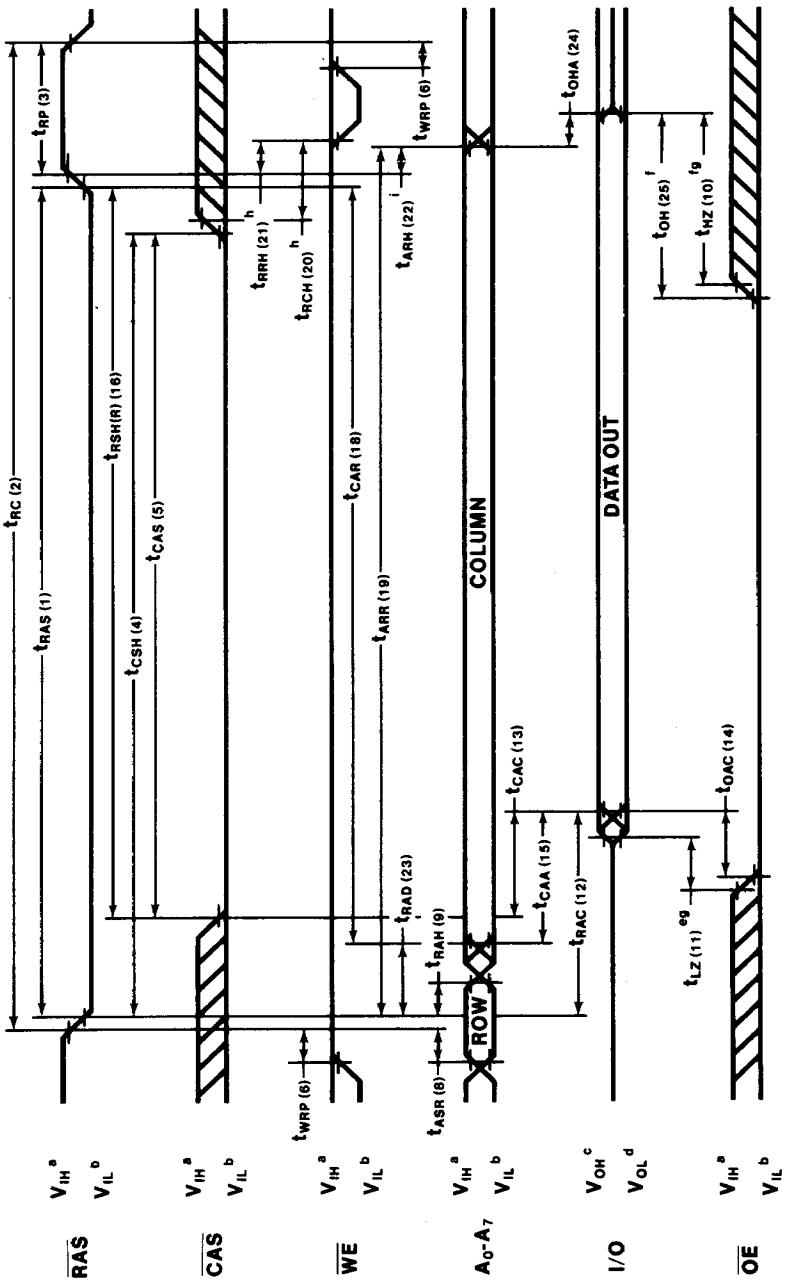
No.	Symbol	Parameter	51C259H-10		51C259H-12		51C259H-15		51C259H-20		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
50	t_{SWC}	Static Column Write Cycle Time	40		55		65		85		ns	
51	t_{WPA}	Write Precharge Access Time		25		30		30		35	ns	13
52	t_{WRA}	Write-Read Access Time		90		105		120		145	ns	13
53	t_{WOH}	Write To $\overline{OE}$ Hold Time	20		25		30		35		ns	
54	t_{SWH}	Delay From $\overline{RAS}$ To Second Write Command	115		135		170		225		ns	

NOTES:

* This parameter not applicable if operated with $\overline{CAS}$ grounded.

10. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
11. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{OWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is a $\overline{CAS}$ controlled write cycle and the data out pin will remain in high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{OWD} \geq t_{OWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle.
12. All previously specified A.C. characteristics are applicable.
13. Access time from a write command to a read command is determined by the longer of t_{CAA} or t_{WPA} or t_{WRA}.

WAVEFORMS
READ CYCLE



NOTE: a, b V_{IH}(min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c, d V_{OH}(min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}
e t_{LZ} is referenced to the later of $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ low transition.
f t_{HZ} and t_{OH} are referenced to the earlier of $\overline{CAS}$ or $\overline{OE}$ high transition.
g Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
h Either t_{RCH} or t_{RRH} must be satisfied
i If $t_{ARH} \geq t_{ARH}$(min), then data from the last address will be latched on D_{OUT} by a $\overline{RAS}$ high transition, until either a $\overline{CAS}$ or $\overline{OE}$ high transition releases the data.

C1608

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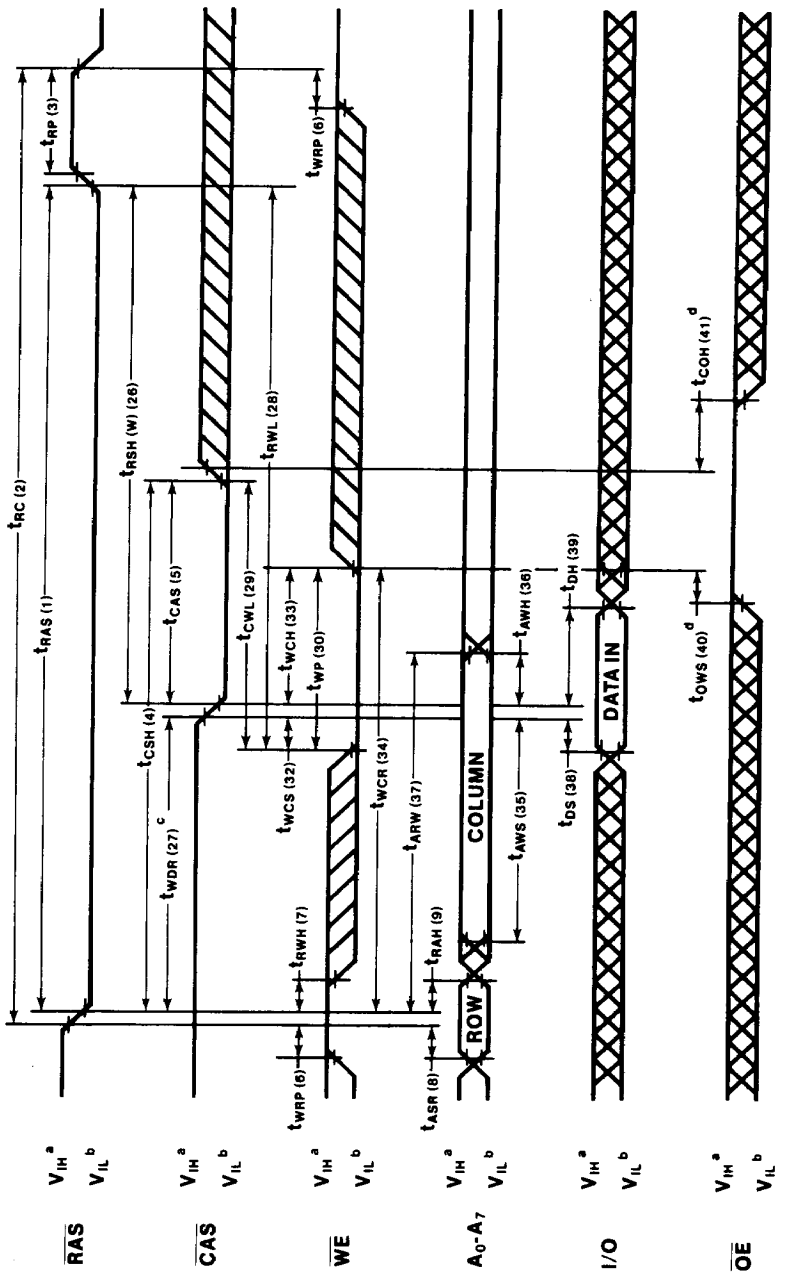
WAVEFORMS (Cont'd.)
WRITE CYCLE ($\overline{CAS}$ Controlled) [e]

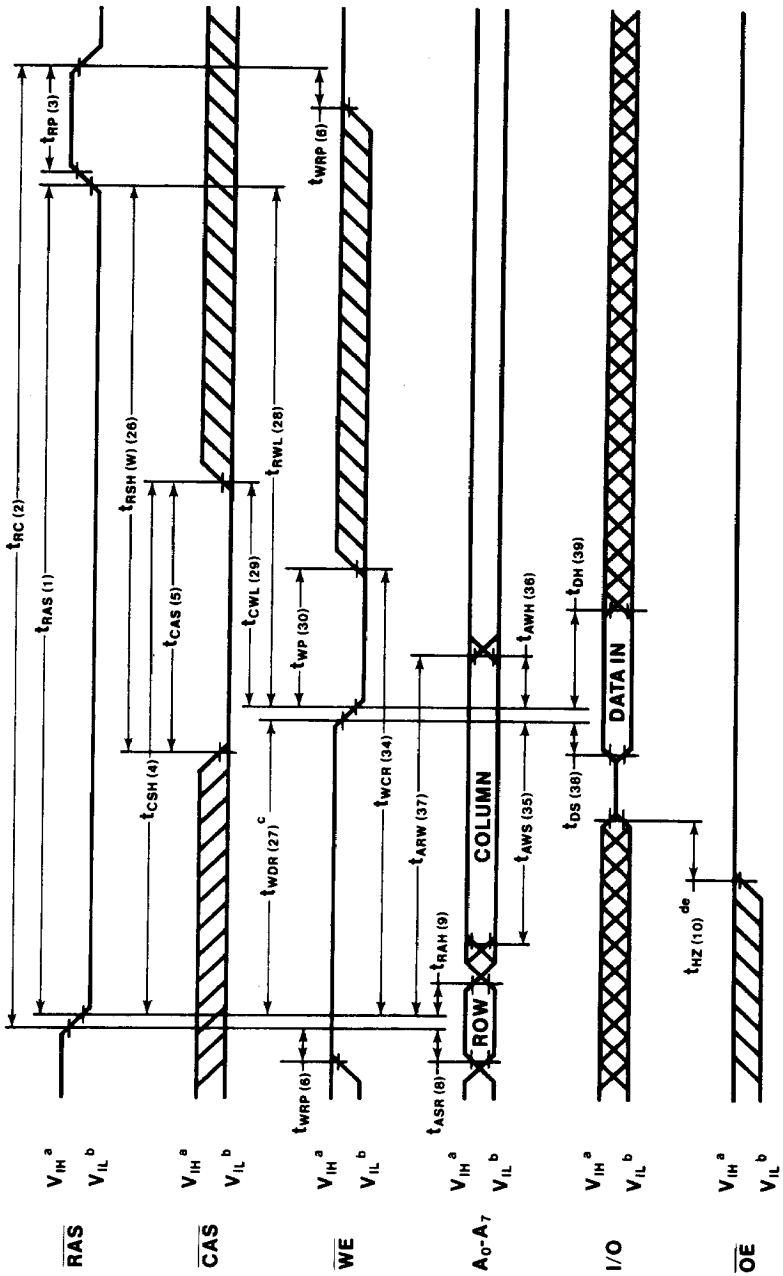


NOTE: a., b. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.
c. t_{WDR} is reference to the later of the $\overline{CAS}$ or $\overline{WE}$ low transition.
d. If the low transition of $\overline{WE}$ occurs before or simultaneously with the low transition of $\overline{CAS}$ and the high transition of $\overline{CAS}$ occurs before the high transition of $\overline{WE}$, then the outputs remain in a high impedence state (i.e. $\overline{OE}$ is a don't care).
e. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ is high prior to $\overline{RAS}$ low transition.

280033-003

C1610

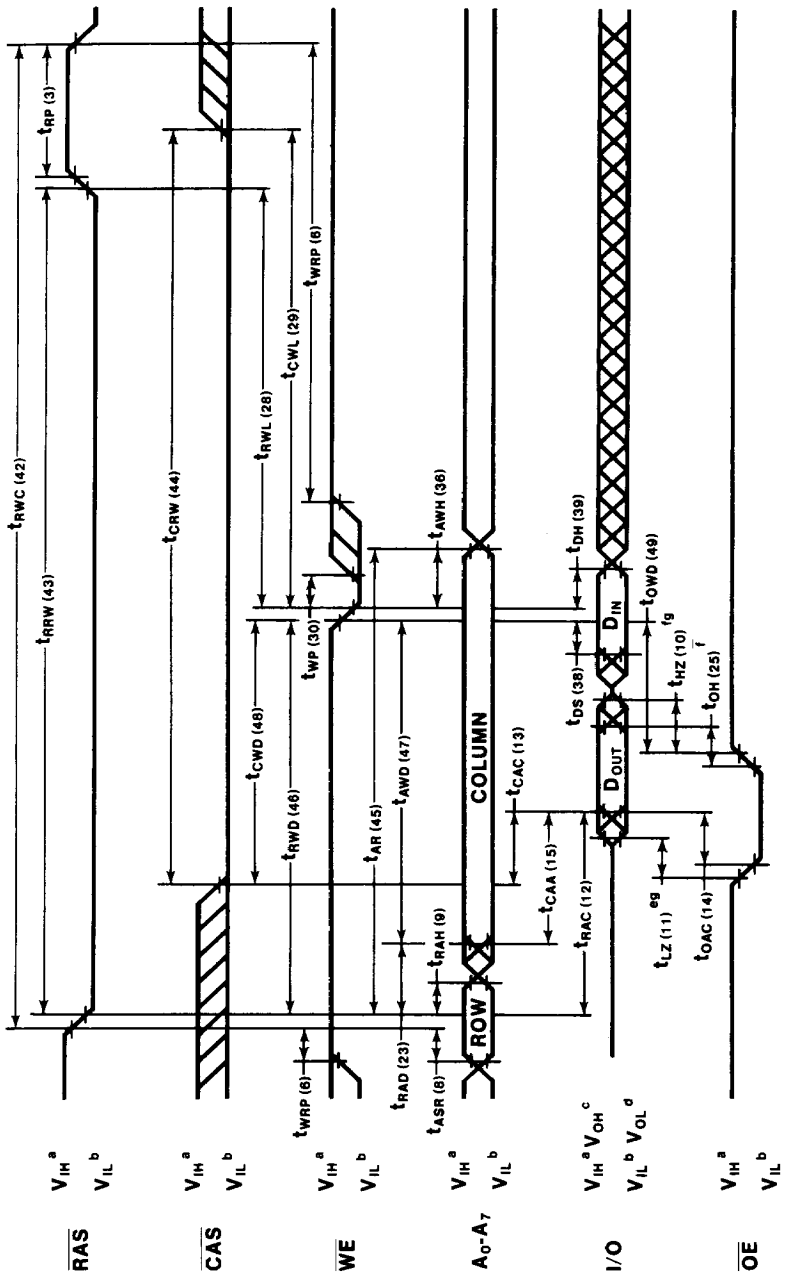
WAVEFORMS (Cont'd.)
WRITE CYCLE ($\overline{WE}$ Controlled) [f]



NOTE: a, b V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c t_{WDR} is reference to the later of the $\overline{CAS}$ or $\overline{WE}$ low transition.
d t_{HZ} is referenced to the earlier of the $\overline{CAS}$ or $\overline{OE}$ high transition or $\overline{WE}$ low transition.
e Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
f $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition.

280033-003

WAVEFORMS (Cont'd.)
READ/MODIFY/WRITE CYCLE

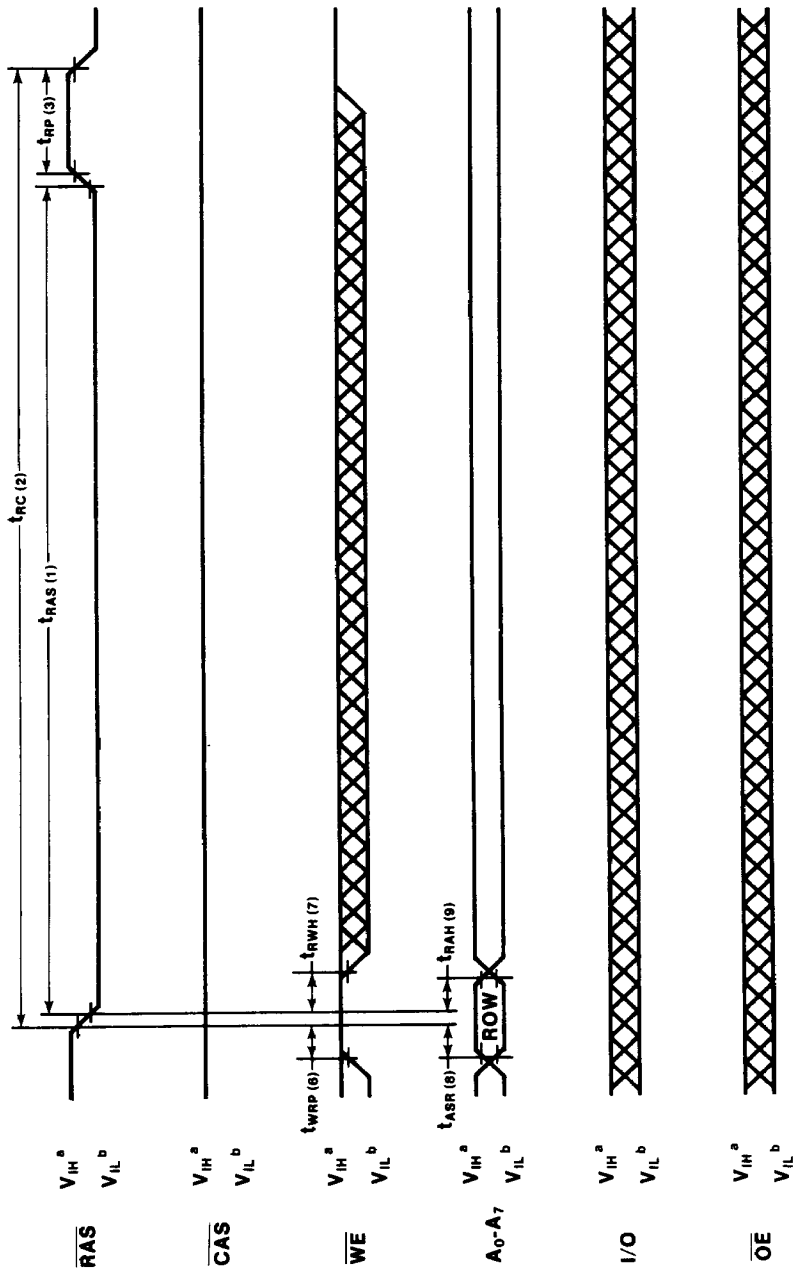


C1611

NOTE: a, b. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.
c, d. V_{OH}(min) and V_{OL}(max) are reference levels for measuring timing of D_{OUT}.
e. t_{LZ} is referenced to the later of RAS, CAS, and $\overline{OE}$ low transition.
f. t_{HZ} and t_{OH} are referenced to the earlier of the CAS or $\overline{OE}$ high transition.
g. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

280033-003

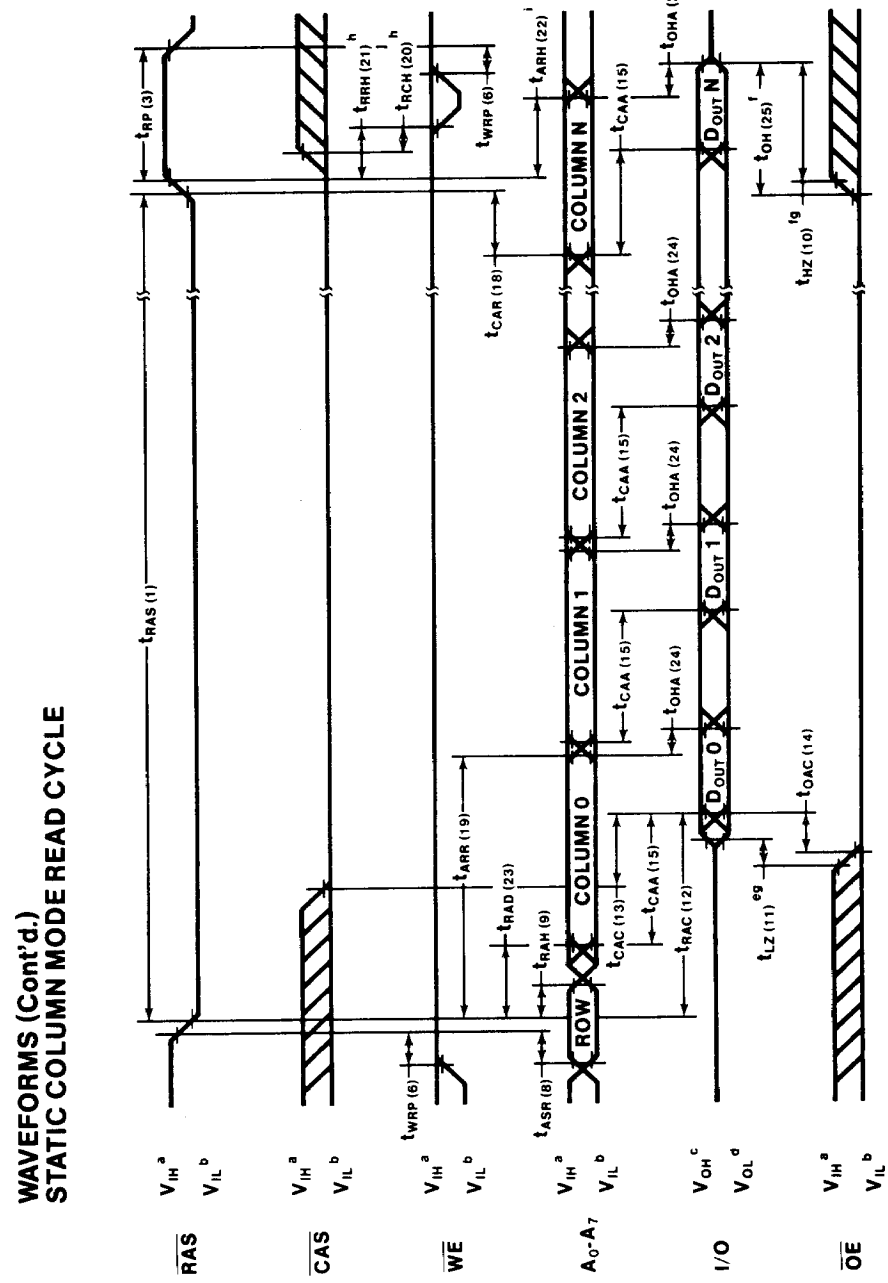
WAVEFORMS (Cont'd.)
RAS-ONLY REFRESH CYCLE



NOTE: a, b V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.

280033-003

WAVEFORMS (Cont'd.)
STATIC COLUMN MODE READ CYCLE

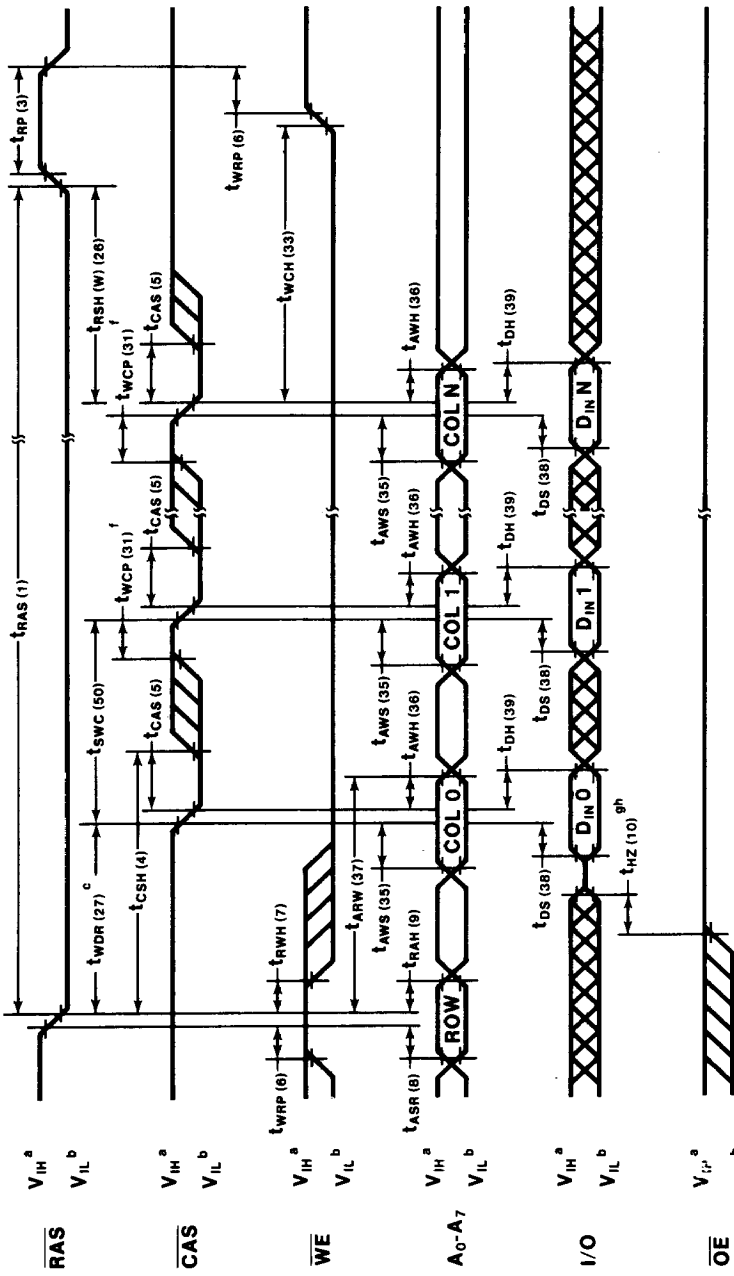


NOTE: a b V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals
c d V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}
e t_{LZ} is referenced to the later of $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ low transition
f t_{HZ} and t_{OH} are referenced to the earlier of the $\overline{CAS}$ or $\overline{OE}$ high transition
g Transition is measured +500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent)
h Either t_{RCH} or t_{RRH} must be satisfied.
i If $t_{ARH} > t_{ARH}$ (min), then data from the last address will be latched on D_{OUT} by a $\overline{RAS}$ high transition, until either a $\overline{CAS}$ or $\overline{OE}$ high transition releases the data

C1613

280033-003

WAVEFORMS (Cont'd.)
STATIC COLUMN MODE WRITE CYCLE ($\overline{CAS}$ Controlled) [g]

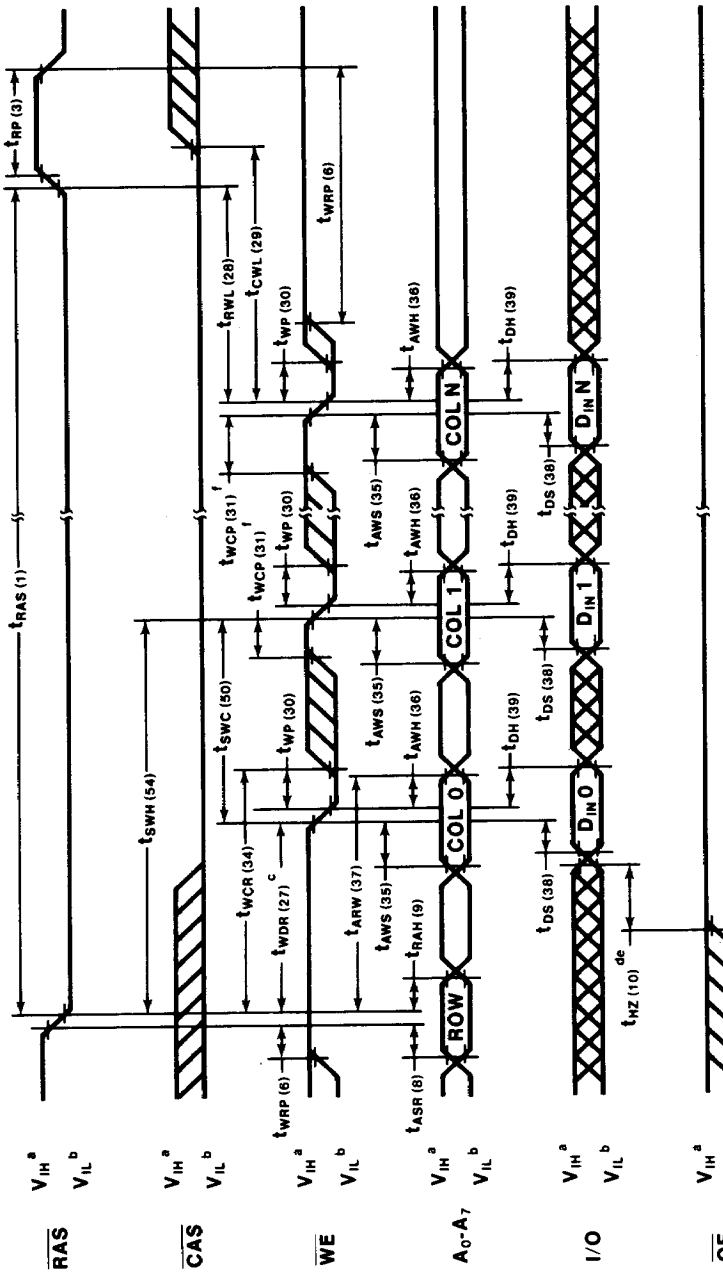


NOTE: a. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.
c. t_{WDR} is reference to the later of the $\overline{CAS}$ or $\overline{WE}$ low transition.
d. t_{HZ} is referenced to the earlier of the $\overline{CAS}$ or $\overline{OE}$ high transition or $\overline{WE}$ low transition.
e. Transition is measured +-500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
f. t_{WCP} is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.
g. $\overline{WE}$ is low prior to or simultaneously with a $\overline{CAS}$ low transition. $\overline{CAS}$ is high prior to a $\overline{RAS}$ low transition.

C1614

280033-003

WAVEFORMS (Cont'd.)
STATIC COLUMN MODE WRITE CYCLE ($\overline{WE}$ Controlled) [g]

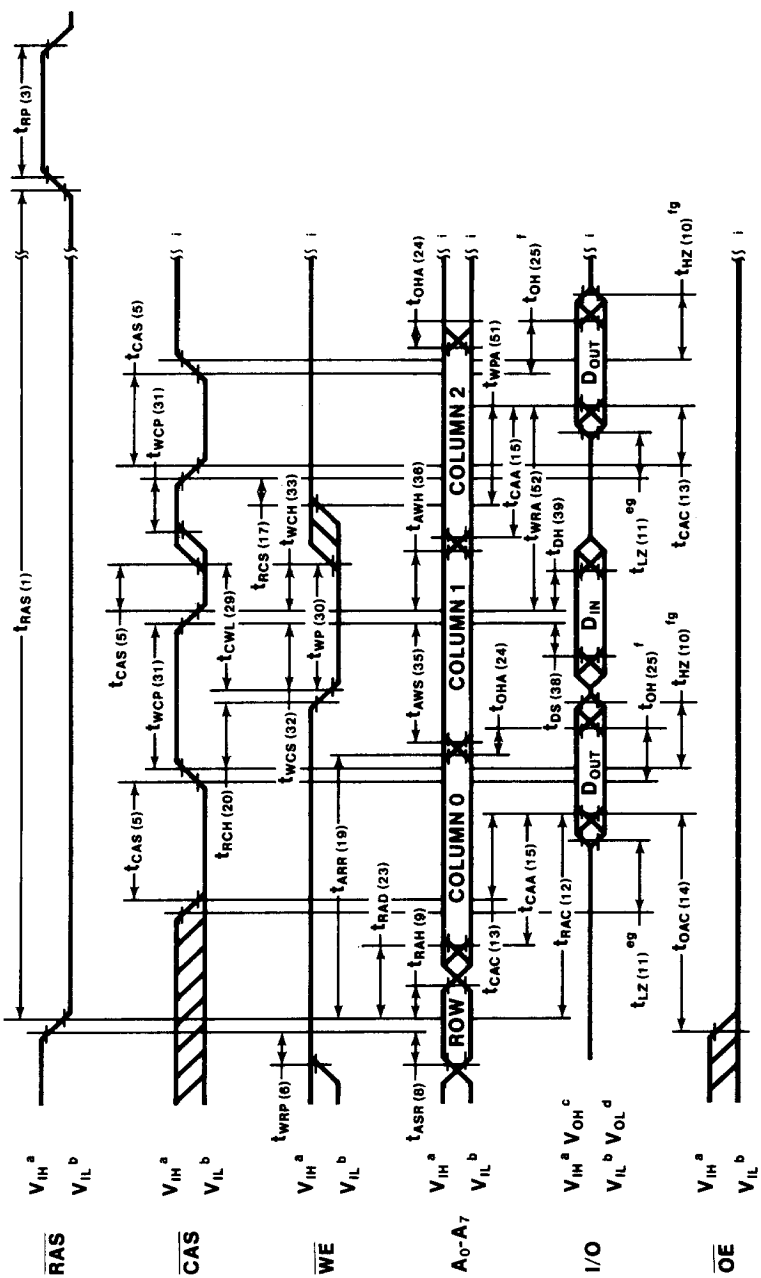


NOTE: a. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
b. t_{WDR} is reference to the later of the $\overline{CAS}$ or $\overline{WE}$ low transition.
c. t_{HZ} is referenced to the earlier of the $\overline{RAS}$ or $\overline{CAS}$ or $\overline{OE}$ high transition.
d. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
e. t_{WCP} is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.
f. $\overline{CAS}$ is low prior to a $\overline{WE}$ low transition.

C1615

280033-003

WAVEFORMS (Cont'd.)
STATIC COLUMN MODE READ/WRITE/READ . . . CYCLE ($\overline{CAS}$ Controlled) [h]

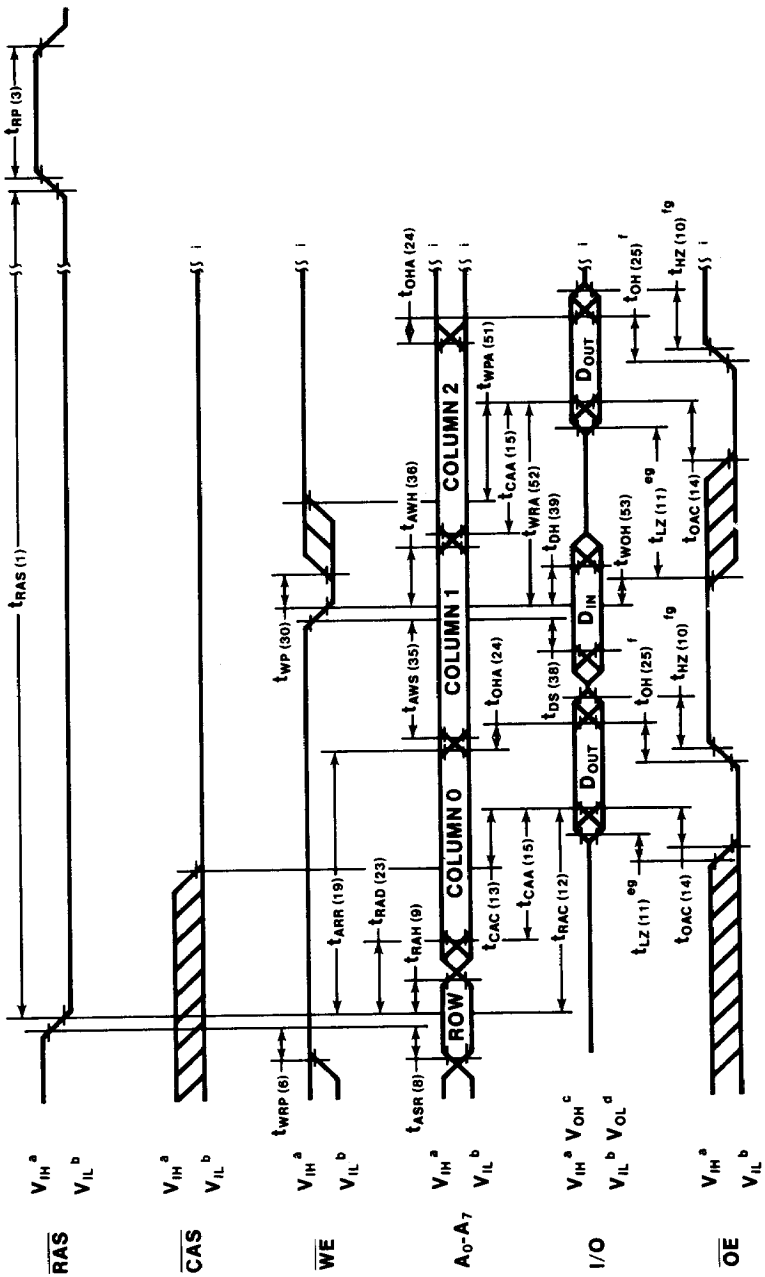


NOTE: a, b. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.
c, d. V_{OH}(min) and V_{OL}(max) are reference levels for measuring timing of D_{OUT}.
e. t_{LZ} is referenced to the later of $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ low transition.
f. t_{HZ} and t_{OH} are referenced to the earlier of $\overline{CAS}$ or $\overline{OE}$ high transition.
g. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
h. $\overline{WE}$ is low prior to or simultaneously with a $\overline{CAS}$ low transition.
i. The cycle can be terminated by either a read or a write operation followed by a $\overline{RAS}$ high transition. See pages 11 or 12 for timings.

C1616

280033-003

WAVEFORMS (Cont'd.)
STATIC COLUMN MODE READ/WRITE/READ . . . CYCLE ($\overline{WE}$ Controlled) [h]



NOTE: a, b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c, d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{LZ} is referenced to the later of $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ low transition if $\overline{RAS}$ and $\overline{CAS}$ and $\overline{OE}$ are low.
f. t_{HZ} and t_{OH} are referenced to the earlier of $\overline{CAS}$ or $\overline{OE}$ high transition.
g. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
h. $\overline{CAS}$ is low prior to a $\overline{WE}$ low transition.
i. The cycle can be terminated by either a read or a write operation followed by a $\overline{RAS}$ high transition. See pages 11 or 13 for timings.

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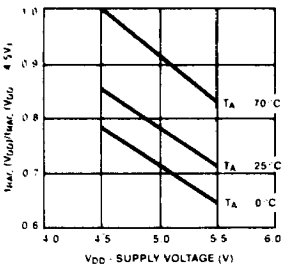
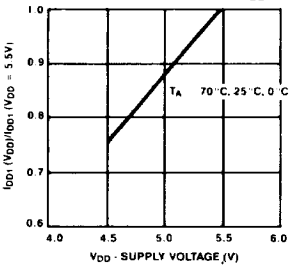
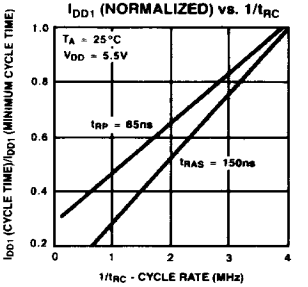
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) vs. V_{DD}



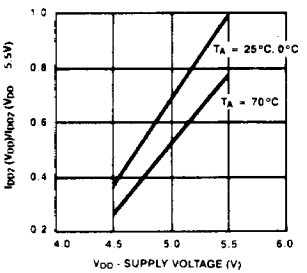
GRAPH 2
TYPICAL OPERATING CURRENT
I_{DD1} (NORMALIZED) vs. V_{DD}



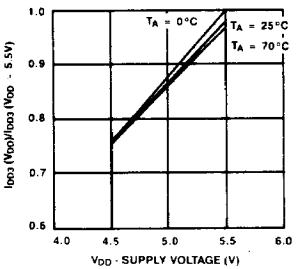
GRAPH 3
TYPICAL OPERATING CURRENT
I_{DD1} (NORMALIZED) vs. $1/t_{RC}$



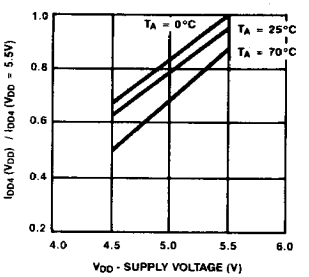
GRAPH 4
TYPICAL TTL STANDBY CURRENT
I_{DD2} (NORMALIZED) vs. V_{DD}



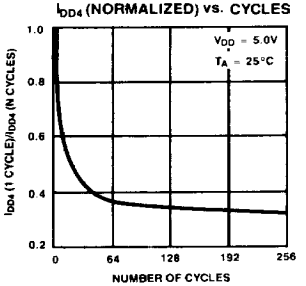
GRAPH 5
TYPICAL REFRESH CURRENT
I_{DD3} (NORMALIZED) vs. V_{DD}



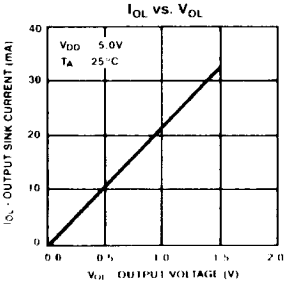
GRAPH 6
TYPICAL STATIC COLUMN MODE CURRENT
I_{DD4} (NORMALIZED) vs. V_{DD}



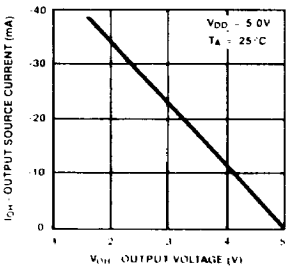
GRAPH 7
TYPICAL RIPPLEMODE CURRENT
I_{DD4} (NORMALIZED) vs. CYCLES



GRAPH 8
TYPICAL OUTPUT SINK CURRENT
I_{OL} vs. V_{OL}



GRAPH 9
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} vs. V_{OH}



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280033-003

FUNCTIONAL DESCRIPTION

The 51C259H is a CHMOS dynamic RAM optimized for high data bandwidth applications. The functionality is similar to a traditional dynamic RAM. The 51C259H reads and writes 4 bits of data at a time by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, is only latched during a write cycle by the later of either Column Address Strobe ($\overline{CAS}$) or Write Enable $\overline{WE}$. During the read cycle, the column address is not latched and continuously flows through the internal input latches. Access time is primarily dependent upon a valid column address. $\overline{CAS}$ acts as a chip select signal and can remain low during the entire memory operation.

Memory Cycle

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{ARR}. $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation. Data out is controlled by the Out Enable ($\overline{OE}$) and $\overline{CAS}$ which is discussed in the Data Out Operation.

For applications where $\overline{CAS}$ is held low, the data out becomes valid when t_{RAC}, t_{CAA}, and t_{OAC} are all satisfied.

For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. Data out becomes valid only when t_{RAC}, t_{CAA}, t_{OAC}, and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{CAA}, t_{OAC}, and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{OAC}, and t_{CAC} are all satisfied.

Write Cycle

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation. The column address is latched in by the later of $\overline{WE}$ or $\overline{CAS}$. As in the read cycle, $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation. For applications where $\overline{CAS}$ is held low, the input data must be valid at or before the falling edge of $\overline{WE}$. For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The input data must be valid at or before the falling edge of $\overline{WE}$, or $\overline{CAS}$, whichever occurs last. Consequently, the write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the later of $\overline{WE}$ or $\overline{CAS}$ low transition. In a $\overline{CAS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ will maintain the I/O in the high impedance state; terminating with $\overline{WE}$ allows the output to go active, and the $\overline{OE}$ must be brought high to allow for inputs on the I/O.

The 51C259H incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write function has been initiated, the 51C259H internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only cycle will perform refresh.

Static Column Mode Operation

Static column mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Read, write, and read-write-read cycles can be performed during static column mode operation. The row address is internally retained by maintaining $\overline{RAS}$ active. Following the entry cycle into static column mode operation, the data is accessed simply by changing the column address. Because the column address buffer acts as a transparent or flow-through latch, access begins from a valid column address. Thus, the 51C259H operates like a static RAM for multiple accesses within the same row. $\overline{CAS}$ acts as a chip select.

Data Out Operation

The 51C259H Input/Output (I/O) is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables data to transfer into and from a selected row address. A $\overline{RAS}$ high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or a $\overline{CAS}$ low level enables the internal I/O data path. A $\overline{CAS}$ high transition or $\overline{CAS}$ high level disables the I/O data path and disables the output driver if the driver was enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path, nor on the output driver. An $\overline{OE}$ low transition or an $\overline{OE}$ low level enables the output driver when the I/O data path is enabled. An $\overline{OE}$ high transition or an $\overline{OE}$ high level disables the output driver, but does not disable the data latch when it has been enabled. A $\overline{WE}$ low level disables the output driver when a $\overline{CAS}$ low level occurs. If the $\overline{WE}$ low transition occurs after the $\overline{CAS}$ low transition such that the output driver is enabled prior to the $\overline{WE}$ low transition, it is necessary to use $\overline{OE}$ to disable the output driver prior to the $\overline{WE}$ low transition to allow data in set-up time (t_{DS}). A $\overline{WE}$ high transition passes control of the ouput drive to $\overline{OE}$.

Power On

An initial pause of 100 μS is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of the cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).

The V_{DD} current (I_{DD}) requirement of the 51C259H during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS} = V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.