OP-07 Series Instrumentation Grade Operational Amplifier

Features

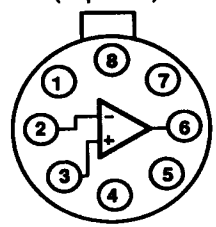
- Low noise 0.1 Hz to 10 Hz — 0.35 μV_{p-p}
- Ultra-low V_{os} — 10 μV
- Ultra-low V_{os} drift — 0.2 $\mu V/^{\circ}C$
- Fits 725, 108A, 741, and AD510 sockets
- Long term stability — 0.2 μV/Month
- Low input bias current — ±1 nA
- High CMRR — 126 dB
- Wide input voltage range — ±14V
- Wide supply voltage range — ±3V to ±22V

Description

The OP-07 amplifier series is designed for precision low level signal conditioning where ultra low V_{os} and TCV_{os} are required along with very low bias currents. Internal compensation eliminates the need for external components. Novel circuit design and tight process controls are used to obtain very low values of V_{os}. V_{os} is further reduced by a computer controlled digital nulling techniques at test. Low frequency noise is minimized. Internal biasing techniques reduce external bias and offset currents to values in the order of ±1 nA over the military temperature range. OP-07s are direct replacements for the 108A, 714, 725 and 5507. They can replace chopper stabilized amplifiers in many applications.

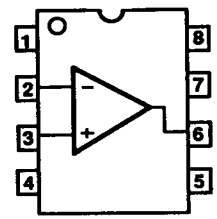
Connection Information

8-Lead TO-99 Metal Can
(Top View)



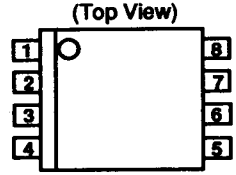
65-03205A

8-Lead Dual In-Line Package
(Top View)



65-03206A

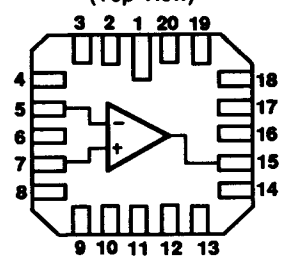
8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

Pin	Function
1	V_{os} Trim
2	-Input
3	+Input
4	$-V_s$
5	NC
6	Output
7	$+V_s$
8	V_{os} Trim

20-Pad LCC
(Top View)



65-02657A

Pin	Function
2	V_{os} Trim
5	-Input
7	+Input
10	$-V_s$
15	Output
17	$+V_s$
20	V_{os} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
OP-07CT	T	0°C to +70°C
OP-07DT	T	0°C to +70°C
OP-07ET	T	0°C to +70°C
OP-07CD	D	0°C to +70°C
OP-07DD	D	0°C to +70°C
OP-07ED	D	0°C to +70°C
OP-07CN	N	0°C to +70°C
OP-07DN	N	0°C to +70°C
OP-07EN	N	0°C to +70°C
OP-07CM	M	0°C to +70°C
OP-07DM	M	0°C to +70°C
OP-07EM	M	0°C to +70°C
OP-07T	T	-55°C to +125°C
OP-07T/883B	T	-55°C to +125°C
OP-07AT	T	-55°C to +125°C
OP-07AT/883B	T	-55°C to +125°C
OP-07D	D	-55°C to +125°C
OP-07D/883B	D	-55°C to +125°C
OP-07AD	D	-55°C to +125°C
OP-07AD/883B	D	-55°C to +125°C
OP-07L	L	-55°C to +125°C
OP-07L/883B	L	-55°C to +125°C
OP-07AL	L	-55°C to +125°C
OP-07AL/883B	L	-55°C to +125°C

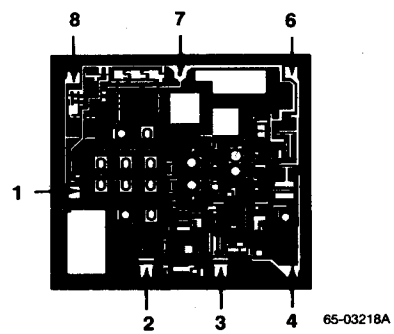
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
L = 20-pad leadless chip carrier
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
OP-07A ..... -55°C to +125°C
OP-07E/C/D ..... 0°C to +70°C
Lead Soldering Temperature
(SO-8; 10 sec) ..... +260°C
(DIP, LCC, TO-99; 60 sec) ..... +300°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



Die Size: 75 x 78 mils
Min . Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	20-Pad LCC	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Small Outline	8-Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	175°C	125°C	125°C
Max. P_D T_A <50°C	925 mW	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	37°C/W	45°C/W	50°C/W	–	–
Therm. Res. θ_{JA}	105°C/W	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	7.0 mW/°C	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			10	25		30	75	μV
Long Term Input Offset Voltage Stability[3,4]			0.2	1.0		0.2	1.0	μV/Mo
Input Offset Current			0.3	2.0		0.4	2.8	nA
Input Bias Current			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density[2]	f_O = 10Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	f_O = 100Hz		10	13		10	13	
	f_O = 1000Hz		9.6	11		9.6	11	
Input Noise Current[2]	0.1Hz to 10Hz		14	30		14	30	pA_{p-p}
Input Noise Current Density[2]	f_O = 10Hz		0.32	0.80		0.32	0.80	$\frac{pA}{\sqrt{Hz}}$
	f_O = 100Hz		0.14	0.23		0.14	0.23	
	f_O = 1000Hz		0.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[3]		30	80		20	60		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		110	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	110		100	110		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	300	500		200	500		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500k\Omega$, V_O = ±0.5V, V_S = ±3V	150	500		150	500		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±12	±12.8		
	$R_L \geq 1k\Omega$	±10.5	±12		±10.5	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		0.1	0.3		V/μS
Unity Gain Bandwidth	A_{VCL} = +1.0		0.8			0.8		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V		75	120		75	120	mW
	V_S = ±3V		4.0	6.0		4.0	6.0	
Offset Adjustment Range	R_P = 20kΩ		±4.0			±4.0		mV

Notes:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. OP-07A is tested fully warmed up.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.
4. Long Term Input Offset Voltage Stability refers to the average trend line of V_{os} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{os} during the first 30 operating days are typically 2.5 μV.

Electrical Characteristics (Continued)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	75		60	150		60	150	μV
Long Term Input Offset Voltage Stability[3,4]			0.3	1.5		0.4	2.0		0.5	3.0	$\mu V/Mo$
Input Offset Current			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current			±1.2	±4.0		±1.8	±7.0		±2.0	±12	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6		0.38	0.65		0.38	0.65	μV_{p-p}
Input Noise Voltage Density[2]	f_O = 10Hz		10.3	18		10.5	20		10.5	20	$\frac{nV}{\sqrt{Hz}}$
	f_O = 100Hz		10	13		10.2	13.5		10.2	13.5	
	f_O = 1000Hz		9.6	11		9.8	11.5		9.8	11.5	
Input Noise Current[2]	0.1Hz to 10Hz		14	30		15	35		15	35	pA_{p-p}
Input Noise Current Density[2]	f_O = 10Hz		0.32	0.8		0.35	0.9		0.35	0.9	$\frac{pA}{\sqrt{Hz}}$
	f_O = 100Hz		0.14	0.23		0.15	0.27		0.15	0.27	
	f_O = 1000Hz		0.12	0.17		0.13	0.18		0.13	0.18	
Input Resistance (Diff. Mode)[3]		15	50		8.0	33		7.0	31		MΩ
Input Resistance (Com. Mode)			160			120			120		GΩ
Input Voltage Range		±13	±14		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	94	107		90	104		90	104		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	200	500		120	400		120	400		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500\Omega$, V_O = ±0.5V, V_S = ±3.0V	150	500		100	400			400		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12	±13		±12	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±11.5	±12.8		±11.5	±12.8		
	$R_L \geq 1k\Omega$	±10.5	±12			±12					
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		0.1	0.3		0.1	0.3		$V/\mu S$
Unity Gain Bandwidth	A_{VCL} = +1.0		0.8			0.8			0.8		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60			60		Ω
Power Consumption	V_S = ±15V		75	120		80	150		80	150	mW
	V_S = ±3.0V		4.0	6.0		4.0	8.0		4.0	8.0	
Offset Adjustment Range	R_p =20kΩ		±4.0			±4.0			±4.0		mV

See footnotes on page 3.

Electrical Characteristics (Continued)

(V_S = ±15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			25	60		60	200	μV
Average Input Offset Voltage Drift Without External Trim[2]			0.2	0.6		0.3	1.3	μV/°C
With External Trim[3]	R_p = 20kΩ		0.2	0.6		0.3	1.3	
Input Offset Current			0.8	4.0		1.2	5.6	nA
Average Input Offset Current Drift[2]			5.0	25		8.0	50	pA/°C
Input Bias Current			±1.0	±4.0		±2.0	±6.0	nA
Average Input Bias Current Drift[2]			8.0	25		13	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		106	123		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	94	106		94	106		dB
Large Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	200	400		150	400		V/mV
Output Voltage Swing	R_L ≥ 2kΩ	±12	±12.6		±12	±12.6		V

Notes: 1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.

Electrical Characteristics (Continued)

(V_S = ±15V and 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			45	130		85	250		85	250	μV
Average Input Offset Voltage Drift Without External Trim[2]			0.3	1.3		0.5	1.8		0.7	2.5	μV/°C
With External Trim[3]	R_P = 20kΩ		0.3	1.3		0.4	1.6		0.7	2.5	
Input Offset Current			0.9	5.3		1.6	8.0		1.6	8.0	nA
Average Input Offset Current Drift[2]			8.0	35		12	50		12	50	pA/°C
Input Bias Current			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Average Input Bias Current Drift[2]			13	35		18	50		18	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	90	104		86	100		86	100		dB
Large Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	180	450		100	400		100	400		V/mV
Output Voltage Swing	R_L = 2kΩ	±12	±12.6		±11	±12.6		±11	±12.6		V

Notes: 1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.

Digital Nulling Technique

The digital nulling technique involves the zener diode nulling network of Figure 1. The zener diodes have relatively high breakdown voltages and never operate in the zener mode. The purpose of the zeners is to short out resistors R1, 2R1, 4R1, or 8R1 by forcing a high reverse current through the diode to metalize the junction. The input offset voltage can be adjusted by varying the collector resistor ratio. If the difference in the two collector resistors (R_C) is a small increment ΔR_C, V_{OS} can be written as:

$$V_{OS} = V_T \ln \frac{R_C + \Delta R_C}{R_C} = V_T \ln \left(1 + \frac{\Delta R_C}{R_C}\right)$$

for $\Delta R_C/R_C \ll 1.0$ $\ln(1+\Delta R_C/R_C) \approx \Delta R_C/R_C$, thus:

$$V_{OS} \approx V_T \frac{\Delta R_C}{R_C}$$

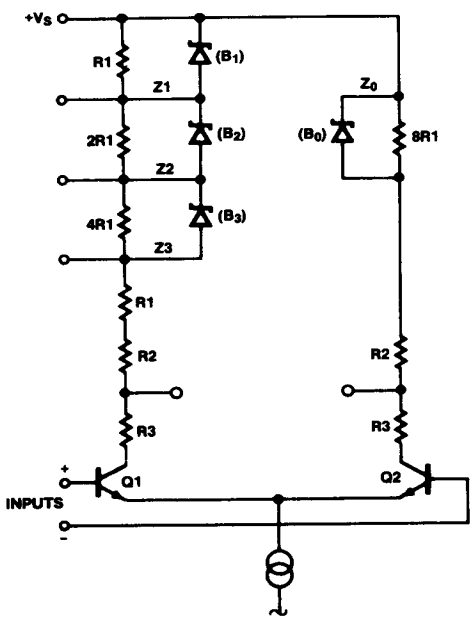
For Figure 1 $R2 + R3 \gg 8R1$, thus

$$V_{OS} \approx -V_T \frac{R_1}{8R1 + R2 + R3} (7 - B_3B_2B_1) \quad (B_0 = 1)$$

or:

$$V_{OS} \approx V_T \frac{R1}{R2 + R3} (1 + B_3B_2B_1) \quad (B_0 = 0)$$

where $B_3B_2B_1$ is a binary number which corresponds to the state of zener diodes Z1, Z2 and Z3 as per Figure 1.



65-00365A

Figure 1. Digital Nulling Network

$$\Delta V_{OS}(25°C) \approx \frac{-2.6mV\ (7 - B_3B_2B_1)R1}{8R1 + R2 + R3} \quad (B_0 = 1.0)$$

$B_n = 1.0$ for Z_n unshorted.

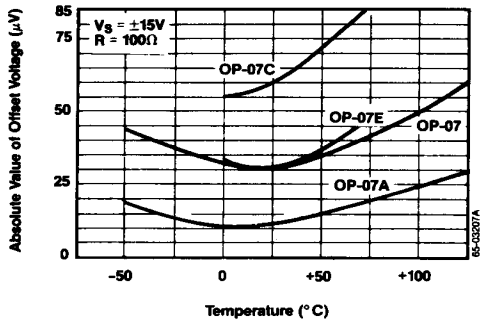
$B_n = 0$ for Z_n shorted.

$B_1B_2B_3$ = Binary number with values from 0 to 7.

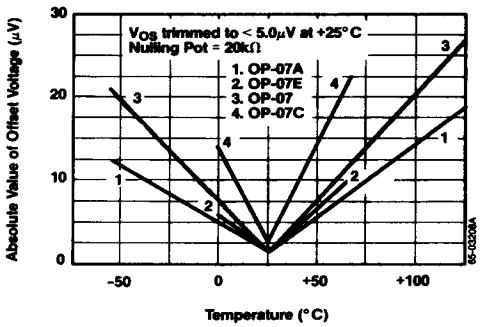
$$\Delta V_{OS}(25°C) \approx \frac{2.6mV\ (1 + B_3B_2B_1)R1}{R2 + R3} \quad (B_0 = 0)$$

Typical Performance Characteristics

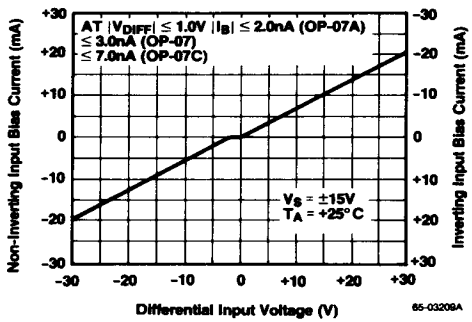
Untrimmed Offset Voltage vs. Temperature



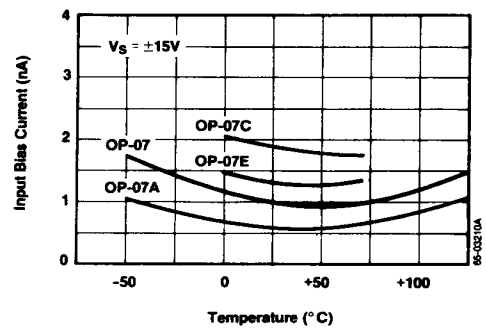
Trimmed Offset Voltage vs. Temperature



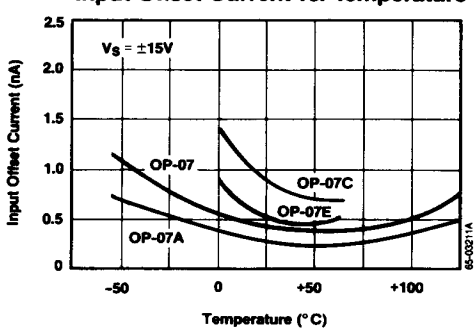
Input Bias Current vs. Differential Input Voltage



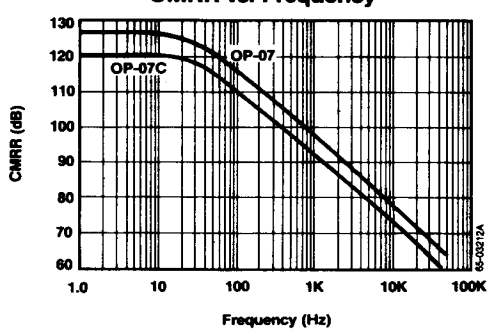
Input Bias Current vs. Temperature



Input Offset Current vs. Temperature

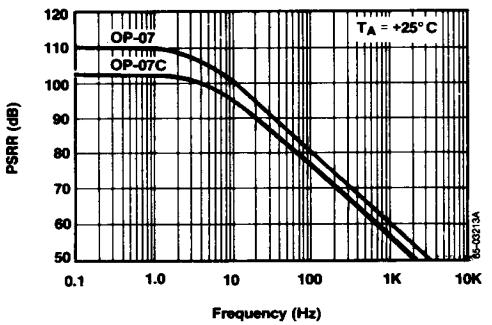


CMRR vs. Frequency

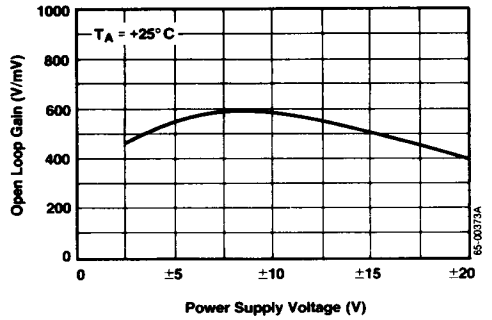


Typical Performance Characteristics (Continued)

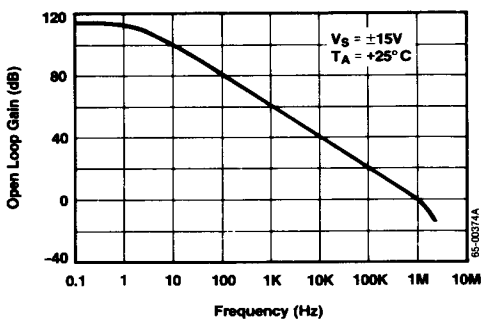
PSRR vs. Frequency



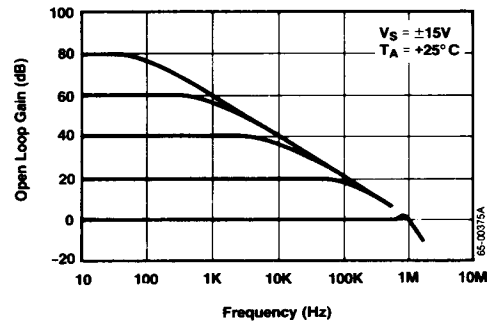
Open Loop Gain vs. Supply Voltage



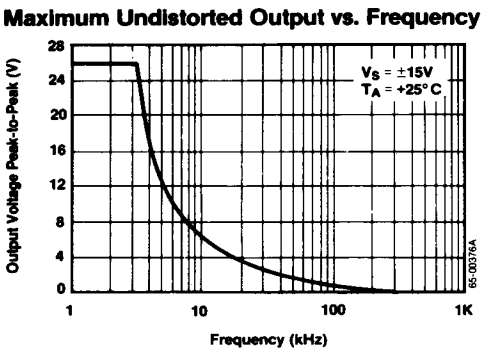
Open Loop Frequency Response



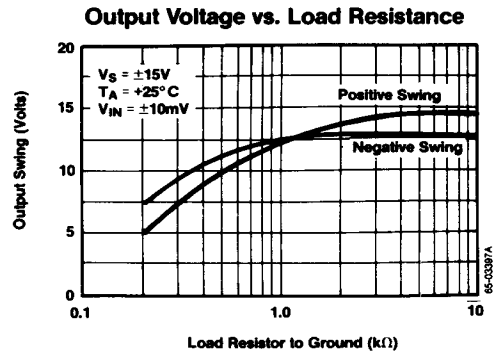
Closed Loop Response for Various Gain Configurations



Maximum Undistorted Output vs. Frequency

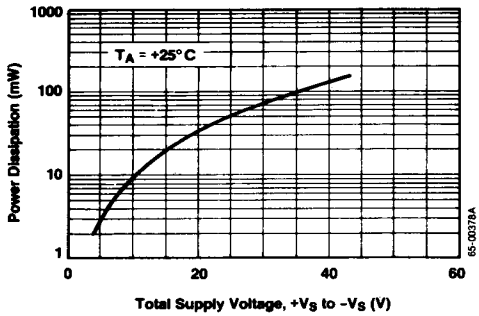


Output Voltage vs. Load Resistance

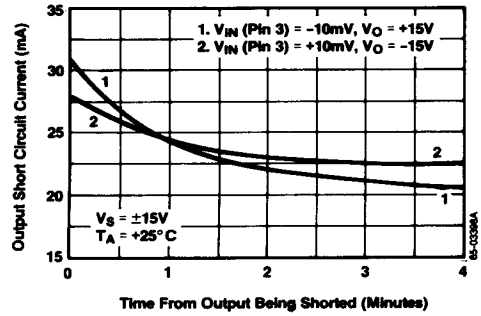


Typical Performance Characteristics (Continued)

Power Consumption vs. Supply Voltage

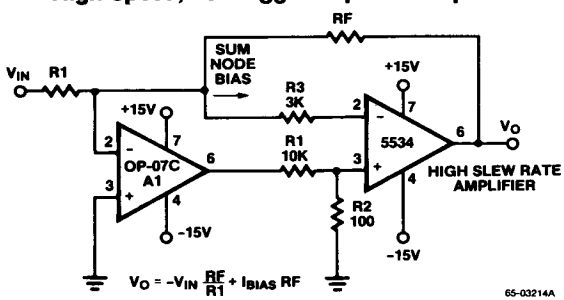


Output Short Circuit Current vs. Time

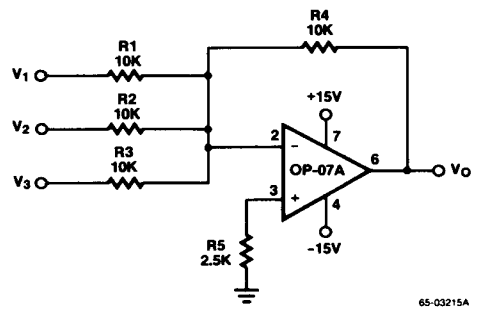


Typical Applications

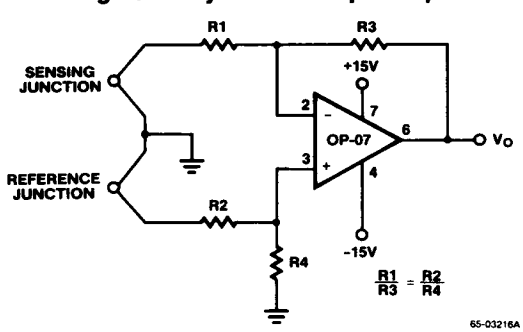
High Speed, Low V_{OS} Composite Amplifier*



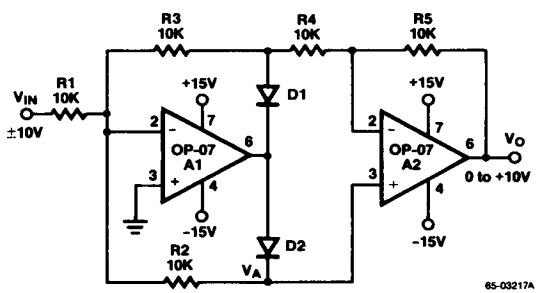
Adjustment-Free Precision Summing Amplifier*



High Stability Thermocouple Amplifier*

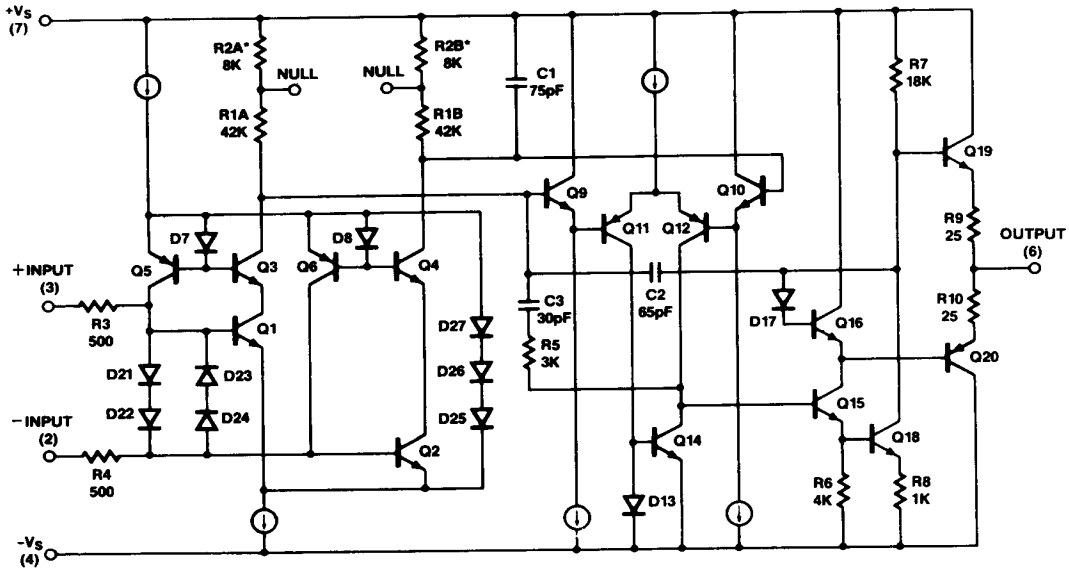


Precision Absolute Value Circuit*



*Pin outs shown for metal can packages

Schematic Diagram



*R2A and R2B are electronically adjusted during factory test for minimum V_{OS}.

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