Call progress decoder NE5900

DESCRIPTION

The NE5900 call progress decoder (CPD) is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor-controlled smart telephone capable of making preprogrammed telephone calls. The call progress decoder information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ring-back, busy signal, or re-order tones.

A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

FEATURES

- Fully decoded tri-state call progress status output
- Works with traditional, precision, or PBX call progress tones
- Low power consumption
- Low cost 3.58MHz crystal or clock
- No calibration or adjustment
- Interfaces with LSTLL, CMOS, NMOS
- Easy application

PIN CONFIGURATION

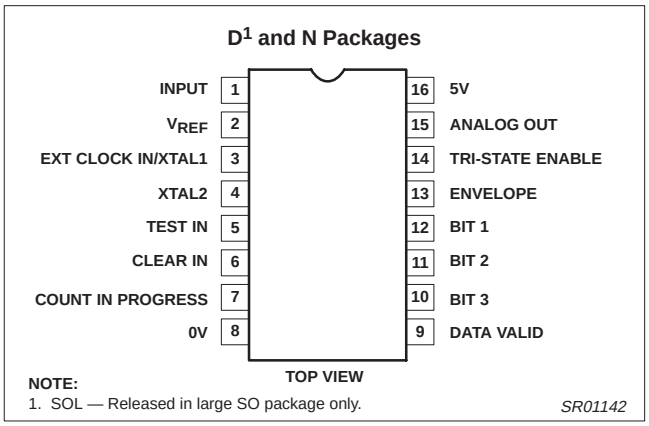

Figure 1. Pin Configuration

APPLICATIONS

- Modems
- PBXs
- Security equipment
- Auto dialers
- Answering machines
- Remote diagnostics
- Pay telephones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SOL) Package	0 to +70°C	NE5900DK	SOT162-1
16-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5900N	SOT38-4

BLOCK DIAGRAM

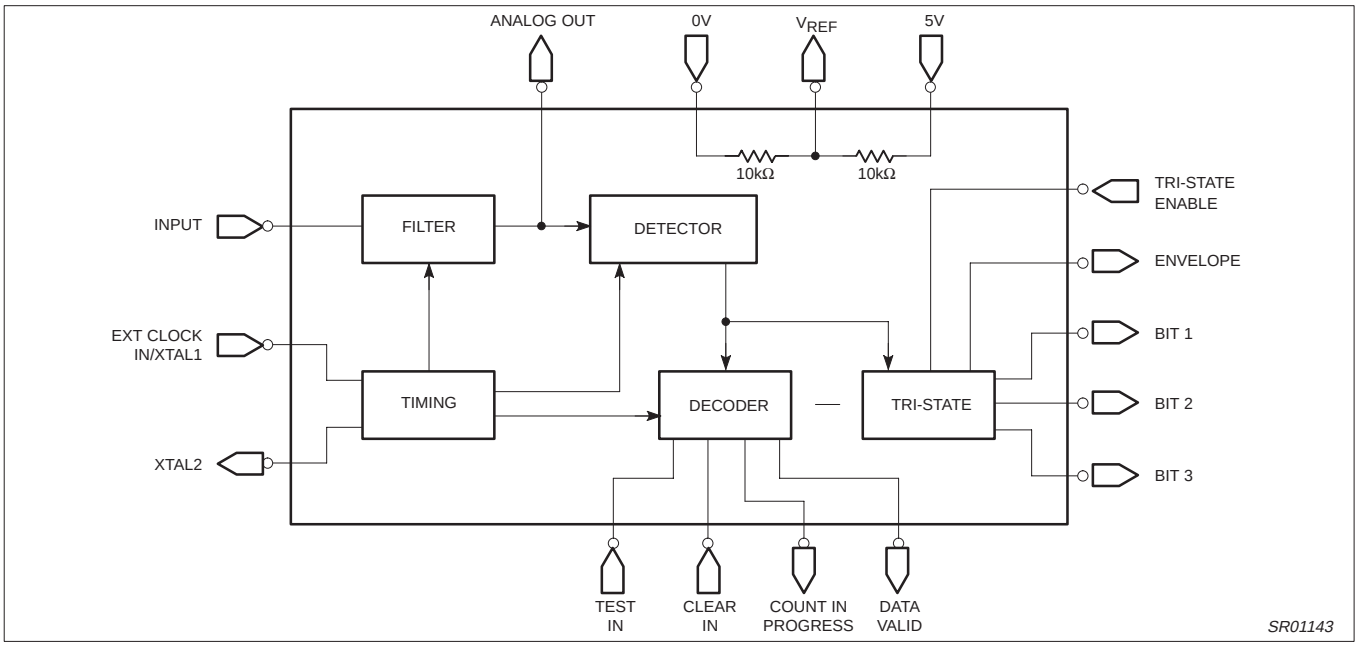

Figure 2. NE5900 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	9	V
V_{IN}	Logic control input voltages	-0.3 to +16	V
V_{IN}	All other input voltages[1]	-0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltages	-0.3 to V_{CC} + 0.3	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating temperature range	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10s)	+300	°C
T_{JMAX}	Junction temperature	+150	°C

NOTE:
1. Includes Pin 3 — Ext Clock In

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{DD}	Power supply voltage	Pin 16 Pin 14 = V_{DD} Pin 5, 6 = 0V	4.5	5.0	5.5	V
	Quiescent current	As above with no output loads		2.0	4.0	mA
	Input threshold	Pin 1 level, frequency = 460Hz, V_{DD} = V_{REF} Output Pin 13 = V_{DD}		-39	-35	dB[1]
	Signal rejection	Pin 1 level, frequency = 300Hz, V_{DD} = V_{REF} Output Pin 13 = 0V			-50	dB[1]
	Low frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V			180	Hz
	High frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V	800			Hz
V_{IH}	Logic 1 level	Pins 6, 14	2.0		15	V
V_{IL}	Logic 0 level	Pins 6, 14	0		0.8	V
I_{IH}	Logic 1 input current	Pins 3, 6, 14 = V_{DD}	-1.0		1.0	µA
I_{IL}	Logic 0 input current	Pins 3, 6, 14 = 0V	-1.0		1.0	µA
V_{IH}	Logic 1 input voltage	Pin 3 External Clock In/XTAL	V_{DD} – 1		V_{DD}	V
V_{IL}	Logic 0 input voltage	Pin 3 External Clock In/XTAL	0		1.0	V
V_{OL}	Logic 0 output voltage	I_{SINK} = 1.6mA Pins 7, 9, 10, 11, 12, 13	0		0.4	V
V_{OH}	Logic 1 output voltage	I_{SOURCE} = 0.5mA Pins 7, 9, 10, 11, 12, 13	V_{DD} – 0.4		V_{DD}	V
I_{OZ}	Tri-state leakage	V_{OUT} = V_{DD} or 0V Pins 10, 11, 12, 13, Pin 14 = 0V	-3.0		3.0	µA
	Filter output gain	Input Pin 1, 460Hz – 20dB, V_{DC} = V_{REF} Output Pin 15, R_{LOAD} = 1MΩ	6.5	8.5	10.5	dB
	Filter frequency response	As above from 300Hz to 630Hz, referenced to 460Hz	-1.0		1.0	dBmo
	Input impedance	Pin 1, frequency = 460MHz	1			MΩ
V_{REF}	Reference voltage	Pin 2, V_{DD} = 5V	2.4	2.5	2.6	V
R_{REF}	Reference resistance	Pin 2		5		Ω
	Envelope response time	Time from removal or application of 460Hz – 20dB (V_{DC} = V_{REF} on Pin 1) to response of Pin 13		38		ms

NOTE:
1. 0dB = 0.775V_{RMS}
2. By design; not tested.

The NE5900 uses the signal in the call progress tone passband and the cadence of interrupt rate of the signal to determine which call progress tone is present.

Figure 3 shows a detailed block diagram of the NE5900.

The signal input from the phone line is coupled through a 470kΩ resistor which, together with two internal capacitors and an internal resistor, form an anti-aliasing filter. This passive low pass filter strongly rejects AM radio interference. Insertion loss is typically 1.5dB at 460Hz. The 470kΩ resistor also provides protection from the transients. The input (Pin 1) DC voltage can be derived from V_{REF} (Pin 2) or allowed to self-bias through a series coupling capacitor (10nF minimum).

Following this is a switched capacitor bandpass filter which accepts call progress tones and inhibits tones not in the call progress band of 300Hz to 630Hz. The bandpass limits are determined by the input clock frequency of 3.58MHz. An on-board inverter between Pins 3 and 4 can be used either as a crystal oscillator or as a buffer for an external 3.58MHz clock signal. The switched capacitor filters provide typical rejection of greater than 40dB for frequencies below 120Hz and above 1.6kHz.

The decoder responds to signals between 300Hz and 630Hz with a threshold of -39dB typical (0dB = 0.775V_{RMS}). The decoder will not respond to any signal below -50dB or to tones up to 0dB which are below 180Hz or above 800Hz. Dropouts of 20ms or bursts of only 20ms duration are ignored. A gap of 40ms or a valid tone of 40ms is detected.

The buffered output of the switched capacitor filter is available at the analog output, Pin 15. A logic output representing the detected envelope of this signal is available at the envelope output, Pin 13.

At the start of an in-band tone (envelope output goes high), a 2.3 second interval is timed out. Transitions of the envelope during this interval are counted to determine the signal present. At 2.3 seconds, the three bits of data representing this decision are stored in the latch and appear at the outputs. A data valid signal goes high at this time, signaling that the data bits, Pins 10 – 12, can be read.

The output code is as follows:

	Pin 12	Pin 11	Pin 10
Dial Tone	0	0	0
Ringing Signal	1	0	0
Busy Signal	0	1	0
Re-order Tone	0	0	1
Overflow	1	1	1

The overflow condition occurs in the event that too many transitions occur during the 2.3 second interval. This can result from noise, voice, or other line disturbances not normally present during the post-dialing interval. Note that the end of dial tone in interpreted as a valid ringing signal.

The clear input resets all internal registers and the output latch, and is to be set low after the completion of dialing. The clear input should be pulsed high for proper operation. Recommended pulse width is between 0.2µs and 20ms. If clear is held high when envelope is high, a false output pulse (Pin 13) can result when clear is returned low.

For applications where dialing is done by a person rather than by a microprocessor, an uncertainty exists about the number of digits to be dialed (local vs long distance). In such situations it is possible to clear the NE5900 by application of the DTMF signal or dial pulses to the clear pin (Pin 6). When dialing is complete, the device is cleared and ready to respond to the next call progress unit.

Enable is held at 5V to enable Pins 10, 11, 12 and 13. When enable is brought low, data valid is also set low. Enable must remain high while the data is also set low. Enable must remain high while the data is being read. The test pin is for production test only and must be kept low in all user applications.

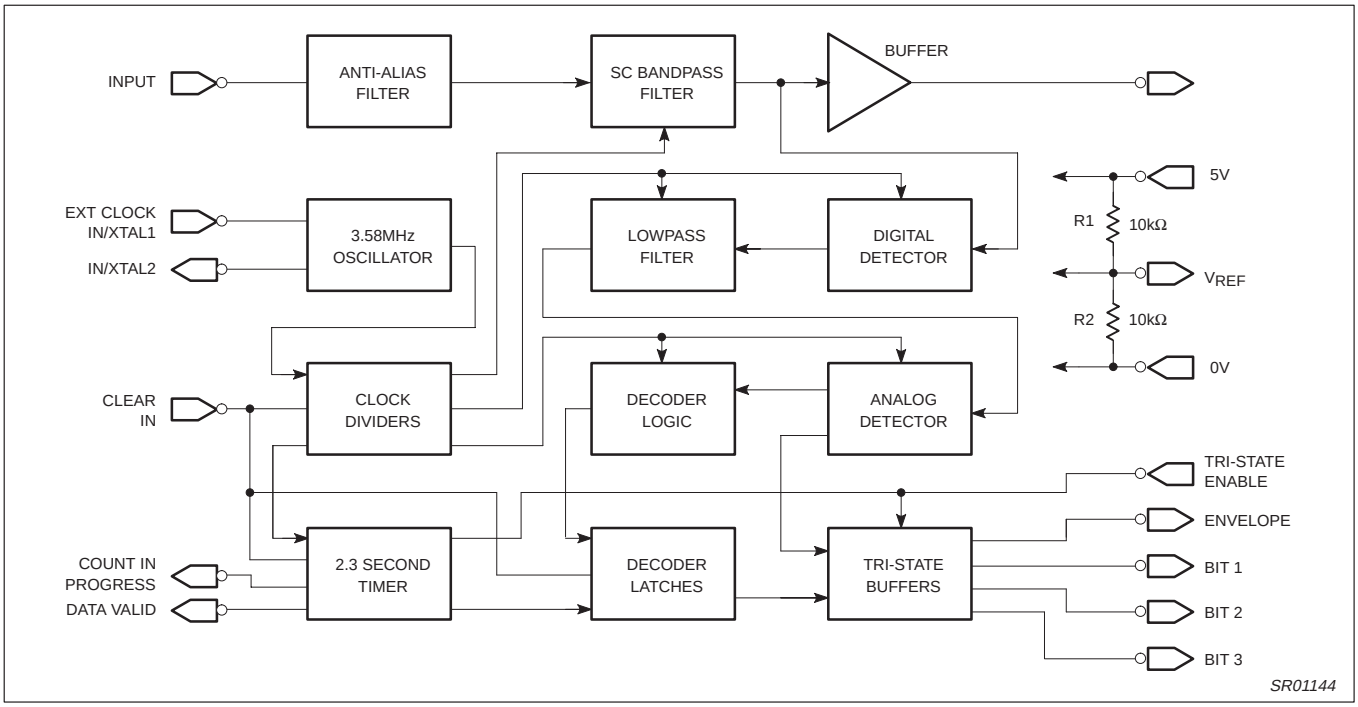

Figure 3. Detailed Block Diagram CPD

Figure 4 shows a typical application of the call progress decoder.

In this application only one external component is needed an no microprocessor activity other than clear is required.

Figure 5 shows the recommended direct interface to the telephone line. Bus connection is possible by utilizing tri-state, and internal timing is accomplished with a 3.58MHz crystal.

The designer can utilize the input signal, clock, bus, or microprocessor interface which best serves the application. Figure 6 gives a typical timing diagram for the application of Figures 4 and 5.

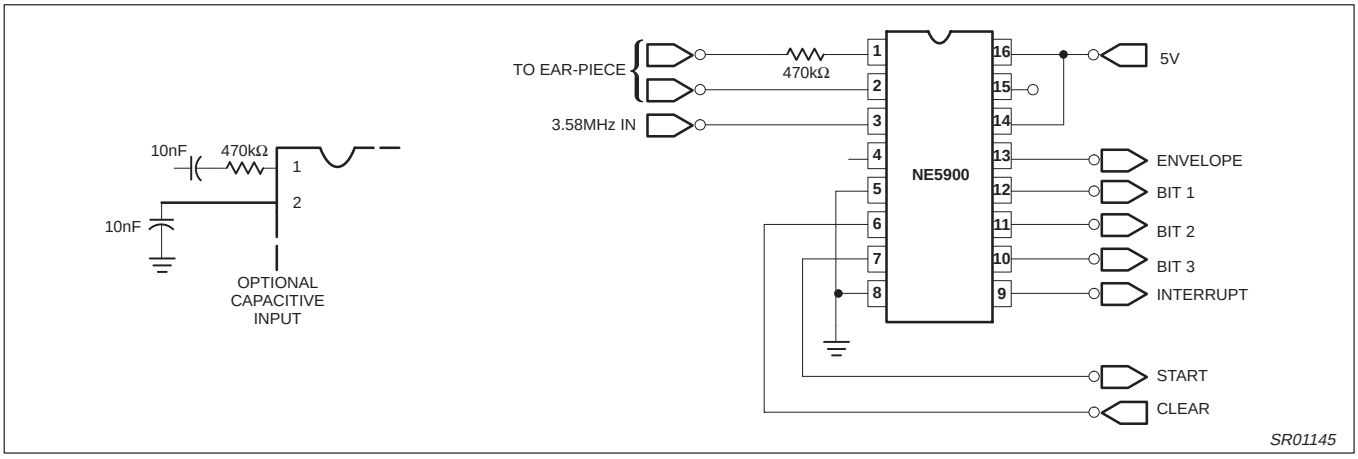

Figure 4. Typical Application

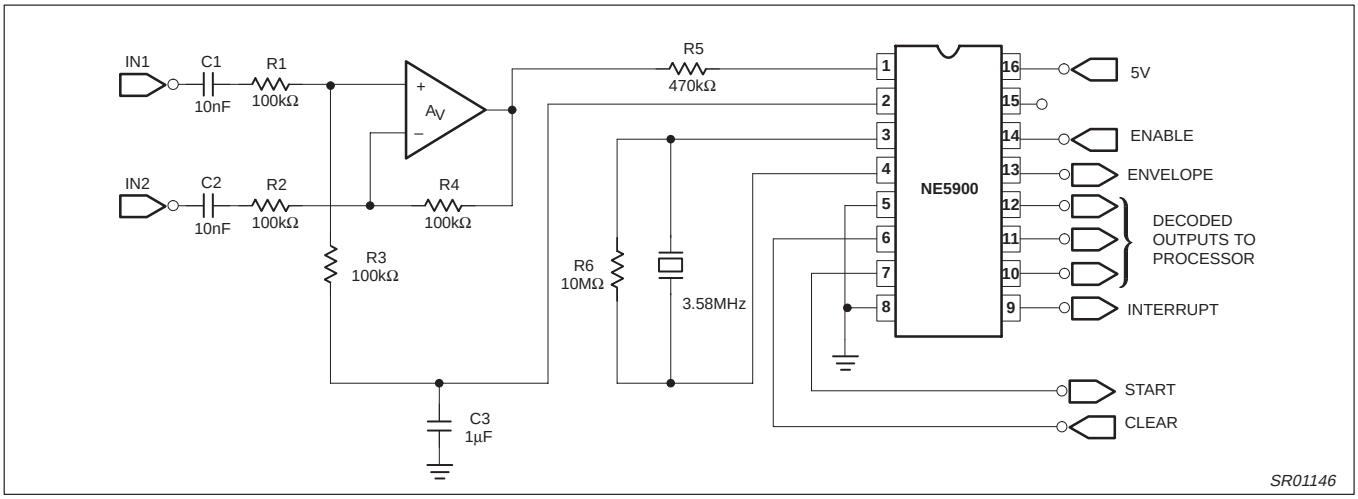

Figure 5. Typical Two-Wire Application

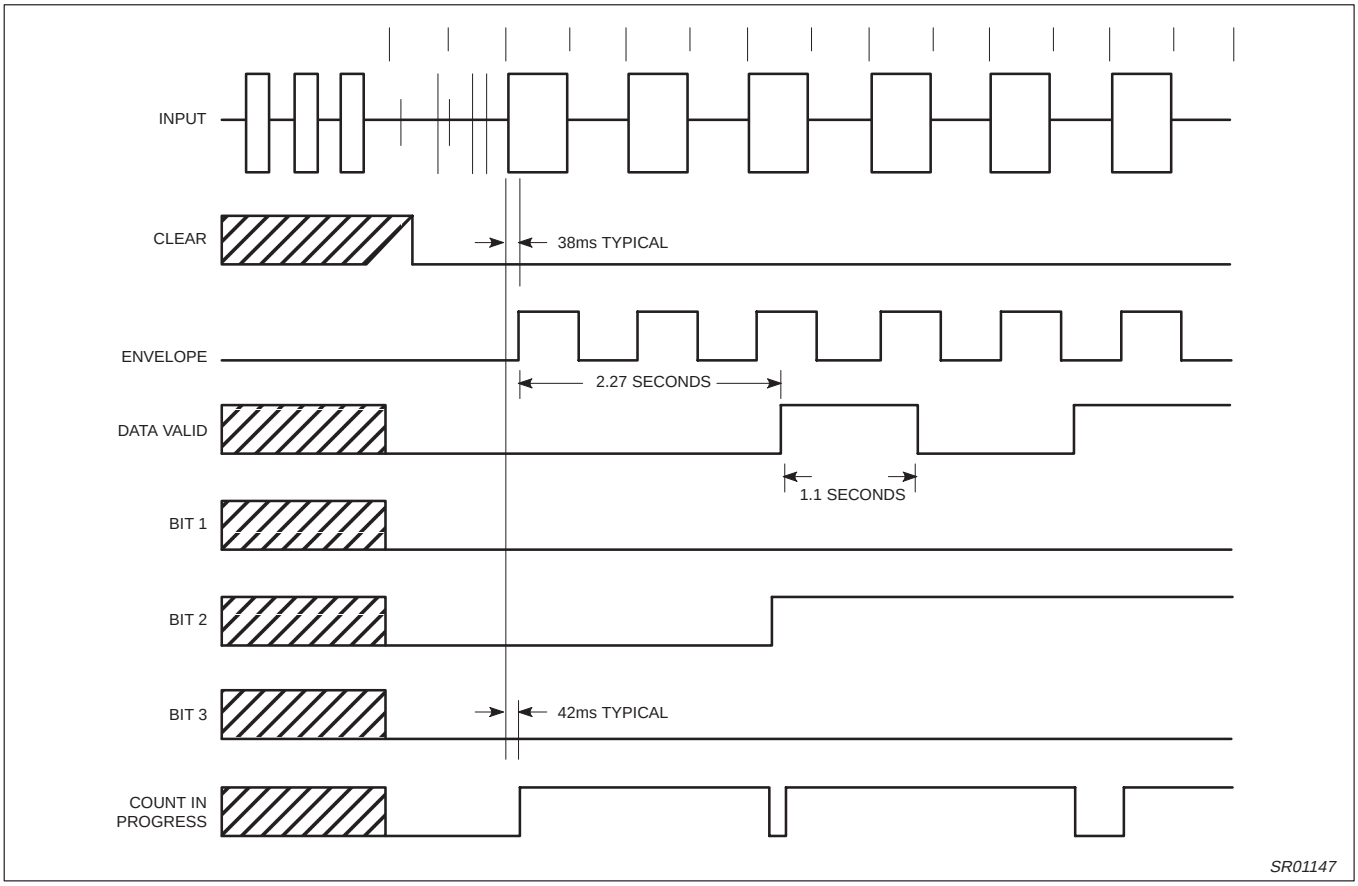
INPUT
CLEAR
38ms TYPICAL
ENVELOPE
2.27 SECONDS
DATA VALID
1.1 SECONDS
BIT 1
BIT 2
BIT 3
42ms TYPICAL
COUNT IN PROGRESS
SR01147

Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS

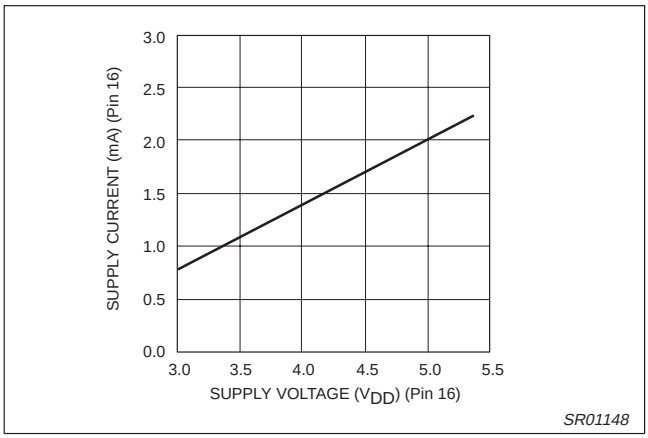

Figure 7. Power Supply Current vs V_{DD}

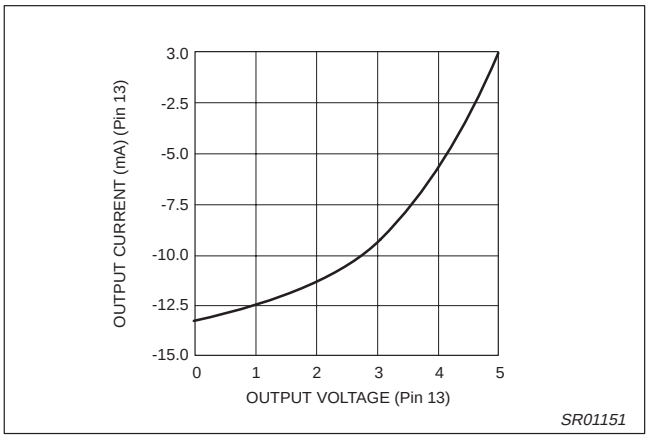

Figure 10. Output Voltage Current Curve Digital Output High

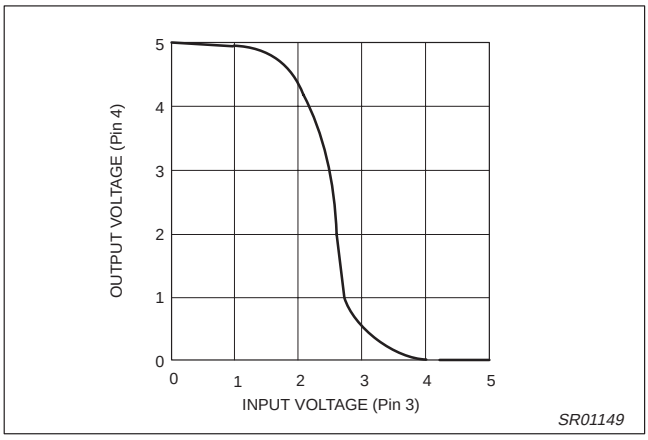

Figure 8. Voltage Transfer Curve

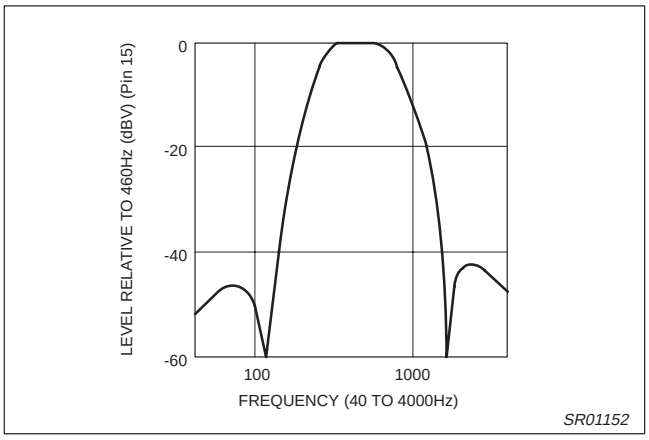

Figure 11. Filter Frequency Response

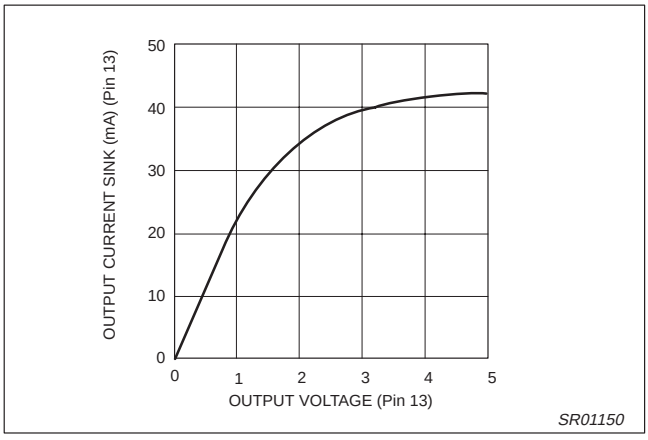

Figure 9. Digital Output Low

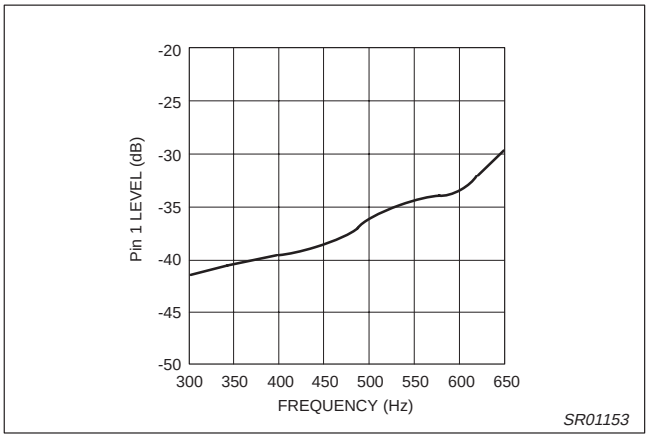

Figure 12. Typical Threshold