64-BIT BIPOLAR WRITE-WHILE-READ RAM (32 × 2) — 82S21 (O.C.)

82S21

DESCRIPTION

The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5-input decoder when the chip enable input, CE is at logic high. $\overline{WS_0}$ and $\overline{WS_1}$ are the write select inputs for the bit 0 and bit 1 of the word selected. $\overline{WE}$ is the write control input. When $\overline{WS_N}$ and $\overline{WE}$ are both at logic low data on the DI_0 and DI_1 data lines are written into the addressed word. The read function is enabled when either $\overline{WS_N}$ or $\overline{WE}$ is at logic high.

An internal latch provides the Write-While-Read capability. When the latch control line (strobe) is logic high and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When strobe goes from a logic high to logic low, the outputs are latched and will remain latched regardless of the state of any other address or control line. When strobe goes from low to high, the outputs unlatch and will assume the contents of the present address word.

FEATURES

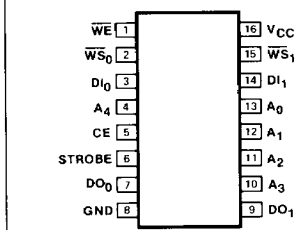
- **Address access time: 50ns max**
- **Write cycle time:**
  - **Transparent mode: 45ns max**
  - **Latched mode: 60ns max**
- **Power dissipation: 7.5mW/bit typ**
- **32mA output sink capability**
- **On-chip output latches**
- **Bit masking control lines**
- **Write-While-Read function**
- **Non-inverting open collector outputs**
- **TTL compatible**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Accumulator register**
- **Control store**

PIN CONFIGURATION

F,N PACKAGE



TOP VIEW

*F - Cerdip
N - Plastic

TRUTH TABLE

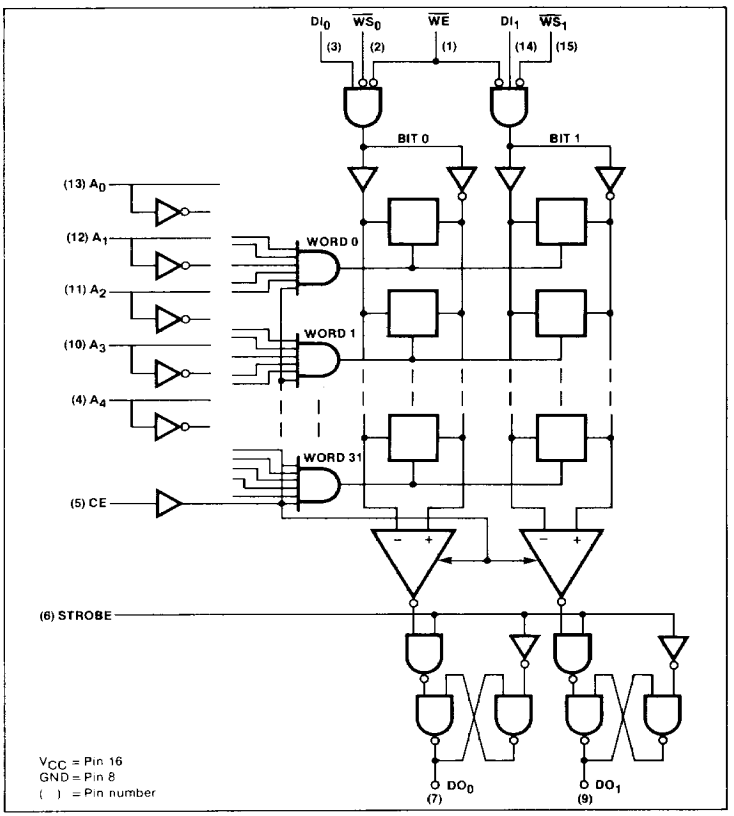
CE	$\overline{WE}$	$\overline{WS_0}$	$\overline{WS_1}$	STROBE	MODE	OUTPUTS
X	X	X	X	0	Output hold	$DO_N = (A_M)$ at last CE = high
0	X	X	X	0	Disabled	DO_N = high
1	1	X	X	1 or ↓	Read (transparent/latched)	$DO_N = (A_M)$
1	0	1	1	1 or ↓	Read (transparent/latched)	
1	0	0	0	0	Write data	$DO_N = (A_M)$ at last strobe = ↓
1	0	0	0	1	Write data	$DO_N = DI_N$
1	0	0	1	X	Write data into bit 0 only	If strobe = low: $DO_N = (A_M)$ at last strobe = ↓
1	0	1	0	X	Write data into bit 1 only	If strobe = high: $DO_N = DI_N$ or (A_M) as per $\overline{WS_N}$

( ) = Contents of
↓ = High to low transition

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_{OH}	Output voltage	+5.5	Vdc
I_{IN}	Input current	-30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER[1]		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low[1]	V_{CC} = 4.75V			0.80	
V_{IH}	High[1]	V_{CC} =5.25V	2			
V_{IC}	Clamp[1,2]	V_{CC} = 4.75V, I_{IN} = −12mA			-1.2	
	Output voltage					V
V_{OL}	Low[1,3]	V_{CC} = 4.75V, I_{OL} = 32mA			0.45	
	Input current					
I_{IL}	Low	V_{IN} = 0.45V			-1.6	mA
I_{IH}	High	V_{IN} = 5.5V			25	μA
	Output current	V_{CC} = 5.25V				μA
I_{OLK}	Leakage[4]	V_{OUT} = 5.25V			40	
I_{CC}	V_{CC} supply current[5]	V_{CC} = 5.25V			130	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

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AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 150\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Access time							ns
T_{AA} Address	Output	Address	Latched or transparent read			50	
T_{CE} Chip enable	Output	Chip enable				50	
Disable time							ns
T_{CD} Chip enable	Output	Chip enable	Latched or transparent read			50	
Setup and hold time							ns
T_{WSA} Setup time	Write	Address	Latched or transparent write	15			
T_{WHA} Hold time				5			
T_{WSD} Setup time	Write	Data in	Latched or transparent write	25			
T_{WHD} Hold time				5			
T_{WSC} Setup time	Write	CE	Latched or transparent write	15			
T_{WHC} Hold time				5			
T_{CES} Setup time	Strobe	Chip enable	Latched read	50			
T_{CEH} Hold time				5			
T_{ADH} Hold time	Output	Address	Latched read	5			
Pulse width							ns
T_{SW} Strobe			Latched read	30			
T_{WP} Write inputs			Latched or transparent write	25			
Latch time							ns
T_{SLR} Read strobe	Strobe	Address	Latched read	50			
T_{SLW} Write strobe	Strobe	Write	Latched write	40			
T_{LRW} WWR strobe	Write	Strobe	Write while read	10			
Delatch time							ns
T_{DL} Strobe	Output	Strobe	Latched read			25	
T_{WD} Valid time	Output	Write	Latched or transparent write			40	ns

NOTES
1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
4. Measured with V_{IL} applied to CE, and V_{IH} to strobe.
5. I_{CC} is measured with all inputs at 4.5V, and the outputs open.

MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable high (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes low and Data Output is in high state.

T_{AA} Delay between beginning of valid Address (with Chip Enable high) and when Data Output becomes valid.

T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.

T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.

T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.

T_{WSD} Required delay between beginning of valid Data Input and end of Write Enable pulse.

T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.

T_{WP} Width of Write Enable pulse.

T_{WD} Delay between beginning of Write Enable pulse and when Data Output reflects the contents of the Data Input.

T_{CES} Minimum delay between leading edge of Chip Enable and trailing edge of Strobe, for latching valid output data.

T_{CEH} Required delay between trailing edge of Strobe and end of Chip Enable, for latching valid output data.

T_{SLR} Minimum delay between Address valid time and trailing edge of Strobe, for latching valid output data.

T_{SW} Minimum width of Strobe pulse required to update contents of output data latches.

T_{ADH} Required delay between trailing edge of Strobe and end of valid Address.

T_{DL} Delay between leading edge of Strobe and when output data latches are released.

T_{LRW} Minimum delay required between trailing edge of Strobe and leading edges of Write Enable or Write Select for latching old output data (being read) while new data is being written (at the same address).

T_{SLW} Minimum delay between leading edge of Write Enable or Write Select and trailing edge of Strobe for latching data being written in output data latches.

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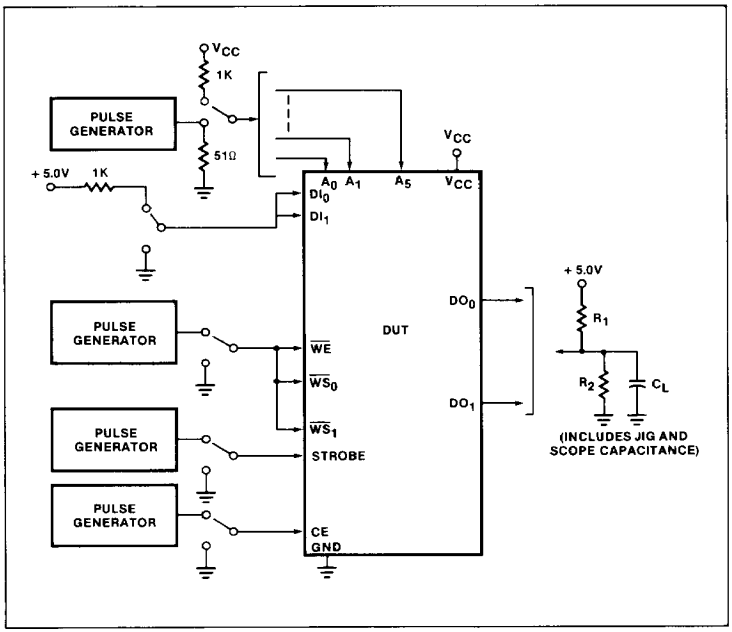
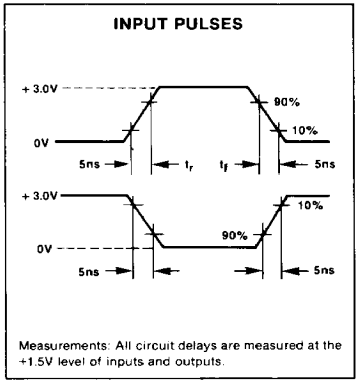
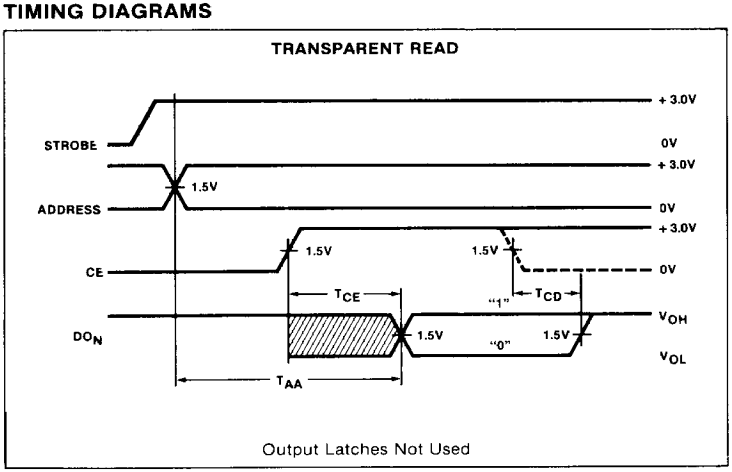
TEST LOAD CIRCUIT



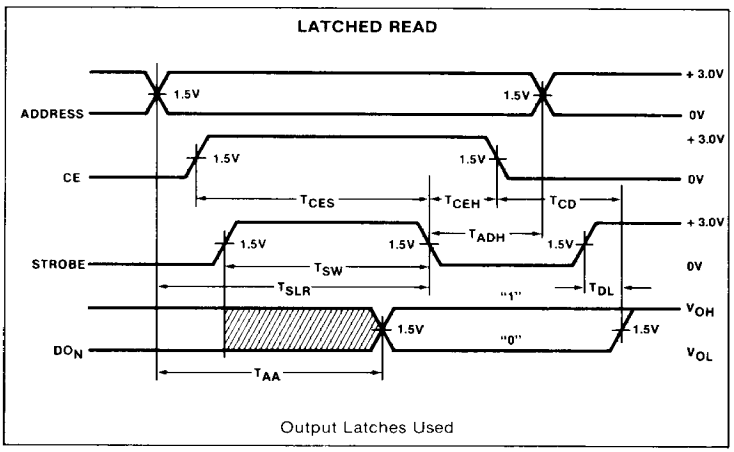
VOLTAGE WAVEFORM

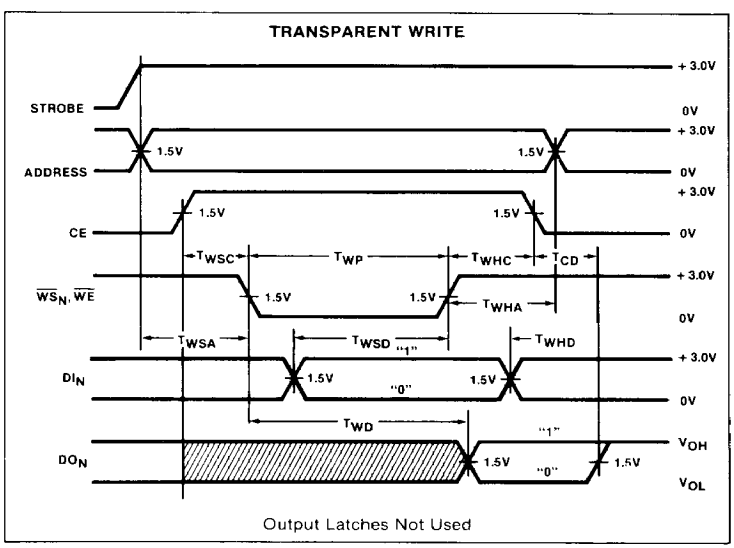


TIMING DIAGRAMS

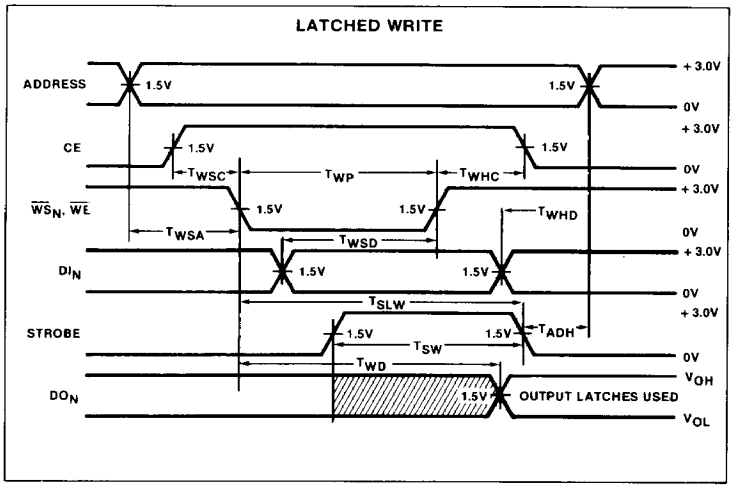


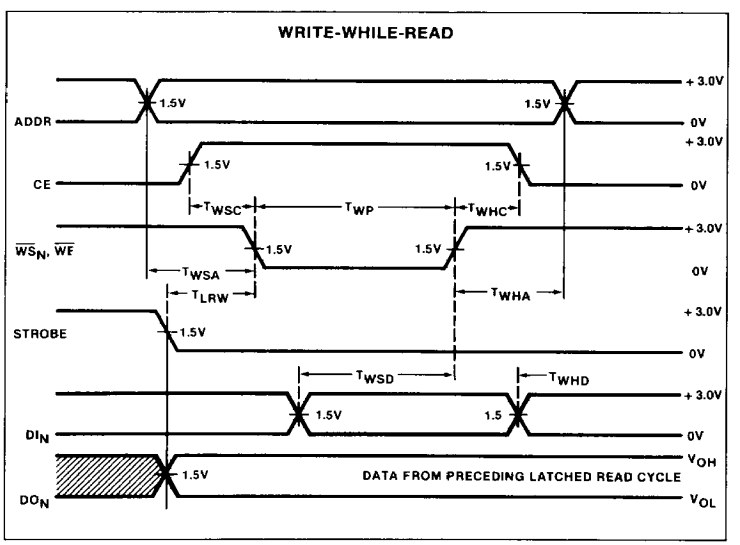
TIMING DIAGRAMS (Cont'd)





TIMING DIAGRAMS (Cont'd)





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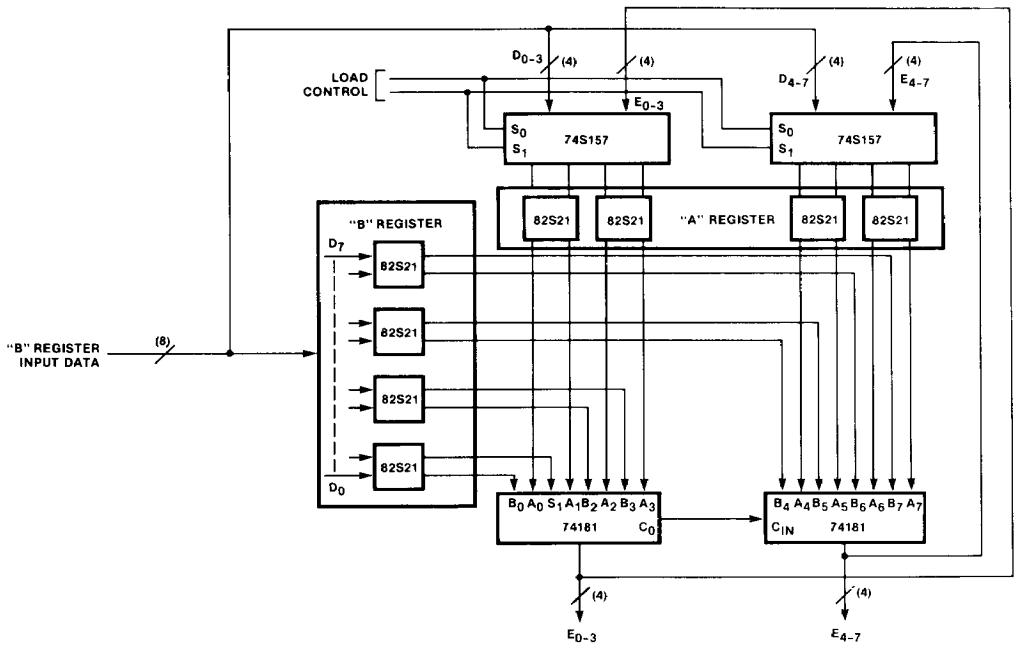
TYPICAL APPLICATION

BASIC 8-BIT FULLY BUFFERED ACCUMULATOR



By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32X8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B → A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.