

DESCRIPTION

The 82S114 and 82S115 are field programmable and include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by \overline{CE}_1 and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

Both 82S114 and 82S115 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S114/115, F or N, and for the military temperature range (-55°C to +125°C) specify S82S114/115, F.

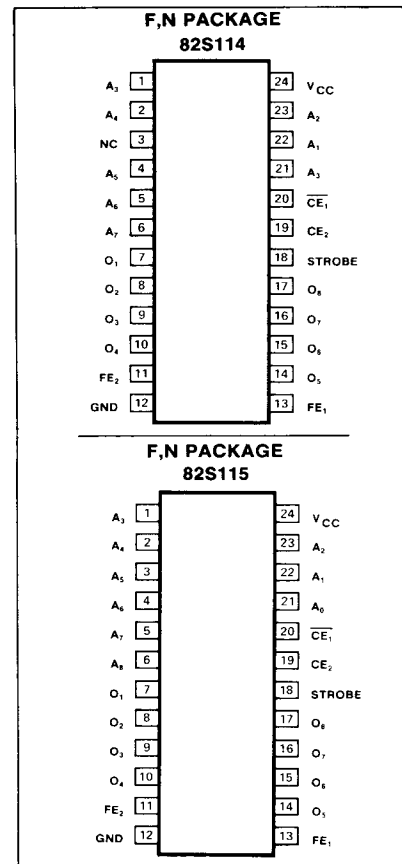
FEATURES

- **Address access time:**
N82S114/115: 60ns max
S82S114/115: 90ns max
- **Power dissipation: 165μW/bit typ**
- **Input loading:**
N82S114/115: -100μA max
S82S114/115: -150μA max
- **On-chip storage latches**
- **Schottky clamped**
- **Fully TTL compatible**

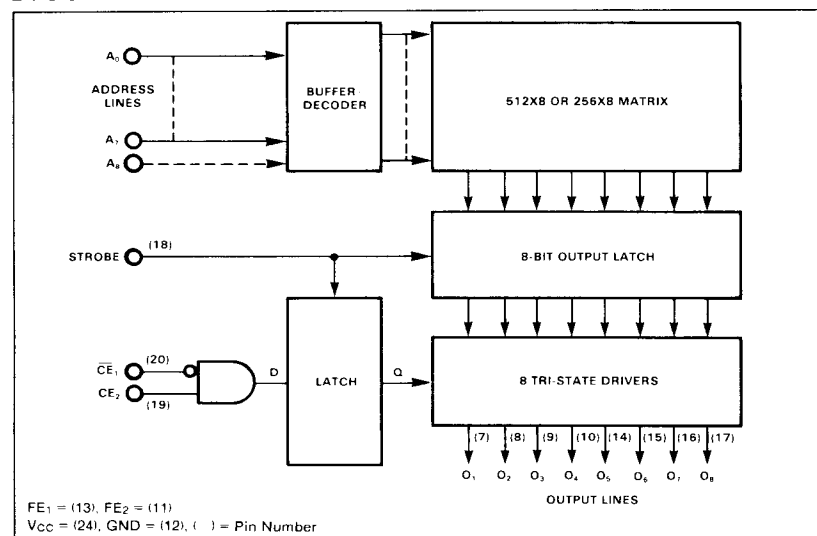
APPLICATIONS

- **Microprogramming**
- **Hardwire algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATIONS



BLOCK DIAGRAM



BIPOLAR MEMORY

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
T _A	Temperature range		°C
	Operating	0 to +75	
	N82S114/115	-55 to +125	
T _{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N82S114/115: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S114/115: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ⁶	N82S114/115			S82S114/115			UNIT
		Min	Typ ¹	Max	Min	Typ ¹	Max	
V _{IL}	Input voltage Low	2.0	-0.8	-1.2	2.0	-0.8	-1.2	V
V _{IH}	High							
V _{IC}	Clamp							
	I _{IN} = -18mA							
V _{OL}	Output voltage Low	2.7	0.4	0.45	2.4	0.4	0.5	V
V _{OH}	High							
	I _{OUT} = 9.6mA \overline{CE}_1 = Low, CE ₂ = High, I _{OUT} = -2mA, High stored							
I _{IL}	Input current Low			-100			-150	μA
I _{IH}	High							
	V _{IN} = 0.45V V _{IN} = 5.5V			25			50	
I _{O(OFF)}	Output current Hi-Z state	-20		40			100	μA
I _{OS}	Short circuit ²							
	\overline{CE}_1 = High or CE ₂ = 0, V _{OUT} = 5.5V \overline{CE}_1 = High or CE ₂ = 0, V _{OUT} = 0.5V V _{OUT} = 0V			-40	-15		-100	
I _{CC}	V _{CC} supply current		130	175		130	185	mA
C _{IN}	Capacitance Input		5			5		pF
C _{OUT}	Output							
	V _{CC} = 5.0V, V _{IN} = 2.0V V _{CC} = 5.0V, V _{OUT} = 2.0V \overline{CE}_1 = High or CE ₂ = 0		8			8		

AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S114/115: 0° ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S114/115: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

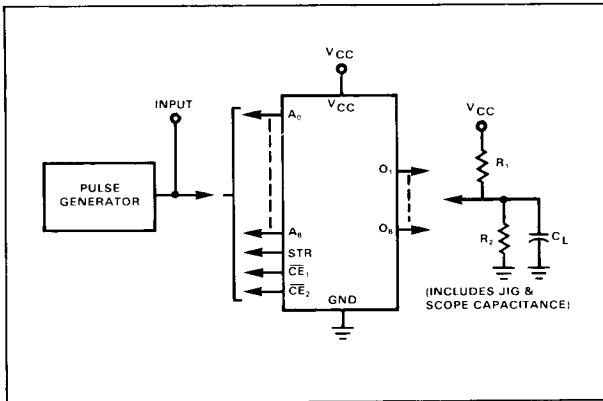
PARAMETER	TO	FROM	TEST CONDITIONS	N82S114/115			S82S114/115			UNIT	
				Min	Typ ¹	Max	Min	Typ ¹	Max		
T _{AAT} ⁷	Output	Address	Latched or transparent read ^{3,5}		35	60		35	90	ns	
T _{CE}											Output
T _{CD}	Output	Chip disable		20	40		20	55	ns		
T _{CDS}	Output	Chip enable	Latched read only ^{4,5}	40	10	0	50	15	0	ns	
T _{CDH}											Hold time
T _{ADH}											Hold time
T _{SW}				30	20		40	20	ns		
T _{SL}				60	35		90	35	ns		
T _{DL}								45	ns		
								30			

NOTES on following page

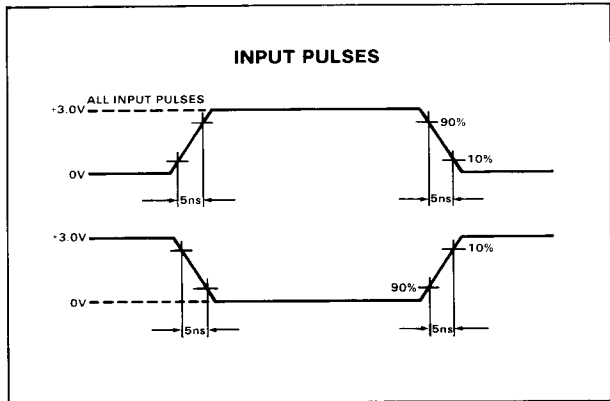
NOTES

1. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25^\circ C$.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
3. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.
4. In latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
5. During operation the fusing pins FE1 and FE2 may be grounded or left floating.
6. Positive current is defined as into the terminal referenced.
7. Tested at an address cycle time of $1\mu sec$.

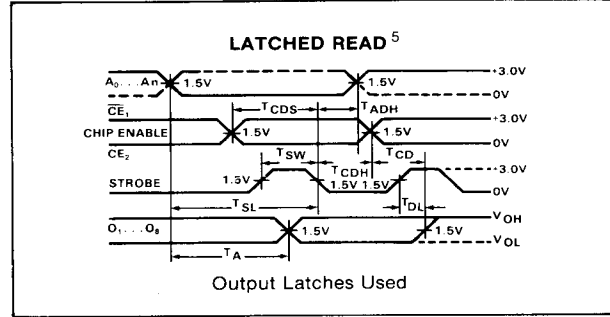
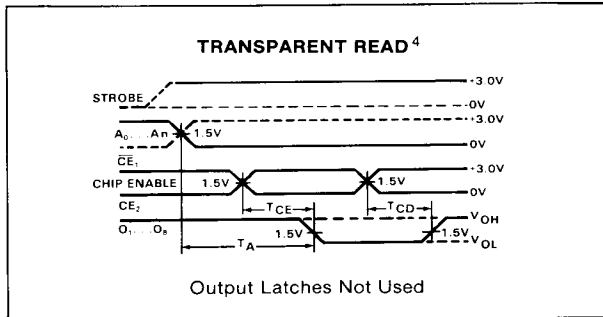
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAMS



PROGRAMMING SYSTEM SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CCP} Power supply voltage To program ¹	$I_{CCP} = 200 \pm 25\text{mA}$, Transient or steady state	4.75	5.0	5.25	V
V_{CCVH} Verify limit Upper		5.3	5.5	5.7	V
V_{CCVL} Lower		4.3	4.5	4.7	
V_S Verify threshold ²		0.9	1.0	1.1	V
I_{CCP} Programming supply current	$V_{CCP} = +5.0 \pm .25\text{V}$	175	200	225	mA
V_{IL} Input voltage Low		0	0.4	0.8	V
V_{IH} High		2.4		5.5	
I_{IL} Input current (FE ₁ & FE ₂ only) Low	$V_{IL} = +0.45\text{V}$			-100	μA
I_{IH} High	$V_{IH} = +5.5\text{V}$			10	mA
I_{IL} Input current (except FE ₁ & FE ₂) Low	$V_{IL} = +0.45\text{V}$			-100	μA
I_{IH} High	$V_{IH} = +5.5\text{V}$			25	
V_{OPF} Forced output voltage (program) ³	$I_{OPF} = 200 \pm 20\text{mA}$, Transient or steady state $V_{OPF} = +17 \pm 1\text{V}$	16.0	17.0	18.0	V
I_{OPF} Forced output current (program)		180	200	220	mA
T_R Output pulse rise time		10		50	μs
t_p FE ₂ programming pulse width		0.3	0.4	0.5	ms
T_D Pulse sequence delay		10			μs
T_{PR} Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS} Programming pause	$V_{CC} = 0\text{V}$	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$ Programming duty cycle ⁴				50	%

PROGRAMMING NOTES

- Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
- V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
- Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle.
- Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0\text{V}$) of 3ms.

RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical low. To write logical high, proceed as follows:

SET-UP

- Apply GND to pin 12.
- Terminate all device outputs with a $10\text{k}\Omega$ resistor to V_{CC} .
- Set \overline{CE}_1 to logic low, and \overline{CE}_2 to logic high (TTL levels).
- Set Strobe to logic high level.

Program-Verify Sequence

- Raise V_{CC} to V_{CCP} , and address the word to be programmed by applying TTL high and low logic levels to the device address inputs.
- After $10\mu\text{s}$ delay, apply to FE₁ (pin 13) a voltage source of $+5.0 \pm 0.5\text{V}$, with 10mA

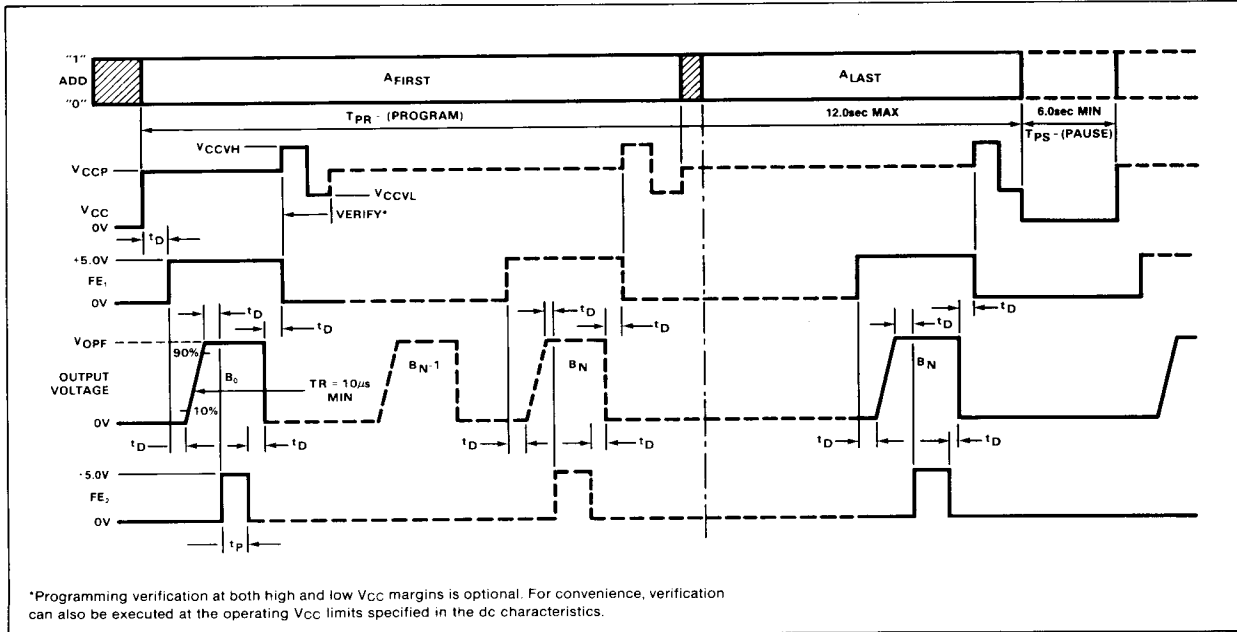
sourcing current capability.

- After $10\mu\text{s}$ delay, apply a voltage source of $+17.0 \pm 1.0\text{V}$ to the output to be programmed. The source must have a current limit 200mA. Program on output at the time.
- After $10\mu\text{s}$ delay, raise FE₂ (pin 11) from 0V to $+5.0 \pm 0.5\text{V}$ for a period of 1ms, and then return to 0V. Pulse source must have a 10mA sourcing current capability.
- After $10\mu\text{s}$ delay, remove $+17.0\text{V}$ supply from programmed output.
- To verify programming, after $10\mu\text{s}$ delay, return FE₁ to 0V. Raise V_{CC} to $V_{CCH} = +5.5 \pm .2\text{V}$. The programmed output should remain in the high state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2\text{V}$, and verify that the programmed output remains in the high state.
- Raise V_{CC} to V_{CCP} and repeat steps 2 through 6 to program other bits at the

same address.

- Repeat steps 1 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



BIPOLAR MEMORY