27960CX
PIPELINED BURST ACCESS 1M (128K x 8) CHMOS EPROM

- **Synchronous 4 Byte Data Burst Access**
- **No Glue Interface to 80960CA**
- **High Performance Clock to Data Out**
  - **— Zero Wait State Data to Data Burst**
  - **— Up to 33 MHz 80960CA Performance**
- **Asynch Microcontroller Reset Function**
  - **— Returns to Known State with High-Z Outputs**
- **Pipelined Addressing for Optimal Bus Bandwidth on 80960CA**
  - **— Next Addressing Overlaps Last Data Byte**
- **CHMOS III-E for High Performance and Low Power**
  - **— 125 mA Active, 30 mA Standby**
  - **— TTL Compatible Inputs**
- **1 Mbit Density Configures as 128K x 8**

Intel's 27960CX is a 5V only, 1,048,576 bit, Erasable Programmable Read Only Memory, organized as 128K words of 8 bits.

The 27960CX provides a no glue synchronous burst interface to the 80960CA bus. Internally the 27960CX is organized in 4 byte blocks, in which each byte is accessed sequentially. The internal state machine is factory configured to generate either 1 or 2 wait-states between the address and first data byte. High performance outputs provide zero wait-state data to data accesses at clock frequencies up to 33 MHz.

Pipelining capability allows addresses to overlap previous data, further optimizing bus bandwidth in 80960CA applications. An asynchronous microcontroller $\overline{\text{RESET}}$ feature puts the outputs in the high impedance state and takes the internal state machine to a known state where a new burst access can begin.

The 27960CX is available in 44-lead PLCC package, providing optimum cost effectiveness.

The 27960CX is manufactured on Intel's 1 micron CHMOS III-E technology. The Quick-Pulse Programming™ algorithm provides fast, reliable programming with throughput under 17 seconds for optimized equipment.

*CHMOS is a Patented Process of Intel Corporation.

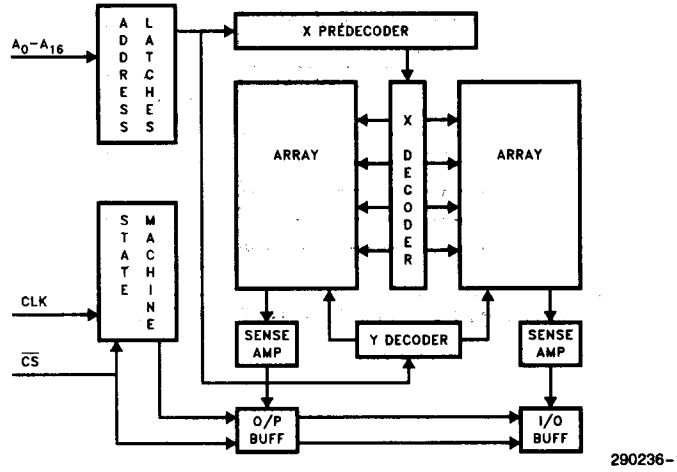

Figure 1. 27960CX Burst EPROM Block Diagram

September 1991
Order Number: 290236-006

27960CX BURST EPROM

EPROMs are established as the preferred code storage device in embedded applications. The non-volatile, flexible, reliable, cost effective EPROM makes a product easier to design, manufacture and service. Until recently, however, EPROMs could not match the performance needs of high-end systems. The 27960CX was designed to support the 80960CA embedded processor. It utilizes the burst interface to offer near zero wait-state performance without the high cost normally associated with this performance.

In embedded designs, board space and cost must be kept at a minimum without impacting performance and reliability. The 27960CX removes the need for expensive high-speed shadow RAM backed up by slow EPROM or ROM for non-volatile code storage. Code optimization concerns are reduced with "off-chip" code fetches no longer crippling to system performance. FONTs can be run directly out of these EPROMs at the same performance as high-speed DRAMs. With the 27960CX, the EPROM is the ideal code or FONT storage device for your 80960CA system.

Architecture

The 27960CX provides a no-glue, synchronous burst interface to the 80960CA's bus. It operates in pipelined or non-pipelined modes. Internally, the 27960CX is organized in 4 byte blocks which are accessed sequentially. A burst access begins on the first clock pulse after $\overline{ADS}$ and $\overline{CS}$ are asserted. The address of the 4 byte block is latched on the rising edge of clock following $\overline{ADS}$. After a preset number of wait-states (1 or 2), data is output one byte at a time on each subsequent clock cycle. A burst access is terminated on the rising edge of clock with $\overline{BLAST}$ asserted. High performance outputs provide zero wait-state data to data accesses at clock frequencies up to 33 MHz. Extra power and ground pins dedicated to the outputs reduce the effects of fast output switching on device performance.

The pipelining capability of the 27960CX allows the address to overlap the last data byte of the burst, further optimizing bus band width in 80960CA applications. In the pipelined mode, with a non-buffered interface, the 27960CX delivers 4 bytes of data in 6 clock cycles at 33 MHz. In a 32-bit configuration, this translates into a read bandwidth of 88 Mbytes/sec. Performance capability of the 27960CX in different 80960CA systems is given in Table I.

*CERQUAD is available in a socket only version.

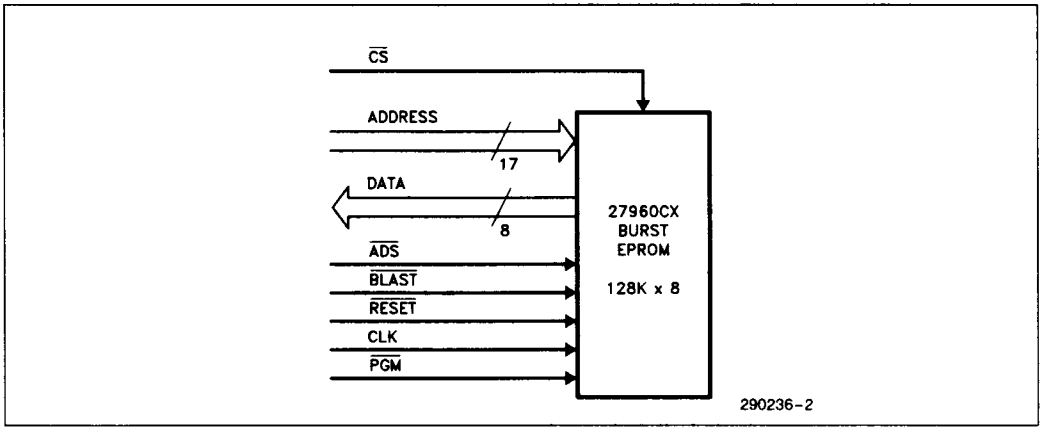

Figure 2. 27960CX Burst EPROM Signal Set

Table 1. Performance Capability

33 MHz 2 WS Non-Buffered: 4 Words/6 Clock Cycles → 88 Mbytes/Sec

ADDR	A_{00}	WS	WS	—	—	—	A_{01}	WS	WS	—	—	—	A_{02}	WS
DATA	—	—	—	D_{00}	D_{01}	D_{02}	D_{03}	—	—	D_{10}	D_{11}	D_{12}	D_{13}	—
PCLK	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_1	C_2	C_3	C_4	C_5	C_6	C_1

25 MHz 2 WS Buffered: 4 Words/6 Clock Cycles → 66 Mbytes/Sec

ADDR	A_{00}	WS	WS	—	—	—	A_{01}	WS	WS	—	—	—	A_{02}	WS
DATA	—	—	—	D_{00}	D_{01}	D_{02}	D_{03}	—	—	D_{10}	D_{11}	D_{12}	D_{13}	—
PCLK	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_1	C_2	C_3	C_4	C_5	C_6	C_1

16 MHz 1 WS Buffered: 4 Words/5 Clock Cycles → 51 Mbytes/Sec

ADDR	A_{00}	WS	—	—	—	A_{01}	WS	—	—	—	A_{02}	WS	
DATA	—	—	D_{00}	D_{01}	D_{02}	D_{03}	—	D_{10}	D_{11}	D_{12}	D_{13}	—	
PCLK	C_1	C_2	C_3	C_4	C_5	C_6	C_1	C_2	C_3	C_4	C_5	C_1	

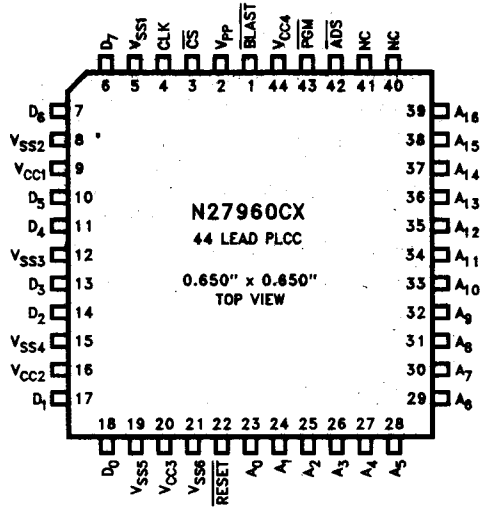

Figure 3. 27960CX 44 Lead PLCC Pinout

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PIN DESCRIPTIONS

Symbol	Pin	Function
A_0–A_{16}	23–39	**ADDRESS INPUTS:** During a burst operation, A_2–A_{16} provides the base address pointing to a block of four consective bytes. A_0 and A_1 select the first byte of the burst access. The 27960CX latches addresses in the first clock cycle. An internal address generator increments addresses A_0 and A_1 for subsequent bytes of the burst.
D_0–D_7	18, 17, 14, 13, 11, 10, 7, 6	**DATA INPUTS/OUTPUTS**
$\overline{ADS}$	42	**ADDRESS STROBE:** Indicates the start of a new bus access. $\overline{ADS}$ is active low in the first clock cycle of a bus access.
$\overline{CS}$	3	**CHIP SELECT:** Master device enable. When asserted (active low) data can be written to and read from the device. In read mode, $\overline{CS}$ enables the state machine and the I/O circuitry. **NOTE:** 1. The address decode path is independent of $\overline{CS}$, i.e., X and Y decoding is always powered up. 2. For programming, $\overline{CS}$ should remain low for the entire cycle. Program and verify functions are done one byte at a time. 3. $\overline{CS}$ going high does not terminate a concurrent burst cycle.
$\overline{BLAST}$	1	**BURST LAST:** Terminates a concurrent burst data cycle at the rising edge of the CLK. It must be asserted by the fourth data byte.
$\overline{RESET}$	22	**RESET:** Resets the state machine into a known state, tri-states the outputs. $\overline{RESET}$ must be asserted for a minimum of 10 clock cycles. At least 5 clock cycles are required after deassertion of $\overline{RESET}$ before beginning the next cycle. $\overline{RESET}$ will abort a concurrent bus cycle.
$\overline{PGM}$	43	**PROGRAM-PULSE CONTROL INPUT**
V_{PP}	2	**PROGRAMMING POWER SUPPLY**
V_{SS}	5, 8, 12, 15, 19, 21	**GROUND**
V_{CC}	9, 16, 20, 44	**SUPPLY VOLTAGE INPUT**

INTERFACE EXAMPLE

Overview

This example illustrates 8-, 16- and 32-bit wide 27960CX interfaces to the 80960CA. The designs offer a simple "no-glue" interface.

A non-buffered 27960CX system organized as 256K x 32 is shown in Figure 4A. Since the 27960CX is capable of driving a 80 pF load, large, non-buffered systems can be implemented by stacking up to 2 banks of 4 EPROMs, resulting in a 256K x 32 memory subsystem. The input capacitive load seen on the address lines (due to the EPROM only) is 24 pF for a 128K x 32 system and 48 pF for a 256K x 32 system. The EPROM is specified at 6 pF for input capacitance (15 pF max) and 12 pF typical for output capacitance. Larger systems can be implemented with buffers (Figure 4B).

Chip Select Logic

High order address lines are decoded to provide $\overline{CS}$. Qualification with other signals is not required. The chip select logic can be implemented with standard asynchronous decoders, PAL's or PLD's (like Intel's 85C508).

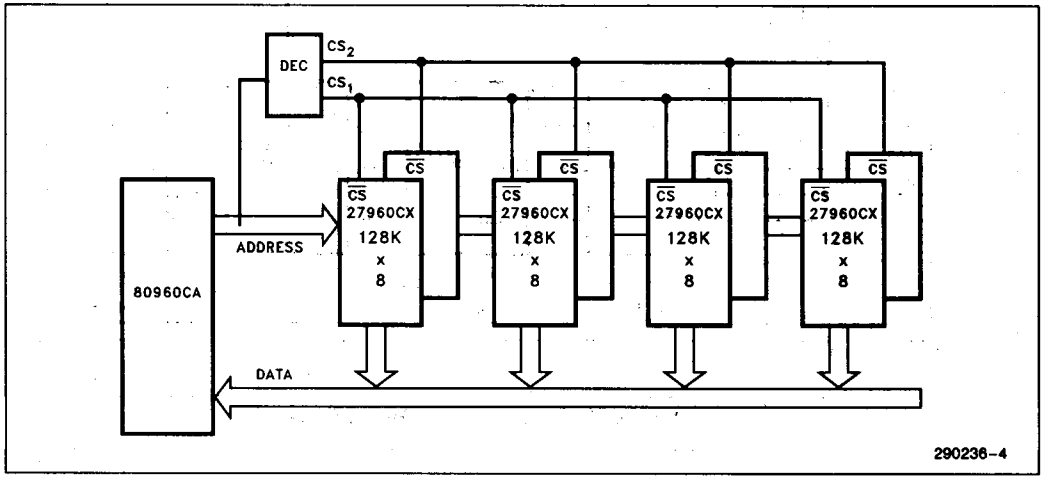


Figure 4A. 256K x 32 Non-Buffered Burst EPROM Memory System

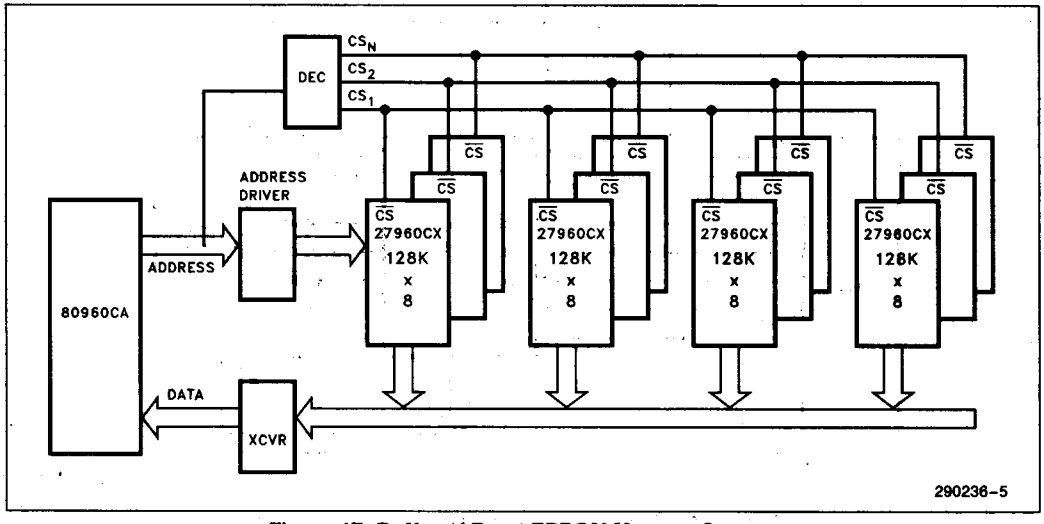


Figure 4B. Buffered Burst EPROM Memory System

Schematics

Figure 5 shows a non-buffered, 128K x 32 27960CX EPROM system.

Chip select logic, the only external logic that is required for this interface, can be derived from the global system chip select circuitry.

In a non-buffered, 16-bit system (Figure 6A) $\overline{BE1}$ and A_2 connect to the lower order address bits of the 27960CX. $\overline{BE1}$ connects to A_0 of both EPROMs, while A_2 connects to both A_1's.

In a non-buffered, 8-bit system (Figure 6B) $\overline{BE0}$ and $\overline{BE1}$ connect to A_0 and A_1 respectively.

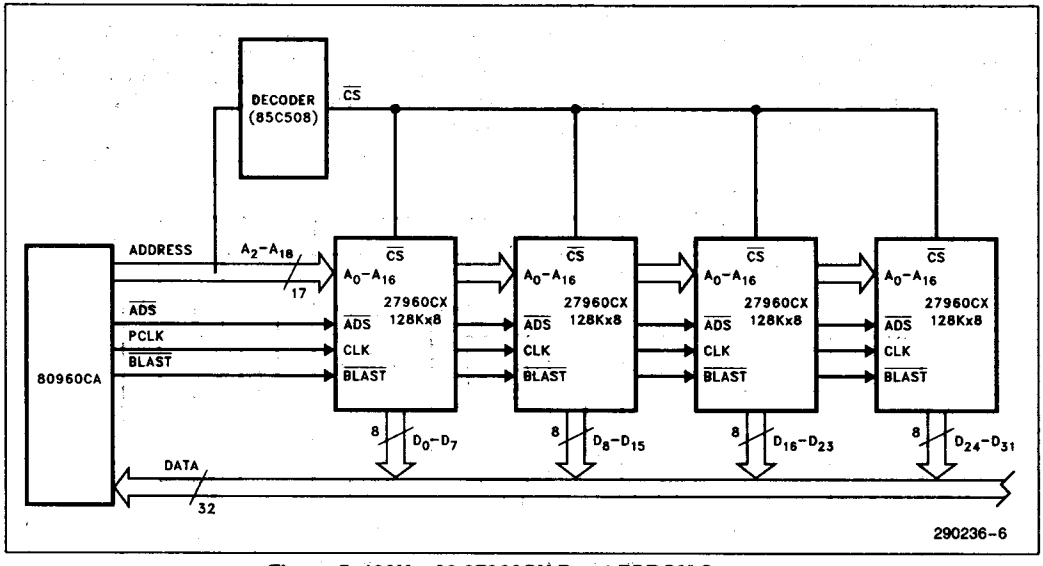


Figure 5. 128K x 32 27960CX Burst EPROM System

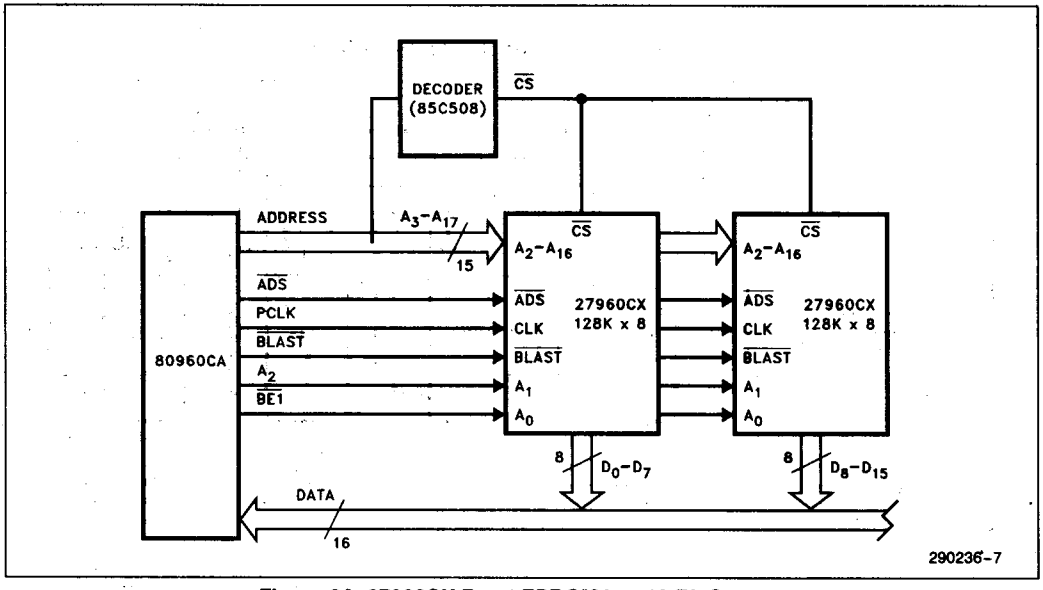


Figure 6A. 27960CX Burst EPROM in a 16-Bit System

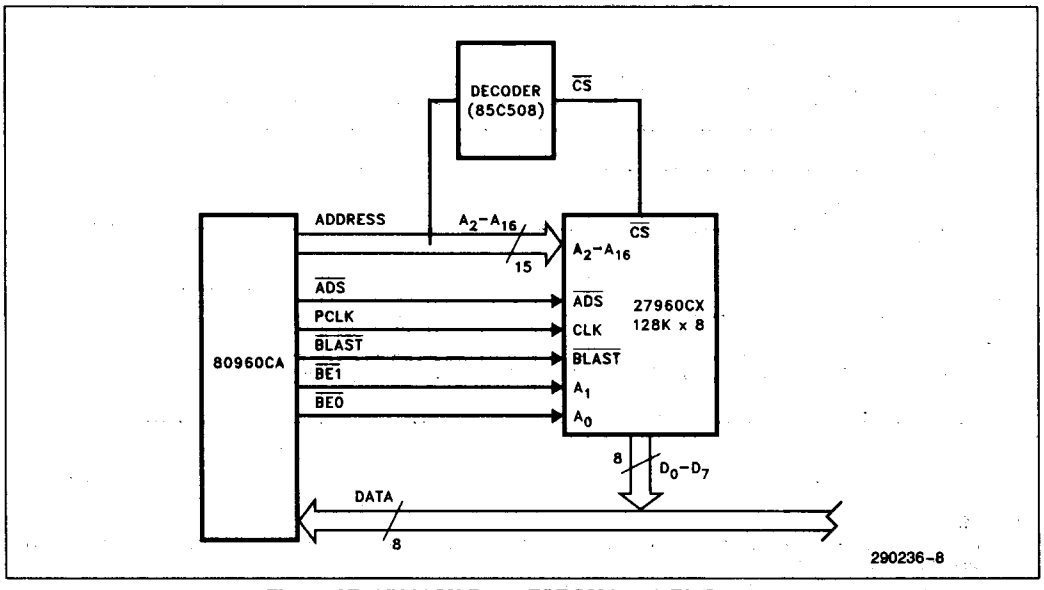


Figure 6B. 27960CX Burst EPROM in a 8-Bit System

Waveforms

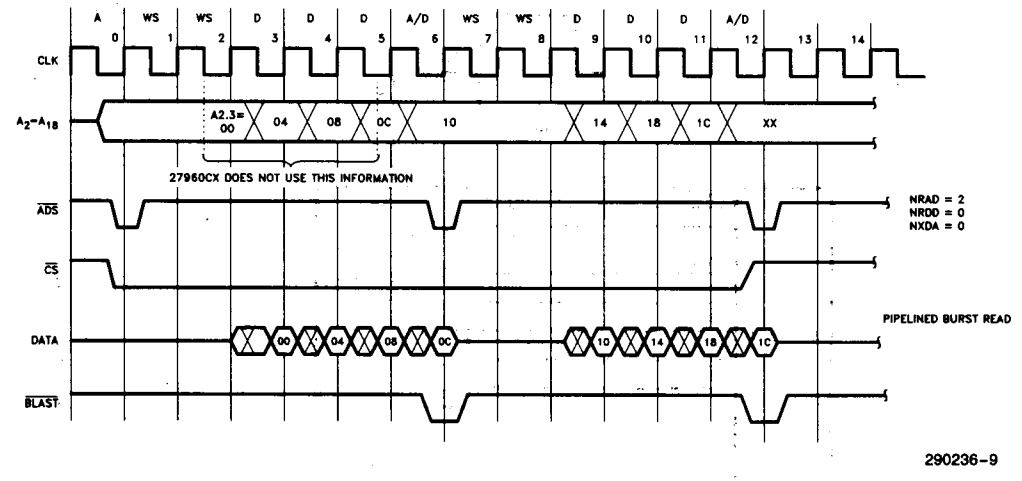
Figure 7 shows the timing waveforms of a 27960CX pipelined read in a 32-bit system.

$\overline{CS}$ Setup Time

$\overline{CS}$ setup time is the time between $\overline{CS}$ being asserted and the first CLK rising edge (during the address cycle). Since a memory access begins on the first CLK rising edge after $\overline{ADS}$ and $\overline{CS}$ are asserted, a minimum $\overline{CS}$ setup time of 7 ns (t_{SVCH}) at 33 MHz is required. With the 80960CA's maximum valid address delay of 14 ns at 33 MHz, 9 ns remains for $\overline{CS}$ decoding logic.

Bootup

The wait state configuration (1 or 2), of the 27960CX is programmed by the user into the 80960CA Region Table parameters of NRAD, NRDD, and NXDA. NRDD is always 0 for the 27960CX.



NOTES:
1. The EPROM can also operate in non pipelined mode i.e, next address and $\overline{ADS}$ can be asserted in the clock cycle following the last data word of the burst.
2. 2 – 0 – 0 – 0 Burst Read → 2 indicates the number of wait states to access the first word
0's indicate the number of wait states for subsequent data words:
0 in this case!

Figure 7. Two Cycles of a 27960CX 2 Wait State 4 Byte Read (2–0–0–0 Burst Read) in a 32 Bit System

During boot-up (Figure 8), the 80960CA picks up it's Region Table data from addresses FFFF FF00; FFFF FF04; FFFF FF08 and FFFF FF0C. Only the least significant byte of each of the above four 32-bit accesses is used to configure the Region Table. For boot-up, the wait-state parameters NRAD and NXDA default to 31 and 3 respectively. During boot-up, the 27960CX will wrap around the first word of the four-word burst and hold the first word until $\overline{BLAST}$ is asserted.

27960CX DEVICE NAMES

The device names on the 27960CX were derived as mnemonics that correspond to the number of wait states and expected operating frequency for the device. For example, the 25 MHz, 2 wait state 27960CX is named 27960C2-25.

AC TIMING DERIVATIONS

The AC timings for the 27960CX were generated specifically to meet the requirements of the 80960CA microprocessor. In each case the applicable 80960CA clock frequency and AC timing were taken together with an address buffer delay (if needed) and a typical 2 ns guardband to generate the 27960CX AC timing. Worst case timings were always assumed. On timings where the EPROM is faster than the microprocessor, we specified the time required by the EPROM and left the excess time as additional system guardband. The example below shows how the 27960C2-33 $tavc_0h$ timing was derived.

@33 MHz the clock cycle is ~30 ns.
t_{OV2} of the 80960CA is 3 ns – 14 ns.
Typical 2 ns guardband.

27960C2-33 $tavc_0h$ = 30 ns – 14 ns – 2 ns
= 14 ns

Decoders are needed for the systems chip select decoding. For the 27960CX timings we assumed a 10 ns chip select decoder for 16 MHz and a 7 ns decoder for 25 MHz and 33 MHz systems. The example below shows how the 27960C2-33 tsvch timing was derived.

@33 MHz the clock cycle is ~30 ns.
t_{OV2} of the 80960CA is 3 ns – 14 ns.
Decoder = 7 ns

27960C2-33 tsvch = 30 ns – 14 ns – 7 ns
= 9 ns

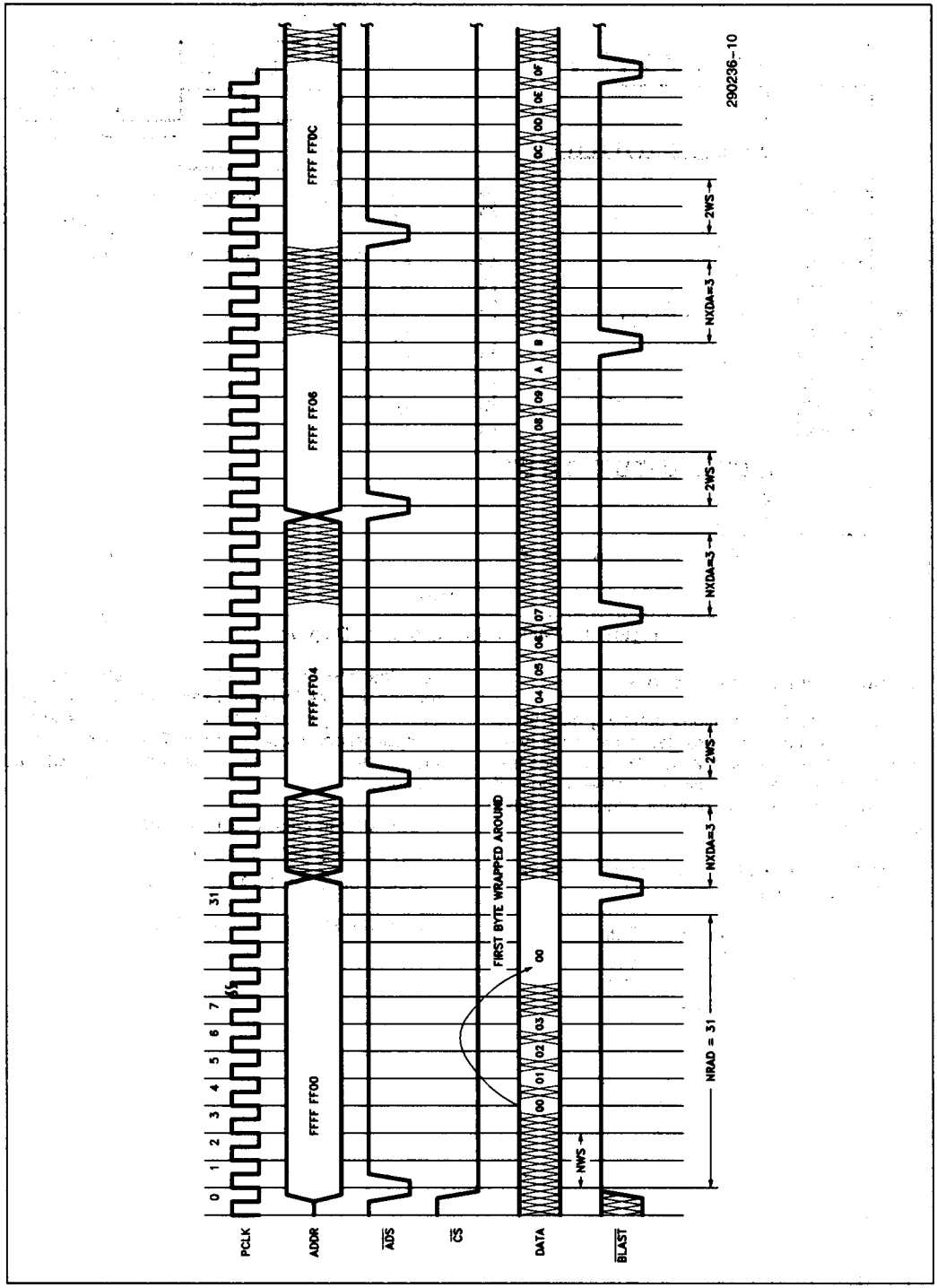


Figure 8. 27960CX/80960CA Bootup Timing

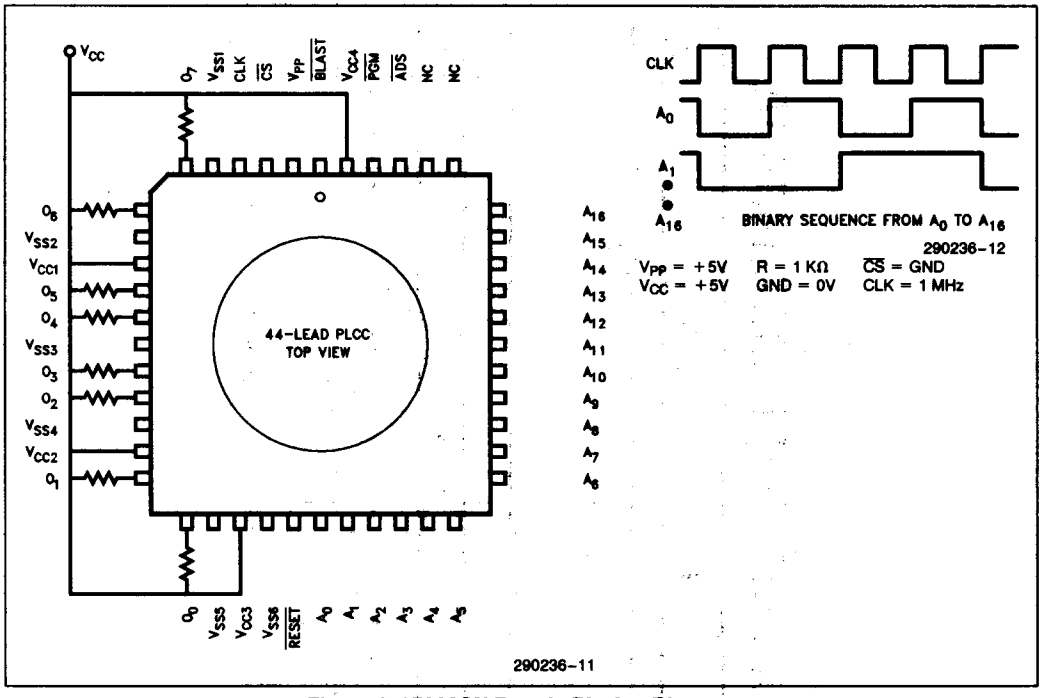


Figure 9. 27960CX Burn In Biasing Diagram

System Buffering Considerations

For large system applications buffering may be required between the microprocessor and memory devices. The 25 and 16 MHz 27960CX AC timings take this into account. For applications not requiring buffering these devices will provide additional system guardband.

The list below shows the buffers used in generating the 27960CX timings:

	Input Buffer	Output Buffer
25 MHz	8 ns	5 ns
16 MHz	10 ns	7 ns

Note that the 25 MHz buffers are slightly faster in keeping with the increased sensitivity for higher performance. Significantly faster buffers are available for applications requiring them. The example below shows the tchqv timing analysis for a buffered 27960C2-25.

@25 MHz the clock cycle is ~40 ns.

t_{IH1} of the 80960CA is 5 ns.

Output buffer for 25 MHz = 5 ns

27960C2-25 t_{CHQV} = 40 ns − 5 ns − 5 ns
= 30 ns

ABSOLUTE MAXIMUM RATINGS*

Read Operating Temperature . . . . . 0°C to +70°C(8)
Case Temperature Under Bias . . −10°C to +80°C(8)
Storage Temperature . . . . . −65°C to +125°C
All Input or Output Voltages with Respect to Ground . . . . . −0.6V to +6.5V(4)
Voltage on A_9 with Respect to Ground . . . . . −0.6V to +13.0V(4)
V_{PP} Supply Voltage with Respect to Ground . . . . . −0.6V to +14.0V(4)
V_{CC} Supply Voltage with Respect to Ground . . . . . −0.6V to +7.0V(4)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

DC CHARACTERISTICS $0°C < T_A +70°C, V_{CC} = 5V \pm 10\%$, TTL Inputs

Symbol	Parameter		Notes	Min	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current				10	µA	$V_{OUT} = 5.5V$
I_{PP}	V_{PP} Load Current Read				10	µA	$V_{PP} = 0$ to V_{CC}, $\overline{PGM} = V_{IH}$
I_{SB}	V_{CC} Standby	Switching	2		45	mA	$\overline{CS} = V_{IH}$, f = 33 MHz
		Stable	2		30	mA	$\overline{CS} = V_{IH}$
I_{CC}	V_{CC} Active Current		1, 3, 7		125	mA	$\overline{CS} = V_{IL}$, f = 33 MHz, $I_{OUT} = 0$ mA
V_{IL}	Input Low Voltage		4	−0.5	0.8	V	
V_{IH}	Input High Voltage			2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		5	$V_{CC} - 0.8$		V	$I_{OH} = -100$ µA
			5	2.4		V	$I_{OH} = -400$ µA
I_{OS}	Output Short Circuit		6		100	mA	

NOTES:
1. Maximum current is with outputs unloaded.
2. I_{CC} standby current assumes no output loading i.e., $I_{OH} = I_{OL} = 0$ mA.
3. I_{CC} is the sum of current through $V_{CC3} + V_{CC4}$ and does not include the current through V_{CC1} and V_{CC2}. (V_{CC1} and V_{CC2} supply power to the output drivers. V_{CC3} and V_{CC4} supply power to the reset of the device.)
4. Minimum DC input voltage on input and output pins is −0.5V. During transitions, this level may undershoot to −2.0V for periods less than 20 ns.
5. Maximum DC voltage on input and output pins is $V_{CC} + 0.5V$ which may overshoot to $V_{CC} + 2.0V$ for periods less than 20 ns.
6. One output shorted for no more than one second. I_{OS} is sampled but not 100% tested.
7. I_{CC} max measured with a 10.11 µF capacitor between V_{CC} and V_{SS}.
8. This specification defines commercial product operating temperatures.

4

EXPLANATION OF AC SYMBOLS

The nomenclature used for timing parameters are as per IEEE STD 662-1980 IEEE Standard Terminology for Semiconductor Memory.

Each timing symbol has five characters. The first is always a "t" (for time). The second character represents a signal name. e.g., (CLK, $\overline{ADS}$, etc.). The third character represents the signal's level (high or low) for the signal indicated by the second character. The fourth character represents a signal name at which a transition occurs marking the end of the time interval being specified.

The fifth character represents the signal level indicated for the fourth character. The list below shows character representations.

A:	Address	R:	$\overline{Reset}$
B:	$\overline{BLAST}$	Q:	Data
C:	Clock	S:	$\overline{CS}$
H:	Logic High Level	t:	Time
L:	$\overline{ADS}$/Logic Low Level	V:	Valid
P:	V_{PP} Programming Voltage	Z:	Tri-state Level
X:	No longer a valid "driven" logic level		

AC CHARACTERISTICS: READ OPERATION $0°C < T_A < +70°C, V_{CC} = 5V \pm 10\%$

Versions				27960C2-33 33 MHz 2 Wait State		27960C2-25 25 MHz 2 Wait State		27960C1-16 16 MHz 1 Wait State		Unit
No.	**Symbol**	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
1	t_{AVC_0H}	Address Valid to CLK High	CLK_0	12		10		22		ns
2	t_{C_NHAX}	CLK High to Address Invalid	2	0		0		0		ns
3	t_{LLCH}	$\overline{ADS}$ low to CLK High	CLK_0	8		8		22		ns
4	t_{CHLH}	CLK high to $\overline{ADS}$ High	5	6	22	6	32	6	40	ns
5	t_{SVCH}	$\overline{CS}$ Valid to CLK High	1	7		7		14		ns
6	t_{C_NHSX}	CLK High to $\overline{CS}$ Invalid	2	0		0		0		ns
7	t_{CHQV}	CLK High to Data Valid	7		27		30		40	ns
8	t_{CHQX}	CLK High to Data Invalid		5		5		5		ns
9	t_{CHQZ}	CLK High to Data High Z	6		25		30		30	ns
10	t_{BVCH}	$\overline{BLAST}$ Valid to CLK High		8		8		22		ns
11	t_{CHBX}	CLK High to $\overline{BLAST}$ Invalid	3	5	22	5	32	5	40	ns

NOTES:
1. Valid signal level is meant to be either a logic high or logic low.
2. The subscript N represents the number of wait states for this parameter. $\overline{CS}$ can be de-asserted (high) after the number of wait states (N) has expired and the EPROM will continue to burst out data for the current cycle.
3. BLAST# must be returned high before the next rising clock edge.
4. The sum of t_{CHQV} + t_{AVCH} + N_{CLK} will not equal actual t_{AVQV} if independent test conditions are used to obtain t_{AVCH} and t_{CHQV} (N = number of wait states).
5. $\overline{ADS}$ must be returned high before the next rising clock edge.
6. Sampled, not 100% tested. The transition is measured ±500 mV from steady state voltage.
7. For capacitive loads above 80 pF, t_{CHQV} can be derated by 1 ns/20 pF.

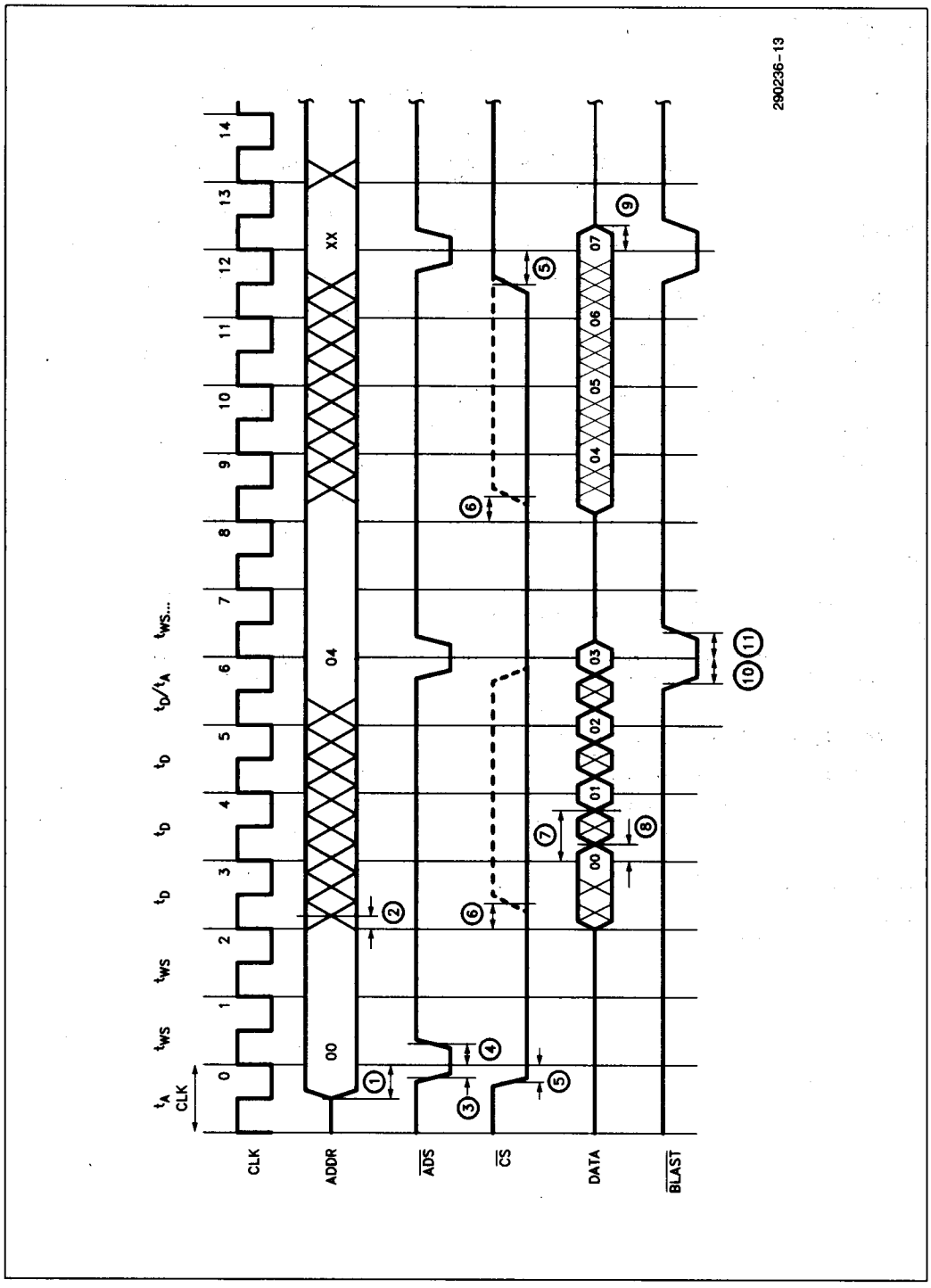


Figure 10. 27960CX Pipelined 2 Wait State AC Waveforms

AC CONDITIONS OF TEST

Input Rise and Fall Times
(10% to 90%) ..... 4 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level 1.5V
Output Timing Reference Level 1.5V

Table 2. Mode Table

Mode	$\overline{CS}$	$\overline{PGM}$	$\overline{BLAST}$	$\overline{ADS}$	$\overline{RESET}$	A_9	V_{PP}	V_{CC}	OUTPUT
Read	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	X	V_{CC}	V_{CC}	D_{OUT}
Standby(6)	V_{IH}	X	X	X	V_{IH}	X	V_{CC} (5)	V_{CC}	High Z
Program	V_{IL}	V_{IL}	V_{IH}	V_{IH}(2)	V_{IH}	X	(3)	(3)	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}	V_{IH}	X	(3)	(3)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	V_{IH}	X	(3)	(3)	High Z
ID Byte 0: Manufacturer	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	89H
ID Byte 1: Part (27960)	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	E0H
ID Byte 2: CX	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	01B
ID Byte 3: 1 Wait State 2 Wait States	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	01B 10B
Reset	X	X	X	X	V_{IL}	X	V_{CC}	V_{CC}	High Z

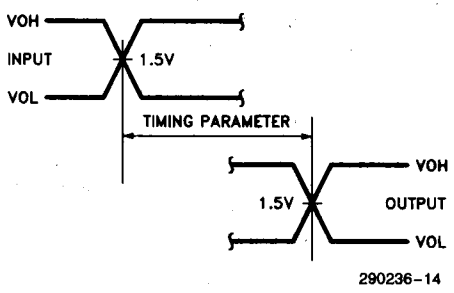
NOTES:
1. V_{IH} until data terminated at which time $\overline{BLAST}$ must go to V_{IL}.
2. Need to toggle from V_{IH} to V_{IL} to V_{IH}.
3. See DC Programming Characteristics for V_{CC}, V_{ID} and V_{PP} voltages.
4. X can be V_{IL} or V_{IH}.
5. $V_{PP} = V_{CC}$ to meet standy current specification. $V_{CC} > V_{PP} > V_{IL}$ will cause a slight increase in standby current.
6. The device must be in the idle state (by asserting $\overline{RESET}$ or using $\overline{BLAST}$) before going into standby.

CAPACITANCE(1) $T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	12	15	pF	$V_{OUT} = 0V$
C_{VPP}	V_{PP} Capacitance	40	45	pF	$V_{IN} = 0V$

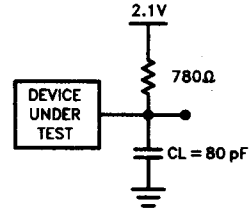
NOTE:
1. Sampled. Not 100% tested.

AC INPUT/OUTPUT REFERENCE WAVEFORMS



Input and output timings are measured from 1.5V. Timing values are specified assuming maximum input and output rise and fall time = 4 ns.

AC TESTING LOAD CIRCUIT

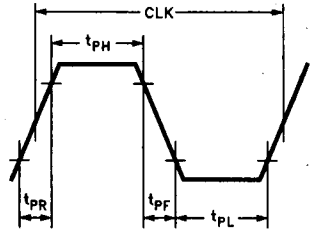


CL includes jig capacitance
For t_{CHQZ} C_L = 5 pF and R_L = 405Ω

CLOCK CHARACTERISTICS

Versions		33 MHz		25 MHz		20 MHz		16 MHz		Units
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
CLK	Period	30.3		40		50		62.5		ns
t_{PR}	Rise Time	1	4	1	4	1	4	1	4	ns
t_{PF}	Fall Time	1	4	1	4	1	4	1	4	ns
t_{PL}	Low Time	(t/2) − 2	t/2	(t/2) − 3	t/2	(t/2) − 4	t/2	(t/2) − 4	t/2	ns
t_{PH}	High Time	(t/2) − 2	t/2	(t/2) − 3	t/2	(t/2) − 4	t/2	(t/2) − 4	t/2	ns
Max Rise Time for Programming CLK = 100 ns										

CLOCK WAVEFORM



Program/Program Verify

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" can be programmed, both "1's" and "0's" can be present in the data word. Ultraviolet erasure is the only way to change "0's" to "1's".

Programming mode is entered when V_{PP} is raised to 12.75V. Program/Verify operation is synchronous with the clock and can only be initiated following an idle state. Program and Program Verify take place in 3 clock cycles. In the first clock cycle, addresses and data are input and programming occurs. Program Verify follows in the second clock cycle and the third clock cycle terminates synchronous Program/Verify operation, returning the state machine to the idle state with outputs at high impedance.

As in the Read mode, A_2–A_{16} point to a four byte block in the memory array. During programming, the internal address increment circuitry is disabled and the programmer must supply A_0 and A_1 to point to an individual byte within the four byte block that is to be programmed. Only one byte is programmed in each 3 cycle Program/Verify sequence.

Program Inhibit

The Program Inhibit mode allows parallel programming and verification of multiple devices with different data. With V_{PP} at 12.75V, a Program/Verify sequence is initiated for any device that receives a valid $\overline{ADS}$ pulse and rising clock edge while $\overline{CS}$ is asserted. A $\overline{PGM}$ pulse programs data in the first cycle of the sequence and data for Program Verify is output in the second cycle. The Program/Verify sequence is inhibited on any devices for which $\overline{CS}$ is not asserted. Data will not be programmed and the outputs will remain in their high impedance state.

int$_e$ligent Identifier™ Mode

The device's manufacturer, product type, and configuration are stored in a four byte block that can be accessed by using the int$_e$ligent Identifier™ mode.

The programmer can verify the device identifier and choose the programming algorithm that corresponds to the Intel 27960CX. The int$_e$ligent Identifier can also be used to verify that the product is configured with the desired Read mode options for wait states.

int$_e$ligent Identifier mode is entered when A_9 (pin 32) is raised to its high voltage (V_{ID}) level. The internal state machine is then set for int$_e$lligent Identifier Read operation. Reading the identifier is similar to a Read operation on a one wait state configured product. Up to four bytes can be read in a single burst access. int$_e$ligent Identifier read is terminated by a synchronous $\overline{BLAST}$ input, returning the state machine to the idle state with outputs at high impedance.

The four byte block code for the int$_e$ligent Identifier code is located at address 00H through 03H and is encoded as follows:

MEANING	(A1, A0)	DATA
Intel ID	Byte 00	89h
27960	Byte 01	E0h
CX	Byte 10	01b
1 Wait State	Byte 11	01b
2 Wait States	Byte 11	10b

RESET MODE

Due to the synchronous nature of the 27960CX, the various operating modes must be initiated from a known idle state. During normal operation, the internal state machine returns to an idle state at the termination of a bus access (after $\overline{BLAST}$ is asserted).

During initial device power up, the state machine is in an indeterminant state. The reset mode is provided to force operation into the idle state. Reset mode is entered when the $\overline{RESET}$ pin is asserted. Output pins are asynchronously set to the high impedance state and address latches are put into the flow through mode. A reset is successfully completed and the state machine set in an idle state when $\overline{RESET}$ has been asserted for a minimum of 10 clock cycles and deasserted for five clock cycles.

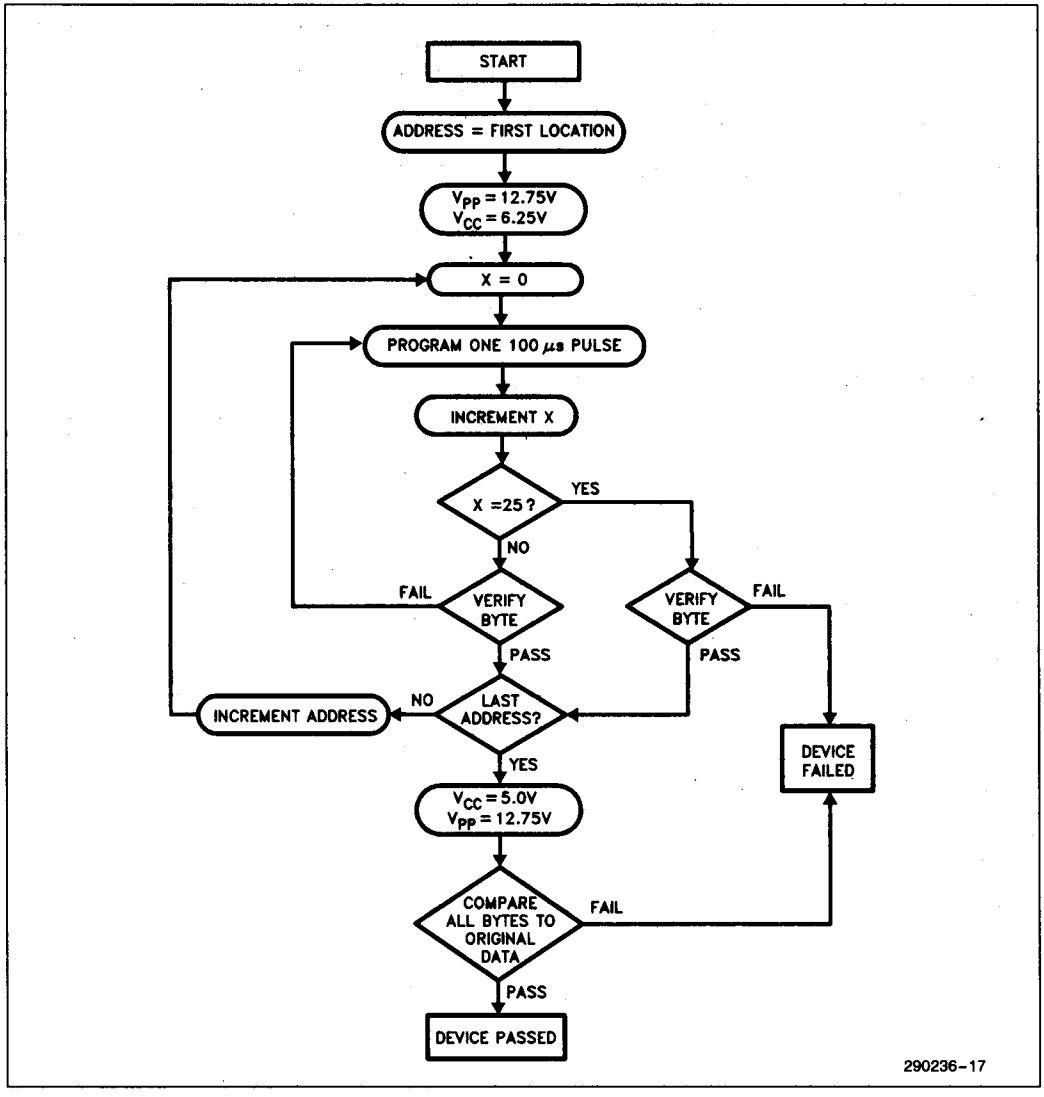


Figure 11. Quick-Pulse Programming™ Algorithm

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm programs Intel's 27960CX. Developed to substantially reduce programming throughput time, this algorithm allows optimized equipment to program a 27960CX in under 17 seconds. Actual programming time depends on the programmer used.

The Quick-Pulse Programming algorithm uses a 100 μs pulse followed by a byte verification to determine when the addressed byte is correctly programmed. The algorithm terminates if 25 100 μs pulses fail to program a byte. Figure 11 shows the 27960CX Quick-Pulse Programming algorithm flowchart.

The entire program-pulse/byte-verify sequence is performed with V_{CC} = 6.25V and V_{PP} = 12.75V. The program equipment must establish V_{CC} before applying voltages to any other pins. When programming is complete, all bytes should be compared to the original data with V_{CC} = 5.0V and V_{PP} = 12.75V.

D.C. PROGRAMMING CHARACTERISTICS T_A = 25° ±5°C

Symbol	Parameter	Notes	Min	Max	Unit	Condition
I_{LI}	Input Load Current			10	μA	$V_{IN} = V_{IH}$ or V_{IL}
I_{CC}	V_{CC} Program Current	1		125	mA	$\overline{CS} = V_{IL}$
I_{PP}	V_{PP} Program Current	1		50	mA	$\overline{CS} = V_{IL}$
V_{IL}	Input Low Voltage		−0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage(Verify)			0.40	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage(Verify)		V_{CC} − 0.8		V	I_{OH} = −400 μA
V_{ID}	A_9 int$_e$ligent Identifier Voltage		11.5	12.5	V	
V_{CC}	Supply Voltage (Program)	2	6.0	6.5	V	
V_{PP}	Program Voltage	2	12.5	13.0	V	

NOTES:
1. The maximium current value is with outputs unloaded.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. During programming clock levels are V_{IH} and V_{IL}.

A.C. PROGRAMMING, RESET AND ID CHARACTERISTICS $T_A = 25°C \pm 5°C$

No.	Symbol	Parameter	Notes	Min	Max	Unit
1	t_{AVPL}	Address Valid to $\overline{PGM}$ Low		2		µs
2	t_{CHAX}	CLK High to Address Invalid		50		ns
3	t_{LLCH}	$\overline{ADS}$ Low to CLK High	1	50		ns
4	t_{CHLH}	CLK High to $\overline{ADS}$ High	2	50		ns
5	t_{SVCH}	$\overline{CS}$ Valid to CLK High		50		ns
6	t_{CHSX}	CLK High to $\overline{CS}$ Invalid	3			ns
7	t_{CHQV}	CLK High to D_{OUT} Valid		100		ns
8	t_{CHQX}	CLK High to D_{OUT} Invalid		0		ns
9	t_{BVCH}	$\overline{BLAST}$ Valid to CLK High		50		ns
10	t_{CHBX}	CLK High to $\overline{BLAST}$ Invalid	4	50		ns
11	t_{QVPL}	DATA Valid to $\overline{PGM}$ Low		2		µs
12	t_{PLPH}	$\overline{PGM}$ Program Pulse Width		95	105	µs
13	t_{PHQX}	$\overline{PGM}$ High to D_{IN} Invalid		2		µs
14	t_{CLPL}	CLK Low to $\overline{PGM}$ Low		50		ns
15	t_{QZCH}	D_{IN} Tri-State to CLK High		2		µs
16	t_{VCS}	V_{CC} Program Voltage to CLK High	7	2		µs
17	t_{VPS}	V_{PP} Program Voltage to CLK High	7	2		µs
18	t_{A_9HCH}	A_9 V_{ID} Voltage to CLK High		2		µs
19	t_{CHA_9X}	CLK High to A_9 Not V_{ID} Voltage		2		µs
20	t_{RVCH}	$\overline{RESET}$ Valid to CLK High	6	50		ns
21	t_{CHCL}	CLK High to CLK Low	5	100		ns
22	t_{CLCH}	CLK Low to CLK High	5	100		ns

NOTES:
1. If $\overline{CS}$ is low, $\overline{ADS}$ can go low no sooner than the falling edge of the previous CLK.
2. $\overline{ADS}$ must return high prior to the next rising edge of clock.
3. $\overline{CS}$ must remain low until after the rising edge of CLK1.
4. $\overline{BLAST}$ must return high prior to the next rising edge of CLK.
5. Max CLK rise/fall time is 100 ns.
6. $\overline{RESET}$ must be low for 10 clock cycles and high for 5 clock cycles.
7. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

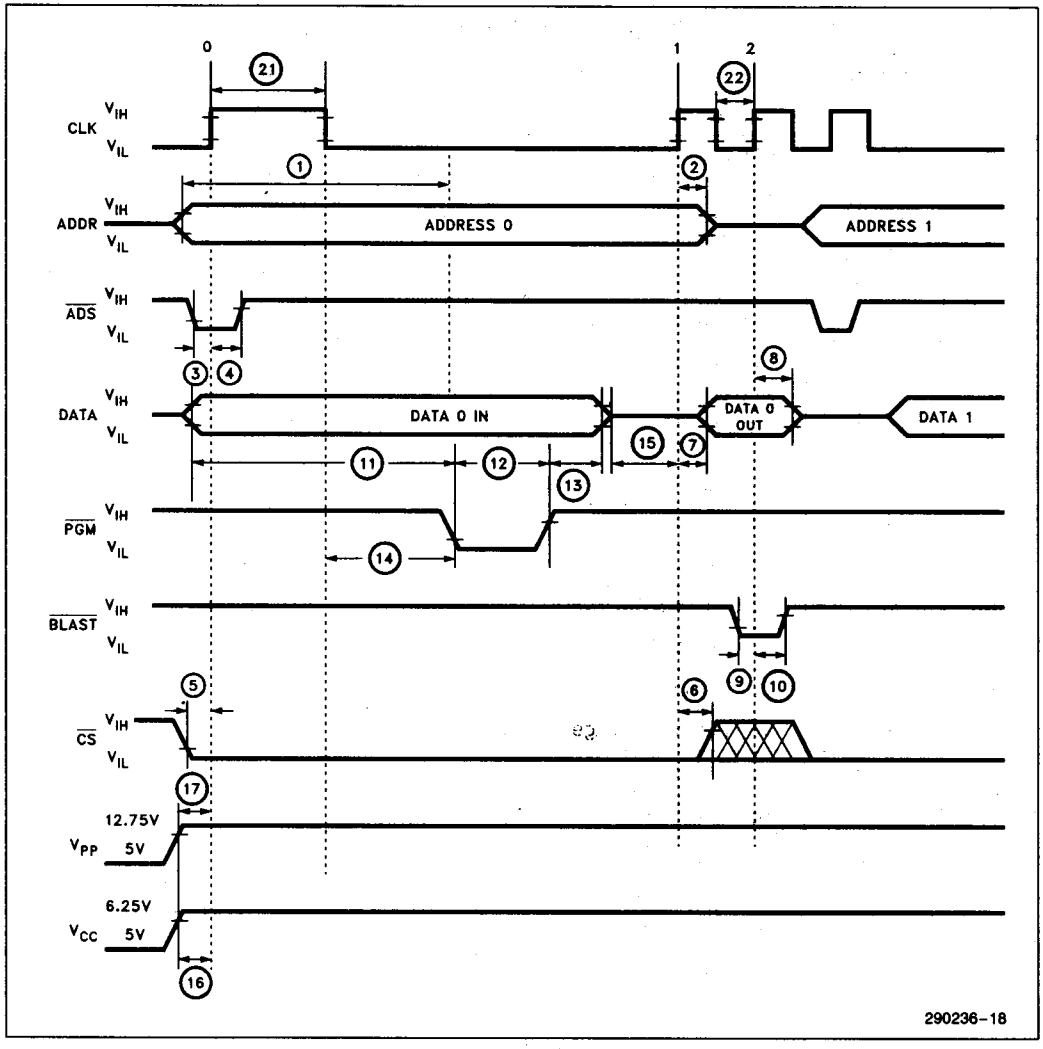


Figure 12. 27960CX Programming Waveforms

RESET and Intelligent Identifier Waveforms

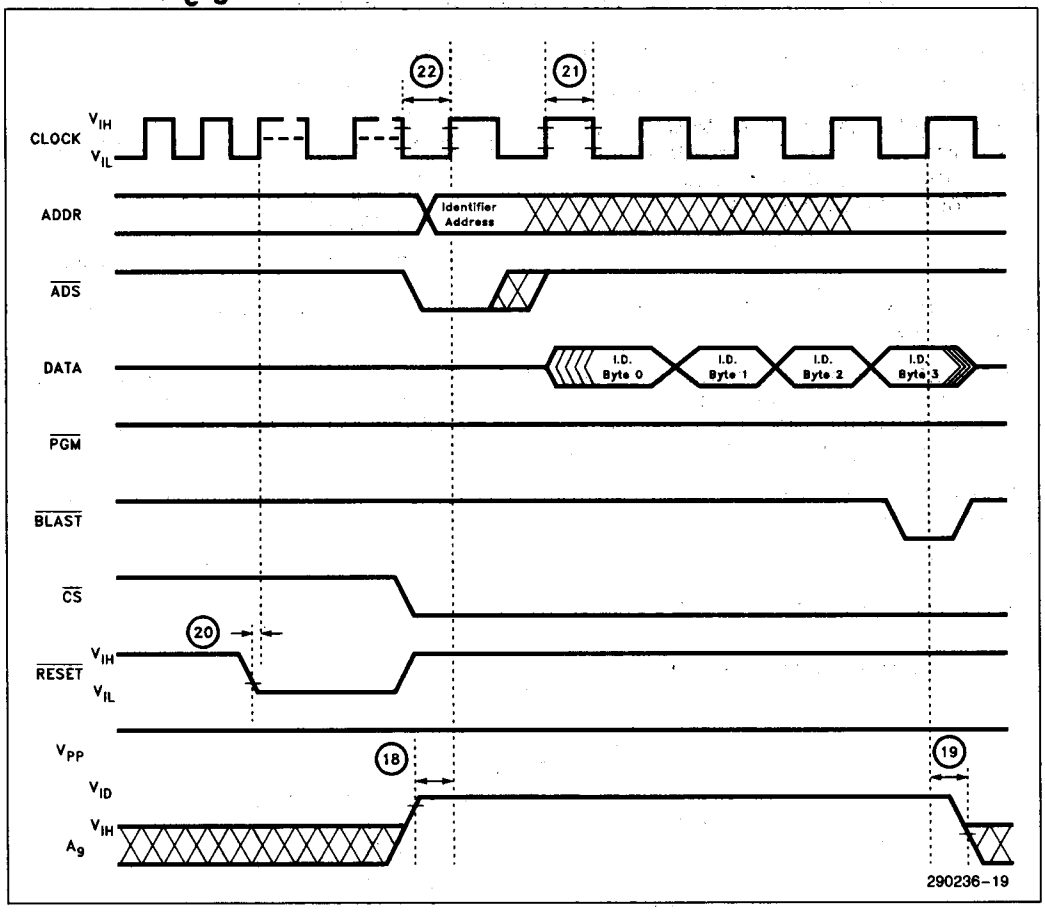


Figure 13. 27960CX RESET and ID Waveforms

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