# SRAM

# 16K x 4 SRAM

CACHE-TAG



## FEATURES

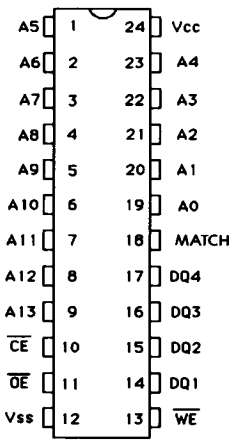
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast match time: 15ns

## OPTIONS

| | MARKING |
|---|---|
| • Timing | |
| 12ns access | -12 |
| 15ns access | -15 |
| 20ns access | -20 |
| 25ns access | -25 |
| 30ns access | -30 |
| 35ns access | -35 |
| • Packages | |
| Plastic DIP (300 mil) | None |
| Ceramic DIP (300 mil) | C |
| Plastic SOJ (300 mil) | DJ |
| Ceramic LCC | EC |

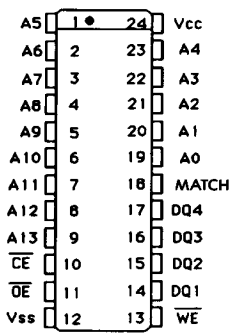
## PIN ASSIGNMENT (Top View)

**24L/300 DIP**



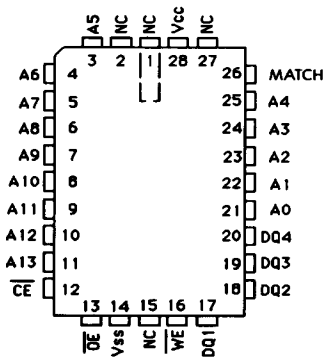

PG, CF

**24L/300 SOJ**




DJB

**28L/LCC**

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## GENERAL DESCRIPTION

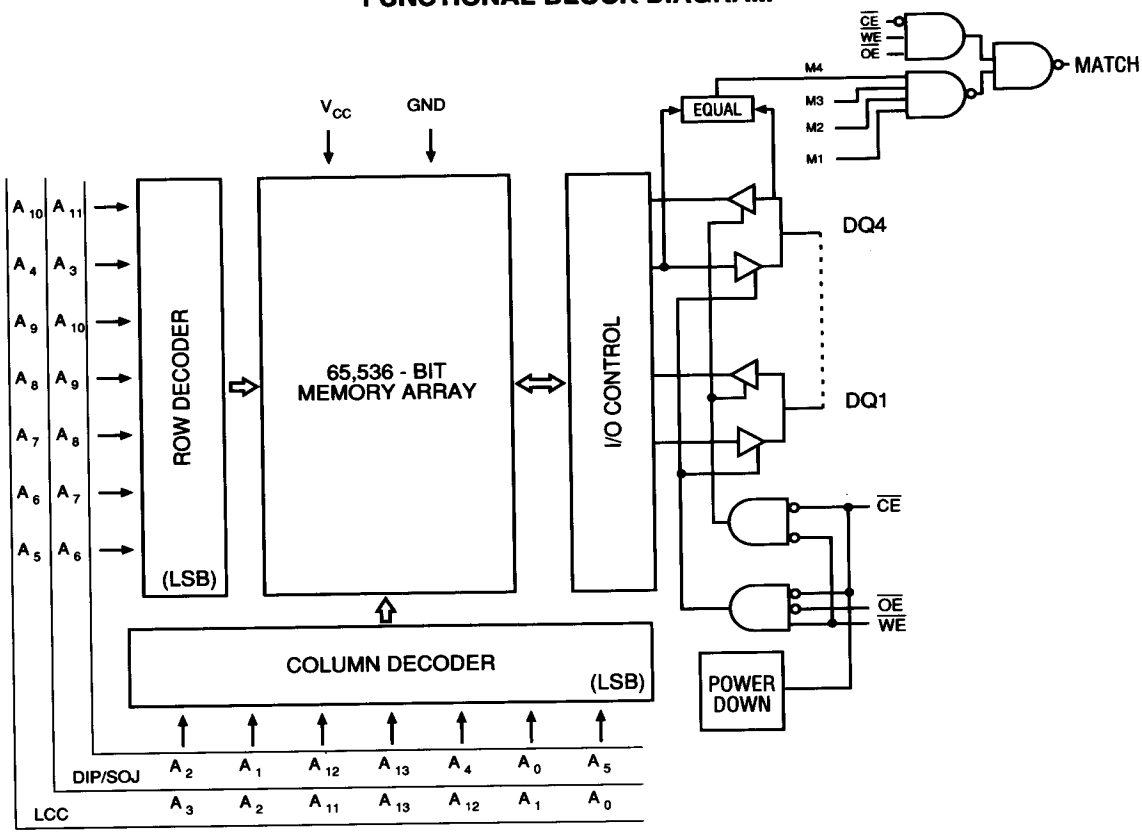
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable $\overline{CE}$ on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

## FUNCTIONAL BLOCK DIAGRAM




## TRUTH TABLE

| MODE | $\overline{OE}$ | $\overline{CE}$ | $\overline{WE}$ | DQ | POWER | MATCH |
|---|---|---|---|---|---|---|
| STANDBY | X | H | X | HIGH Z | STANDBY | HIGH |
| READ | L | L | H | DOUT | ACTIVE | HIGH |
| READ | H | L | H | HIGH Z | ACTIVE | ACTIVE |
| WRITE | X | L | L | DIN | ACTIVE | HIGH |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, Vcc = 5.0V ± 10%)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | | VIH | 2.2 | Vcc +1 | V | 1 |
| Input Low (Logic 0) Voltage | | VIL | -0.5 | 0.8 | V | 1, 2 |
| Input Leakage Current | 0V ≤ VIN ≤ Vcc | ILI | -10 | 10 | µA | |
| Output Leakage Current | Output(s) Disabled, 0V ≤ VOUT ≤ Vcc | ILO | -10 | 10 | µA | |
| Output High Voltage | IOH = -4.0mA | VOH | 2.4 | | V | 1 |
| Output Low Voltage | IOL = 8.0mA | VOL | | 0.4 | V | 1 |

| DESCRIPTION | CONDITIONS | SYMBOL | -12 | -15 | -20 | -25 | -30 | -35 | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Current: Operating | $\overline{CE}$ ≤ VIL, Vcc = Max., Outputs Open | Icc | 140 | 130 | 120 | 110 | 100 | 100 | mA | 3 |
| Power Supply Current: Standby | $\overline{CE}$ ≥ VIH, Vcc = Max | ISB1 | 60 | 50 | 45 | 40 | 40 | 40 | mA | |
| | $\overline{CE}$ ≥ Vcc - 0.2, Vcc = Max. VIL ≤ Vss + 0.2 VIH ≥ Vcc - 0.2, f = 0 | ISB2 | 5 | 5 | 5 | 5 | 5 | 5 | mA | |

## CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $T_A$ = 25°C, f = 1MHz | CI | | 7 | pF | 4 |
| Output Capacitance | Vcc = 5V | CO | | 7 | pF | 4 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$)

| DESCRIPTION | | -12 | | -15 | | -20 | | -25 | | -30 | | -35 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYM | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| **READ Cycle** | | | | | | | | | | | | | | | |
| READ cycle time | $t_{RC}$ | 12 | | 15 | | 20 | | 25 | | 30 | | 35 | | ns | |
| Address access time | $t_{AA}$ | | 12 | | 15 | | 20 | | 25 | | 30 | | 35 | ns | |
| Chip enable access time | $t_{ACE}$ | | 12 | | 15 | | 20 | | 25 | | 30 | | 35 | ns | |
| Output hold from access change | $t_{OH}$ | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns | |
| Chip enable to output in low Z | $t_{LZCE}$ | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns | |
| Chip disable to output in high Z | $t_{HZCE}$ | | 10 | | 10 | | 15 | | 15 | | 20 | | 20 | ns | 6,7 |
| Chip enable to power up time | $t_{PU}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Chip disable to power down time | $t_{PD}$ | | 12 | | 15 | | 20 | | 25 | | 30 | | 35 | ns | |
| Output enable access time | $t_{AOE}$ | | 10 | | 12 | | 15 | | 15 | | 20 | | 20 | ns | |
| Output enable to output in low Z | $t_{LZOE}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Output disable to output in high Z | $t_{HZOE}$ | | 10 | | 10 | | 15 | | 15 | | 20 | | 20 | ns | 6 |
| **WRITE Cycle** | | | | | | | | | | | | | | | |
| WRITE cycle time | $t_{WC}$ | 12 | | 15 | | 20 | | 25 | | 30 | | 35 | | ns | |
| Chip enable to end of write | $t_{CW}$ | 10 | | 12 | | 15 | | 20 | | 25 | | 30 | | ns | |
| Address valid to end of write | $t_{AW}$ | 12 | | 15 | | 15 | | 20 | | 25 | | 30 | | ns | |
| Address set-up time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Address hold from end of write | $t_{AH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Write pulse width | $t_{WP}$ | 10 | | 12 | | 15 | | 20 | | 25 | | 25 | | ns | |
| Data set-up time | $t_{DS}$ | 10 | | 10 | | 12 | | 15 | | 15 | | 15 | | ns | |
| Data hold time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Write disable to output in low Z | $t_{LZWE}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Write enable to output in high Z | $t_{HZWE}$ | 0 | 10 | 0 | 10 | 0 | 12 | 0 | 15 | 0 | 15 | 0 | 15 | ns | 6 |

## AC TEST CONDITIONS

| | |
|---|---|
| Input pulse levels | Vss to 3.0V |
| Input rise and fall times | 5ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See figures 1 and 2 |

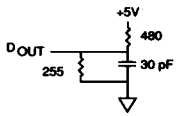



Fig. 1 OUTPUT LOAD EQUIVALENT

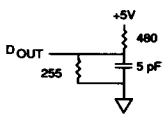



Fig. 2 OUTPUT LOAD EQUIVALENT

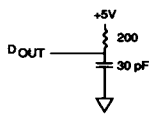
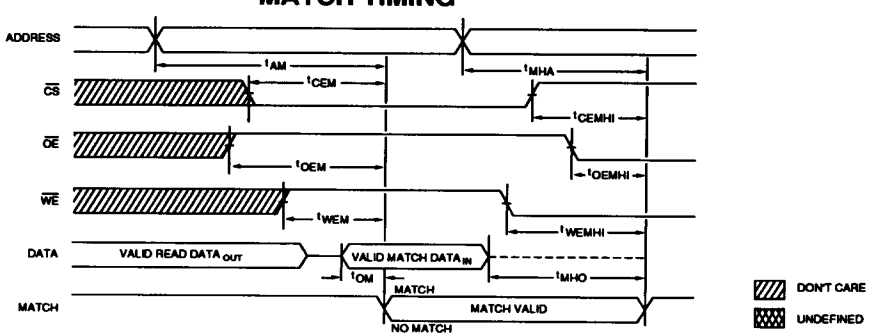



Fig. 3 OUTPUT LOAD EQUIVALENT

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

| DESCRIPTION | | -12 | | -15 | | -20 | | -25 | | -30 | | -35 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYM | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| **MATCH cycle** | | | | | | | | | | | | | | | |
| Address to MATCH valid | $t_{AM}$ | | 15 | | 17 | | 22 | | 25 | | 30 | | 35 | ns | 12 |
| MATCH hold from address | $t_{MHA}$ | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns | 12 |
| $\overline{CE}$ to MATCH | $t_{CEM}$ | | 10 | | 12 | | 15 | | 20 | | 20 | | 20 | ns | 12 |
| $\overline{CE}$ to MATCH high | $t_{CEMhi}$ | | 10 | | 12 | | 15 | | 20 | | 20 | | 20 | ns | 12 |
| $\overline{OE}$ to MATCH valid | $t_{OEM}$ | | 10 | | 12 | | 15 | | 20 | | 20 | | 25 | ns | 12 |
| $\overline{OE}$ to MATCH high | $t_{OEMhi}$ | | 10 | | 12 | | 15 | | 20 | | 20 | | 25 | ns | 12 |
| $\overline{WE}$ to MATCH valid | $t_{WEM}$ | | 10 | | 12 | | 15 | | 20 | | 20 | | 25 | ns | 12 |
| $\overline{WE}$ to MATCH high | $t_{WEMhi}$ | | 10 | | 12 | | 15 | | 20 | | 20 | | 25 | ns | 12 |
| Data input to MATCH valid | $t_{DM}$ | | 10 | | 12 | | 15 | | 20 | | 20 | | 25 | ns | 12 |
| MATCH hold from data | $t_{MHD}$ | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns | 12 |

### MATCH TIMING

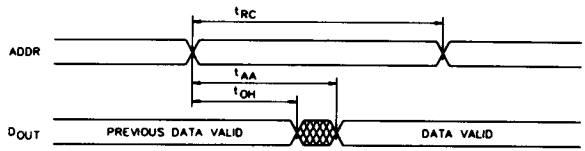



FAST SRAM

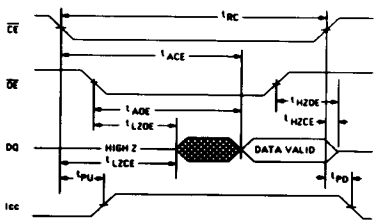
## NOTES

1. All voltages referenced to $V_{SS}$ (GND).
2. -3.0V for pulse width < 20ns.
3. $I_{CC}$ is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. $^{t}HZCE$, $^{t}HZWE$ and $^{t}HZOE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$.
8. $\overline{WE}$ is high for READ cycle.
9. Device is continuously selected. All Chip Enables held in their active state.
10. Address valid prior to or coincident with latest occurring Chip Enable.
11. Match timing parameters are tested with RL = 200 and CL = 30pF as shown in Fig. 3.

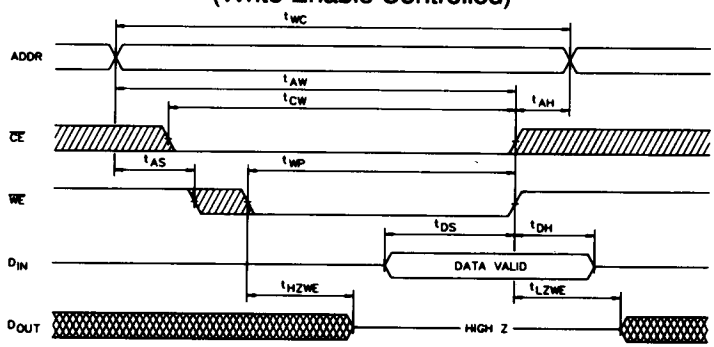
## READ CYCLE NO. 1 (8, 9)



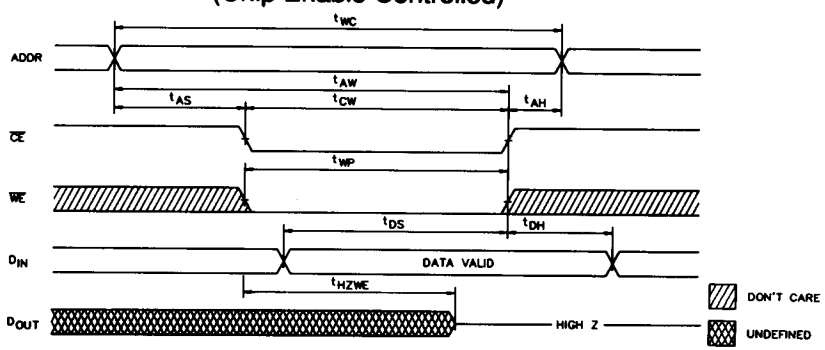

## READ CYCLE NO. 2 (7, 8, 10)




## WRITE CYCLE NO. 1
(Write Enable Controlled)




## WRITE CYCLE NO. 2
(Chip Enable Controlled)



## ORDER INFORMATION


**MT5C6405 DJ-25T**
**MT5C6405 EC-35T**

The Micron Fast SRAM family is functionally equivalent to other manufacturer's products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A. at Micron's modern Boise, Idaho facility. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. Several parameters are sampled; however, functionality is consistently assured over a wider power supply and temperature range than specified. Each unit receives accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you.