FAIRCHILD

SEMICONDUCTOR™

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MM74HC589
8-Bit Shift Registers with Input Latches and 3-STATE Serial Output

General Description

The MM74HC589 high speed shift register utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

The MM74HC589 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Data can also be entered serially the shift register through the SER pin. Both the storage register and shift register have positive-edge triggered clocks, RCK and SCK, respectively. $\overline{SLOAD}$ pin controls parallel LOAD or serial shift operations for the shift register. The shift register has a 3-STATE output to enable the wire-ORing of multiple devices on a serial bus.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

■ 8-bit parallel storage register inputs
■ Wide operating voltage range: 2V–6V
■ Shift register has direct overriding load
■ Guaranteed shift frequency. . . DC to 30 MHz
■ Low quiescent current: 80 µA maximum (74HC Series)
■ 3-STATE output for 'Wire-OR'

Ordering Code:

Order Number	Package Number	Package Description
MM74HC589M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC589SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC589MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC589N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP

Top View
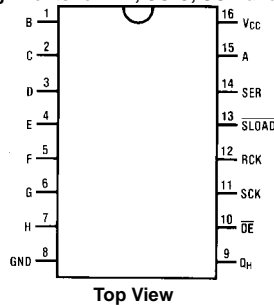
Truth Table

RCK	SCK	SLOAD	$\overline{OE}$	Function
X	X	X	H	Q_H in Hi-Z State
X	X	X	L	Q_H is enabled
↑	X	X	X	Data loaded into input latches
↑	X	L	X	Data loaded into shift register from pins
H or L	X	L	X	Data loaded from latches to shift register
X	↑	H	X	Shift register is shifted. Data on SER pin is shifted in.
↑	↑	H	X	Data is shifted in shift register, and data is loaded into latches

Block Diagram (positive logic)

Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 6.0 mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\|$ ≤ 7.8 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 6.0 mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\|$ ≤ 7.8 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA
I_{OZ}	Maximum 3-STATE Leakage Current	Output in High Impedance State V_{IN} = V_{IL} or V_{IH} V_{OUT} = V_{CC} or GND $\overline{OE}$ = V_{IH}	6.0V		±0.5	±5.0	±10.0	μA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency for SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to $Q_{H'}$			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SLOAD}$ to $Q_{H'}$			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from LCK to $Q_{H'}$	$\overline{SLOAD}$ = logic "0"	25	45	ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L = 1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$R_L = 1$ kΩ, $C_L = 5$ pF	19	25	ns
t_S	Minimum Setup Time from RCK to SCK		10	20	ns
t_S	Minimum Setup Time from SER to SCK		10	20	ns
t_S	Minimum Setup Time from Inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		0	5	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{\overline{SLOAD}}$		8	16	ns

AC Electrical Characteristics

$V_{CC} = 2.0-6V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	Guaranteed Limits	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
f_{MAX}	Maximum Operating Frequency for SCK		2.0V		6	4.8	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK or $\overline{SLOAD}$ to Q_H		2.0V	62	175	220	265	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	37	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK or $\overline{SLOAD}$ to Q_H	$C_L = 150$ pF	2.0V	120	225	280	340	ns
			4.5V	31	45	56	68	ns
			6.0V	28	38	48	58	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_H		2.0V	80	210	265	315	ns
			4.5V	25	42	53	63	ns
			6.0V	21	36	45	54	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay RCK to Q_H	$C_L = 150$ pF	2.0V	80	210	265	313	ns
			4.5V	25	52	66	77	ns
			6.0V	21	44	56	66	ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L = 1$ kΩ	2.0V	70	150	189	224	ns
			4.5V	22	30	38	45	ns
			6.0V	20	26	32	38	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$R_L = 1$ kΩ	2.0V	70	150	189	224	ns
			4.5V	22	30	38	45	ns
			6.0V	20	26	32	38	ns
t_S	Minimum Setup Time from RCK to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_S	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_S	Minimum Setup Time from Inputs A thru H to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_H	Minimum Hold Time		2.0V	−5	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	1	5	5	5	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SLOAD}$, $\overline{SLOAD}$		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$ Guaranteed Limits	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
t_r, t_f	Maximum Input Rise and		2.0V		1500	1500	1500	ns
	Fall Time, Clock		4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output		2.0V	25	60	75	90	ns
	Rise and Fall Time		4.5V	6	12	15	18	ns
			6.0V	5	10	12	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			87				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} sf + I_{CC}$.
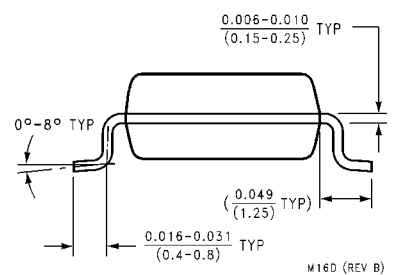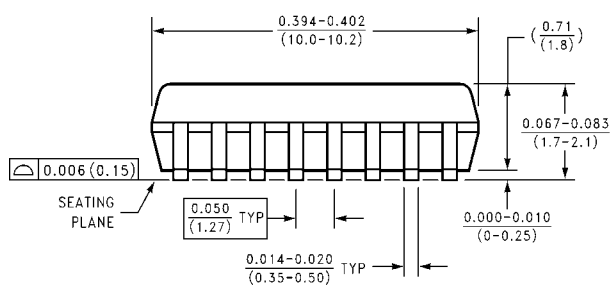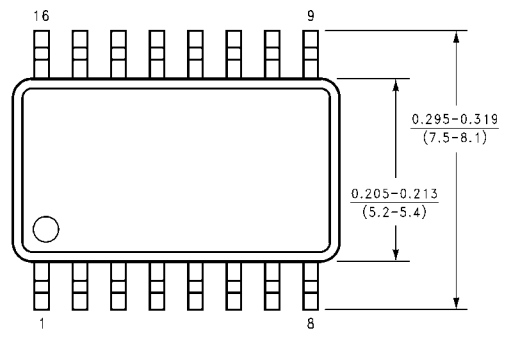
Timing Diagram
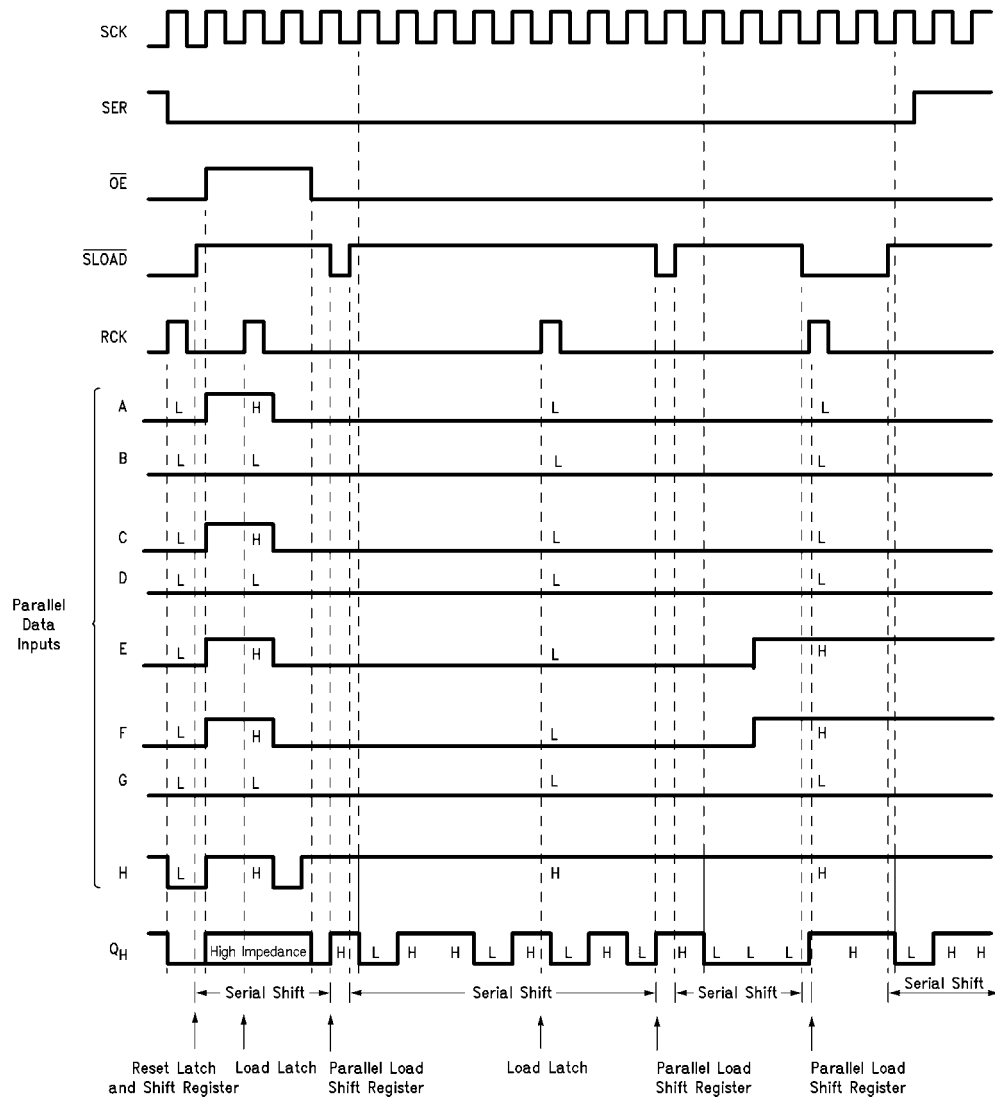
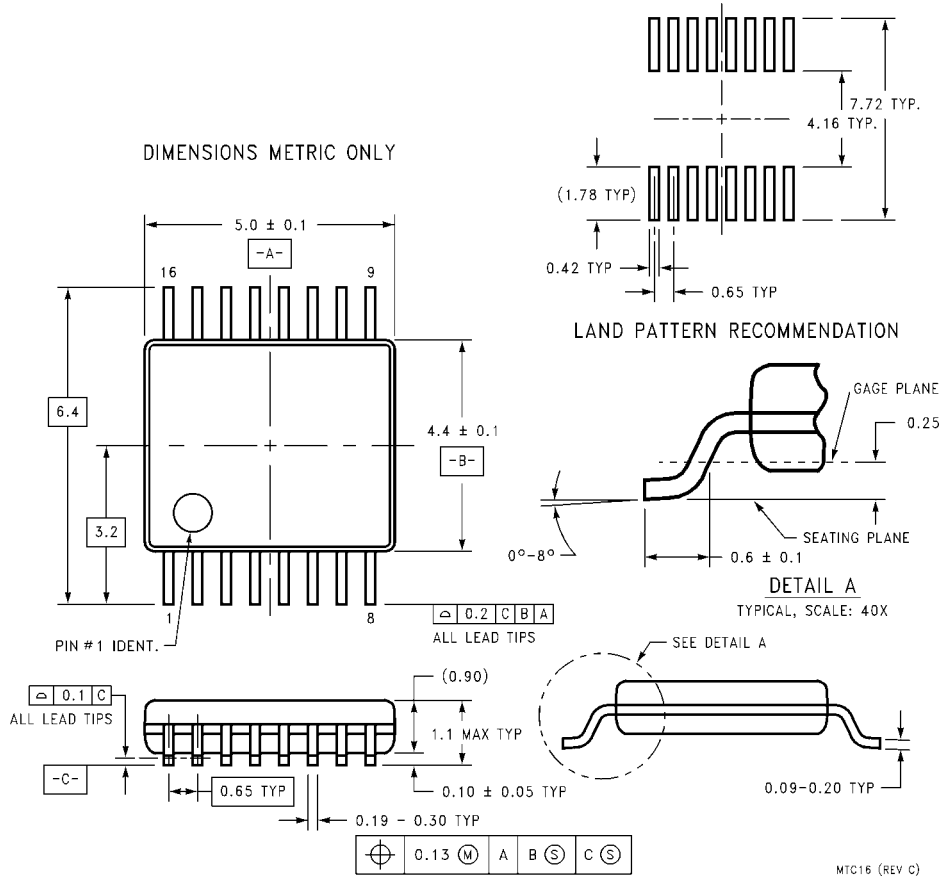# Physical Dimensions inches (millimeters) unless otherwise noted

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO.1
IDENT

1 2 3 4 5 6 7 8

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020 TYP
(0.356 − 0.508)

M16A (REV H)
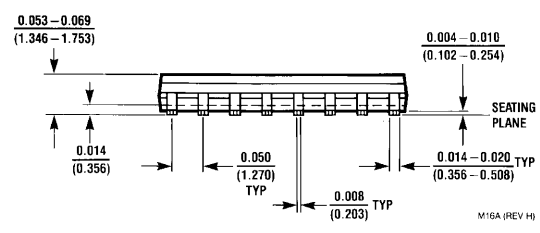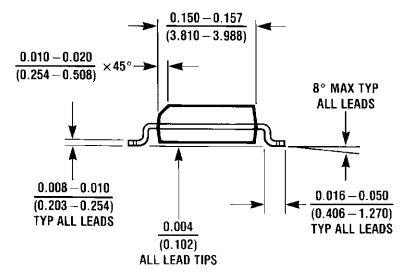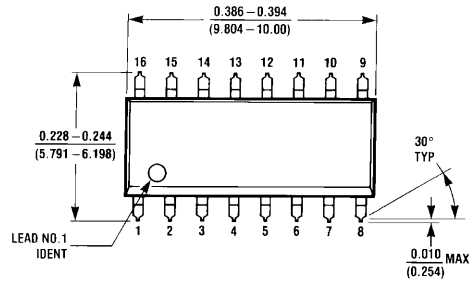
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

16   9

0.295−0.319
(7.5−8.1)

0.205−0.213
(5.2−5.4)

1   8

0.394−0.402
(10.0−10.2)

(0.71)
(1.8)

0.006−0.010 TYP
(0.15−0.25)

□ 0.006 (0.15)

0.067−0.083
(1.7−2.1)

SEATING
PLANE

0.050 TYP
(1.27)

0.000−0.010
(0−0.25)

0°−8° TYP

0.014−0.020 TYP
(0.35−0.50)

(0.049 TYP)
(1.25)

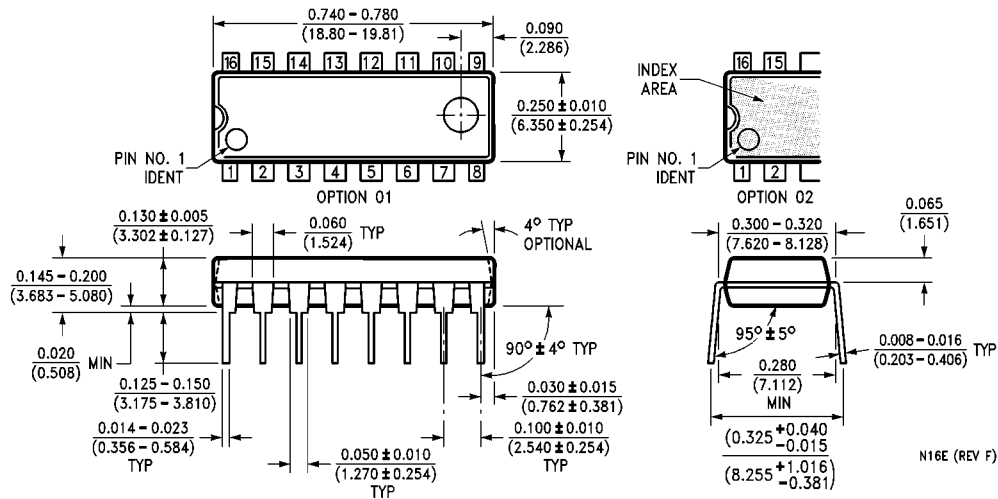0.016−0.031 TYP
(0.4−0.8)

M16D (REV B)

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS METRIC ONLY

7.72 TYP.

4.16 TYP.

(1.78 TYP)

0.42 TYP

0.65 TYP

LAND PATTERN RECOMMENDATION

5.0 ± 0.1

-A-

16   9

6.4

4.4 ± 0.1

-B-

3.2

GAGE PLANE

0.25

0°-8°

0.6 ± 0.1

SEATING PLANE

DETAIL A
TYPICAL, SCALE: 40X

1   8

| ⌖ | 0.2 | C | B | A |

ALL LEAD TIPS

PIN #1 IDENT.

| ⌖ | 0.1 | C |

ALL LEAD TIPS

-C-

0.65 TYP

0.19 - 0.30 TYP

(0.90)

1.1 MAX TYP

0.10 ± 0.05 TYP

SEE DETAIL A

0.09-0.20 TYP

| ⌖ | 0.13 Ⓜ | A | B Ⓢ | C Ⓢ |

MTC16 (REV C)

16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.740 − 0.780
(18.80 − 19.81)

0.090
(2.286)

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

OPTION 01

INDEX
AREA

PIN NO. 1
IDENT

OPTION 02

0.065
(1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.145 − 0.200
(3.683 − 5.080)

0.300 − 0.320
(7.620 − 8.128)

0.020
(0.508) MIN

90° ± 4° TYP

95° ± 5°

0.008 − 0.016
(0.203 − 0.406) TYP

0.125 − 0.150
(3.175 − 3.810)

0.030 ± 0.015
(0.762 ± 0.381)

0.280
(7.112)
MIN

0.014 − 0.023
(0.356 − 0.584)
TYP

0.100 ± 0.010
(2.540 ± 0.254)
TYP

$(0.325\,^{+0.040}_{-0.015})$

0.050 ± 0.010
(1.270 ± 0.254)
TYP

$(8.255\,^{+1.016}_{-0.381})$

N16E (REV F)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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