PLESSEY
Semiconductors

# MJ2841

## 64-WORD x 4-BIT FIRST-IN FIRST-OUT SERIAL MEMORY

The MJ2841 is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four bit parallel word $D_0$-$D_3$ under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs $Q_0$-$Q_3$. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written.

A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFO's to obtain deeper stacks.

Parallel expansion to wider words only requires that rows if FIFO's be placed side by side. Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates.

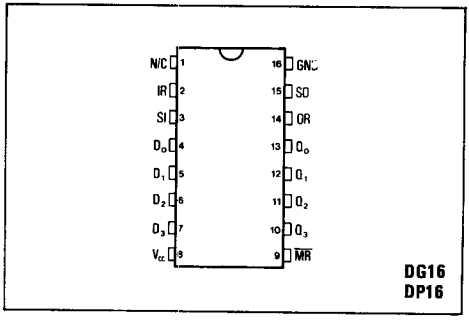



*Fig.1 Pin connections (top view)*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage temperature | -55°C to +125°C |
| Ambient operating temperature | -10°C to +85°C |
| Lead temperature (soldering, 10s max.) | 330°C |
| Voltage on any pin with respect to ground | -0.3V to +7V |

### FEATURES

- Single 5V Supply
- 1.75 MHz Guaranteed Data Rate (Typically 4 MHz)
- Pin Compatible with AM2841/Fairchild 3341
- Asynchronous Buffer For Up To 64 Four Bit Words
- Easily Expandable To Larger Buffers

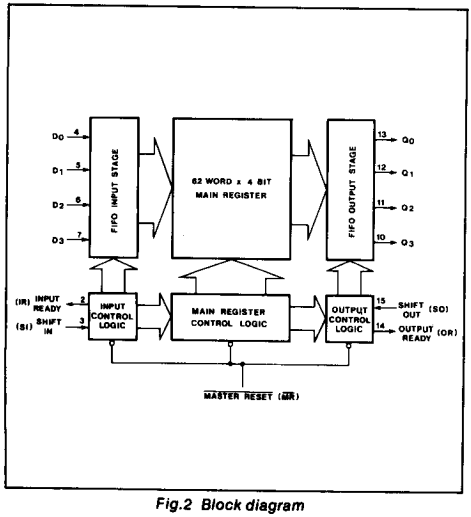



*Fig.2 Block diagram*

### MJ2841 FIFO OPERATION

The MJ2841 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the $n^{th}$ bit of control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the $n^{th}$ data register, simultaneously setting the (n+1)th control register bit, so that the control flag moves with the data. In this fashion, data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs $D_0$-$D_3$ by applying a low to high transition on the shift in (SI) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes low indicating that data has been entered into the first data register and

the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the first control register bit is cleared. This causes IR to go high indicating the inputs are available for another data word.

The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the four data outputs $Q_0$-$Q_3$. An input signal, shift out (SO) is used to shift the data out of the FIFO. A low to high transition on SO clears the last register bit, causing OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the '0' which is now present at the last register allows the data in the next to last register position to move into the last register position and on to the outputs. The '0' in the control register then 'bubbles' back towards the input as the data shifts towards the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes high, OR will go low as before, but when SO next goes low, there is no data to move into the last location so OR remains low until more data arrives at the output. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

An over-riding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the outputs to all low).

## ELECTRICAL CHARACTERISTICS

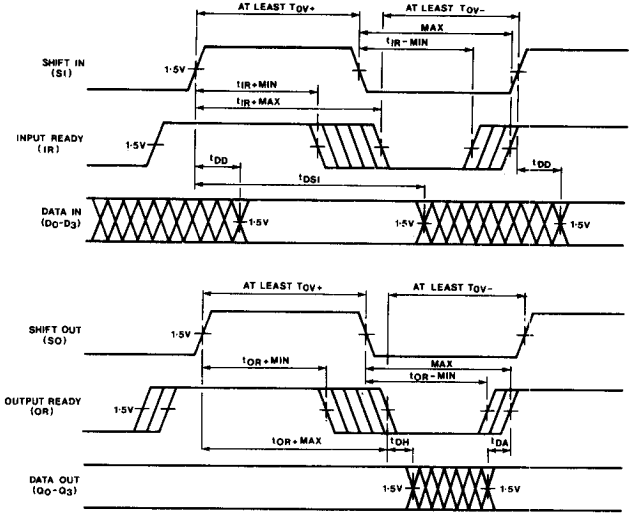
**Test conditions (unless otherwise stated):**
Supply voltage ($V_{CC}$) = +5V ±5%, $T_{amb}$ = 0°C to +70°C
Typical Values at $V_{CC}$ = 5V and $T_{amb}$ = +25°C
All voltages with respect to ground

### Static Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| O/P high voltage | $V_{OH}$ | 2.7 | 3.2 | | V | $I_{OH}$ = -0.2mA |
| O/P low voltage | $V_{OL}$ | | 0.2 | 0.5 | V | $I_{OL}$ = 2mA |
| I/P high level | $V_{IH}$ | 2.5 | | | V | |
| I/P low level | $V_{IL}$ | | | 0.8 | V | |
| I/P leakage current | $I_{IL}$ | -5 | | +10 | μA | $V_{IN}$ = 0V or 5V |
| Supply current | $I_{CC}$ | | 50 | 81 | mA | |

### Switching Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. SI or SO frequency | $f_{MAX}$ | 1.75 | 4.4 | | MHz | |
| Delay, SI high to IR low | $t_{IR}+$ | | 50 | 120 | ns | |
| Delay, SI low to IR high | $t_{IR}-$ | | 80 | 200 | ns | |
| Min. time SI and IR both high | $t_{OV}+$ | | <25 | 45 | ns | |
| Min. time SI and IR both low | $t_{OV}-$ | | <25 | 45 | ns | |
| Data release time | $t_{DSI}$ | | 45 | 110 | ns | |
| Data set-up time | $t_{DD}$ | | 45 | 110 | ns | |
| Delay, SO high to OR low | $t_{OR}+$ | | 80 | 190 | ns | |
| Delay, SO low to OR high | $t_{OR}-$ | | 120 | 290 | ns | |
| Ripple through time | $t_{PT}$ | | 2.5 | 7 | μs | FIFO empty |
| Delay, OR low to data out | $t_{DH}$ | 50 | 85 | | ns | SO = low |
| Min. reset pulse width | $t_{MRW}$ | | 20 | 50 | ns | |
| Delay, data out to OR high | $t_{DA}$ | 0 | 35 | | ns | SO = high |
| Input capacitance | CI | | | 7 | pF | Any pin |




**KEY TO TIMING DIAGRAM**

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DONT CARE ANY CHANGE PERMITTED | CHANGING STATE UNKNOWN |

*Fig.3 Timing diagram*

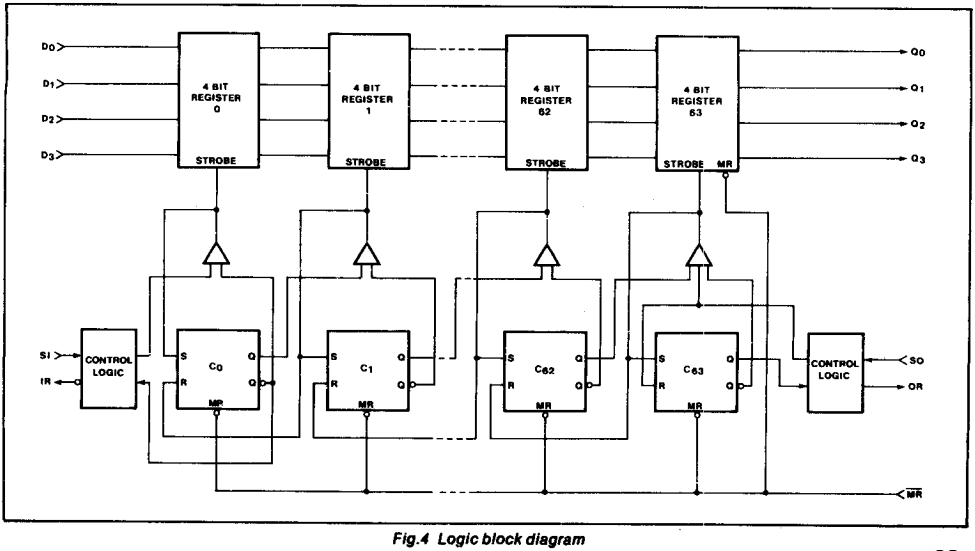



*Fig.4 Logic block diagram*

## OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However OR will remain low, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.
3. If SO is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least $t_{OR}+$) and then will go back to low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought low.
4. When the master reset is brought low, the control register and the outputs are cleared. IR goes high and OR goes low. If SI is high when the master reset goes high then the data on the inputs will be written into the memory and IR will return to the low state until SI is brought low. If SI is low when the master reset is ended, the IR will go high, but the data on the inputs will not enter the memory until SI goes high.