MOTOROLA

MC3416

Specifications and Applications Information

4 x 4 x 2 CROSSPOINT SWITCH

The MC3416 consists of a pair of 4 x 4 matrices of dielectrically isolated SCR's, triggered by a common selection matrix. The device is intended for switching analog signals in communication systems. The use of dielectric isolation processing provides excellent crosstalk isolation while maintaining minimal insertion loss.

The selection array consists of PNP transistors with the input thresholds compatible with either McMOS or MTTL logic families.

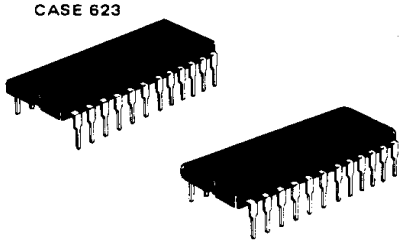
The MC3416 is a monolithic pin-for-pin replacement for the discontinued MCBH7601 hybrid device.

- Low Series Resistance – r_{on} = 6.0 Ohms (Typ) @ I_{AK} = 20 mA
- High Series Resistance – r_{off} = 100 MΩ (Min)
- Pin Compatible with MCBH7601 or RC4444
- High Breakdown Voltage – 30 V (Typ)
- Selection Matrix Compatible with TTL or CMOS Logic Levels
- Dielectric Isolation Insures Low Crosstalk and Low Insertion Loss

4 x 4 x 2 CROSSPOINT SWITCH

DIELECTRICALLY ISOLATED MONOLITHIC INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649

FIGURE 1 – REPRESENTATIVE CELL SCHEMATIC
(Repeated 16 Times)

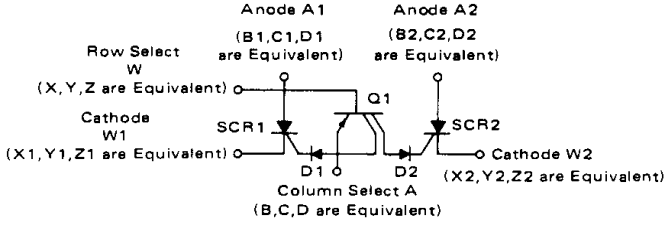
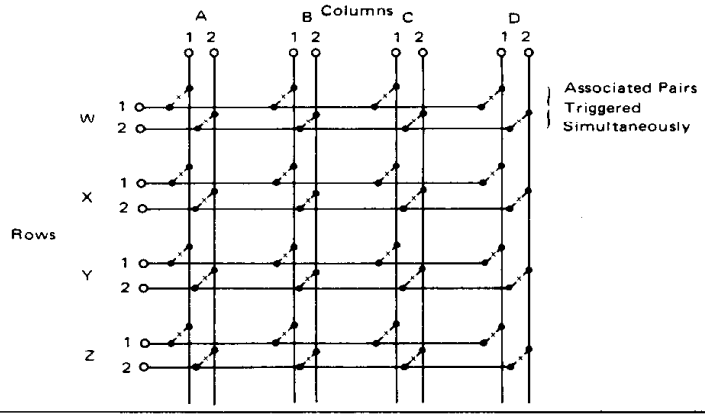
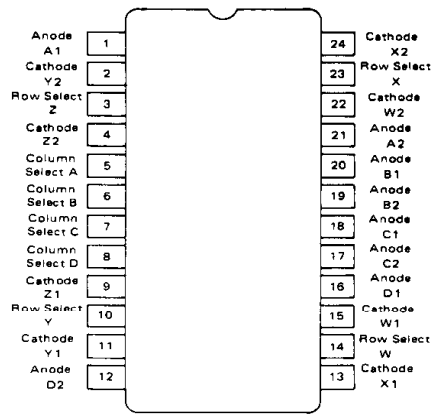


FIGURE 2 – MATRIX CONFIGURATION AND NOMENCLATURE
(X Indicates a Possible Connection)



PIN CONNECTIONS



MAXIMUM RATINGS (Unless otherwise noted, T_A = 25°C)

Rating	Symbol	Value	Unit
Anode-Cathode Current – Continuous (only one SCR at a time)	I_{AK}	150	mA
Enable Current	I_{En}	10	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	150°C	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Max	Unit
Anode Cathode Breakdown Voltage (I_{AK} = 25μA)	BV_{AK}	25	–	Vdc
Cathode-Anode Breakdown Voltage (I_{KA} = 25μA)	BV_{KA}	25	–	Vdc
Base-Cathode Breakdown Voltage (I_{BK} = 25μA)	BV_{BK}	25	–	Vdc
Cathode-Base Breakdown Voltage (I_{KB} = 25μA)	BV_{KB}	25	–	Vdc
Base-Emitter Breakdown Voltage (I_{BE} = 25μA)	BV_{BE}	25	–	Vdc
Emitter-Cathode Breakdown Voltage (I_{EK} = 25μA)	BV_{EK}	25	–	Vdc
OFF State Resistance (V_{AK} = 10 V)	r_{off}	100	–	MΩ
Dynamic ON Resistance (Center Current = 10 mA) (See Figure 8) (Center Current = 20 mA)	r_{on}	 4.0 2.0	 12 10	Ω
Holding Current (See Figure 10)	I_H	0.7	3.0	mA
Enable Current (V_{BE} = 1.5 V) (See Figure 7)	I_{En}	4.0	–	mA
Anode-Cathode ON Voltage (I_{AK} = 10 mA) (I_{AK} = 20 mA)	V_{AK}	 – –	 1.0 1.1	V
Gate Sharing Current Ratio @ Cathodes (Under Select Conditions with Anodes Open) (See Figure 3)	G_{Sh}	0.8	1.25	mA/mA
Inhibit Voltage (V_B = 3.0 V) (See Figure 9)	V_{inh}	–	0.3	V
Inhibit Current (V_B = 3.0 V) (See Figure 9)	I_{inh}	–	0.1	mA
OFF State Capacitance (V_{AK} = 0 V) (See Figure 6)	C_{off}	–	2.0	pF
Turn-ON Time (See Figure 4)	t_{on}	–	1.0	μs
Minimum Voltage Ramp (Which Could Fire the SCR Under Transient Conditions)	dv/dt	800	–	V/μs

FIGURE 3 – TEST CIRCUIT

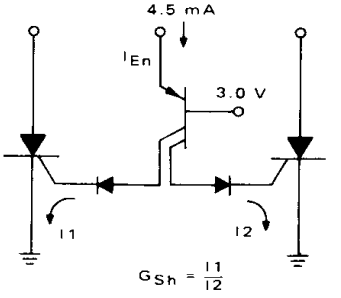


FIGURE 4 – TEST CIRCUIT FOR dv/dt AND t_{on}

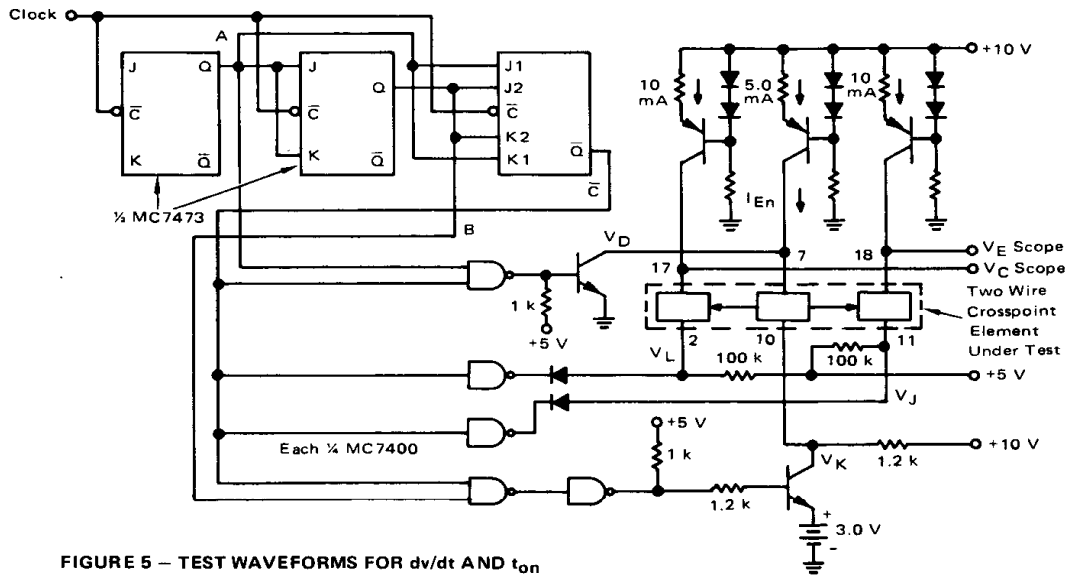


FIGURE 5 – TEST WAVEFORMS FOR dv/dt AND t_{on}

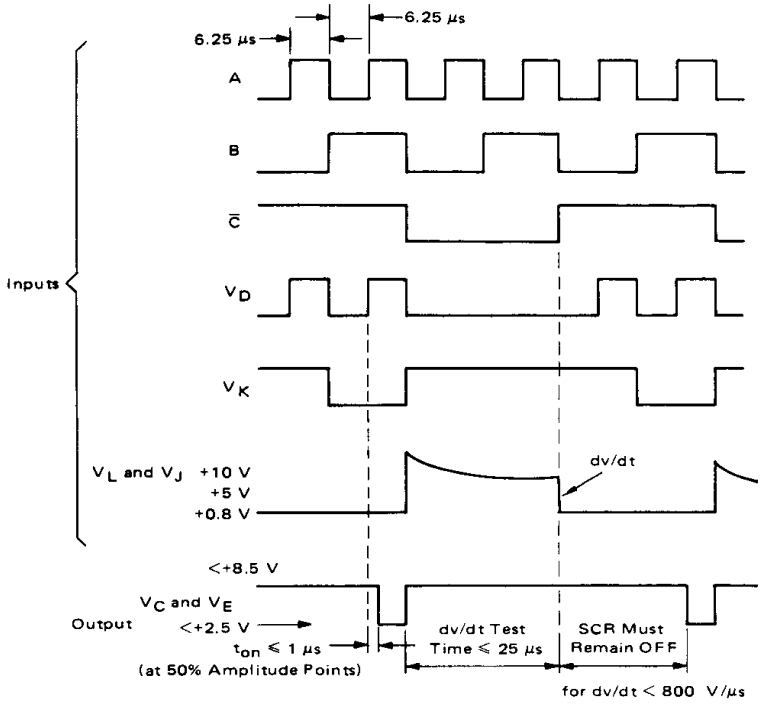


FIGURE 6 – TEST CIRCUIT FOR OFF-STATE CAPACITANCE

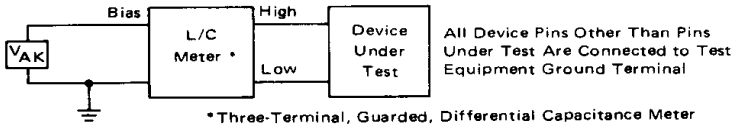


FIGURE 7 – ENABLE CURRENT
(Both SCR's Must Turn On)

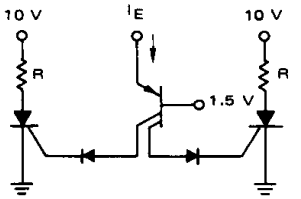


FIGURE 8 – THE CROSSPOINT SCR I-V CHARACTERISTIC (I_G = 0)

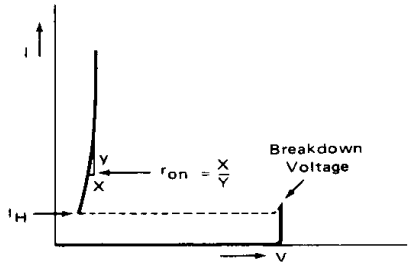
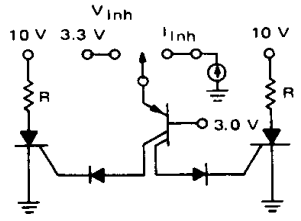


FIGURE 9 – INHIBIT VOLTAGE AND INHIBIT CURRENT (Both SCR's Must Remain OFF)



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TYPICAL CHARACTERISTICS

FIGURE 10 – HOLDING CURRENT versus AMBIENT TEMPERATURE

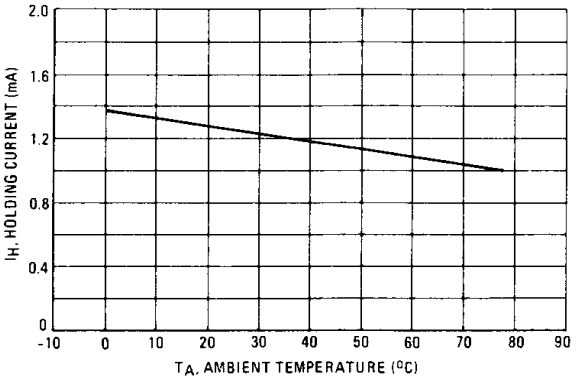


FIGURE 11 – ANODE-CATHODE ON VOLTAGE versus CURRENT AND TEMPERATURE

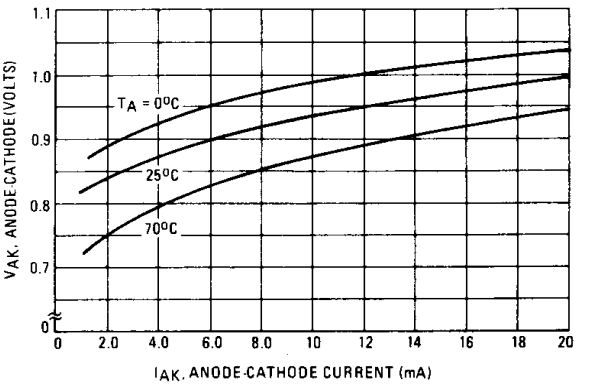


FIGURE 12 – DIFFERENCE IN ANODE-CATHODE ON VOLTAGE (Between Associate Pairs of SCR's) versus ANODE-CATHODE CURRENT

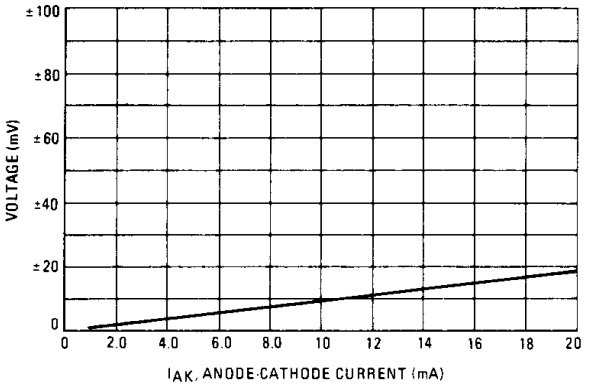


FIGURE 13 – OFF-STATE CAPACITANCE versus ANODE-CATHODE VOLTAGE

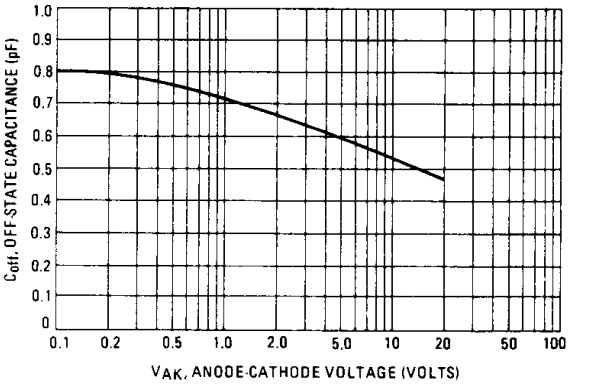


FIGURE 14 – DYNAMIC ON RESISTANCE versus ANODE-CATHODE CURRENT

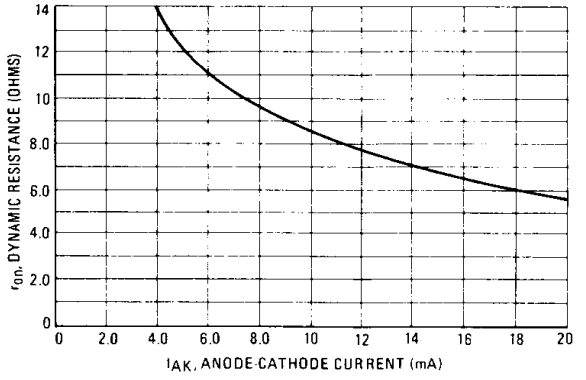


FIGURE 15 – DYNAMIC ON RESISTANCE versus AMBIENT TEMPERATURE

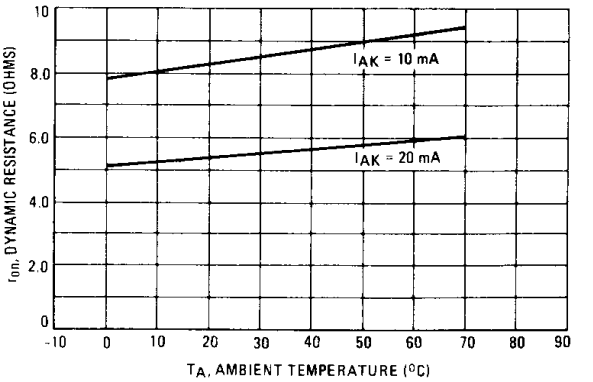


FIGURE 16 – FEEDTHROUGH versus SIGNAL FREQUENCY

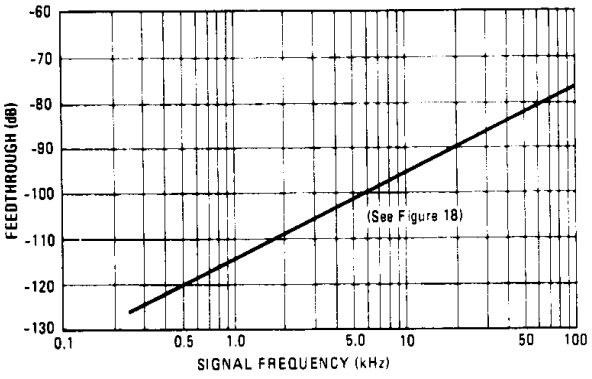


FIGURE 17 – CROSSTALK versus SIGNAL FREQUENCY

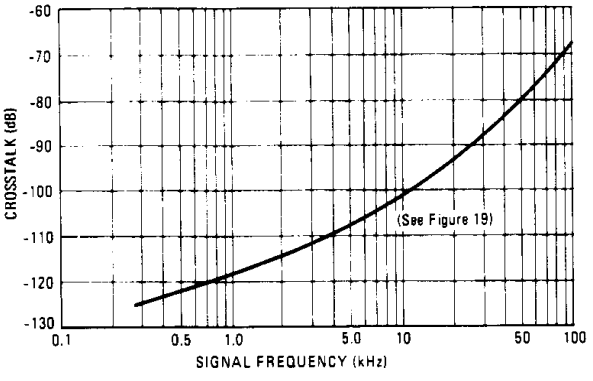


FIGURE 18 – TEST CIRCUIT FOR FEEDTHROUGH versus FREQUENCY

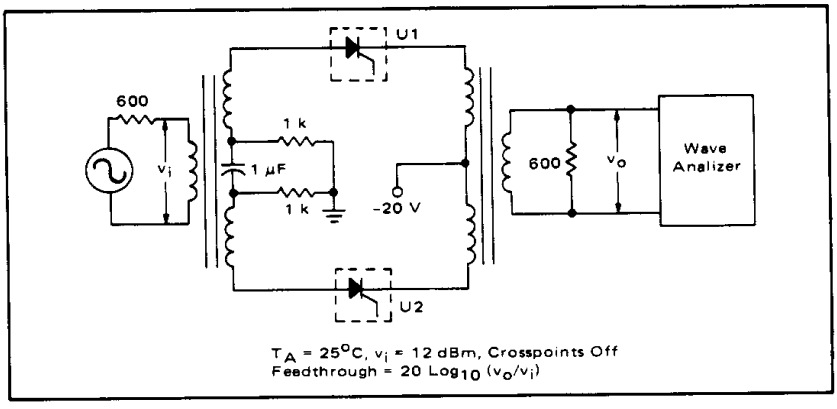


FIGURE 19 – TEST CIRCUIT FOR CROSSTALK versus FREQUENCY

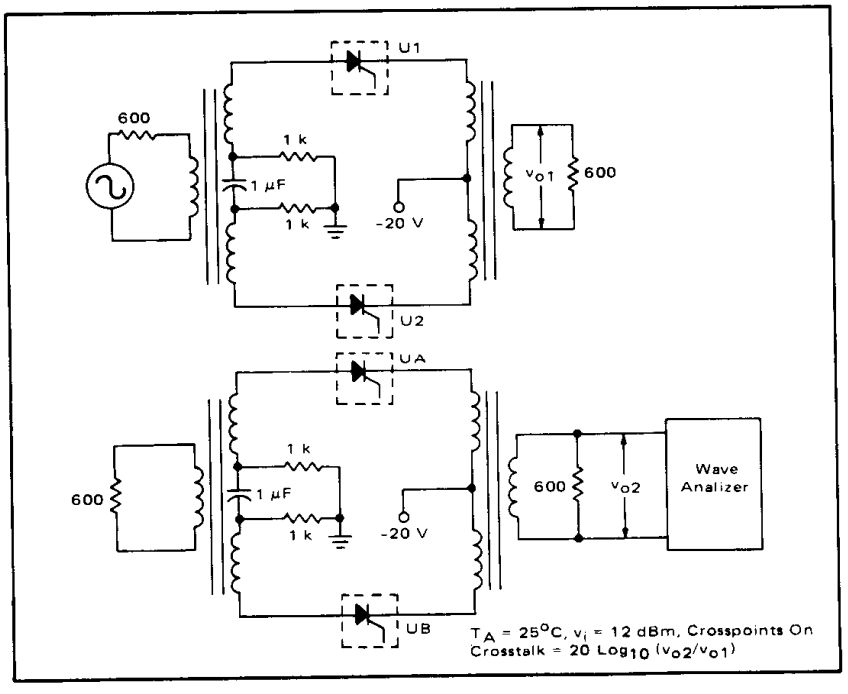
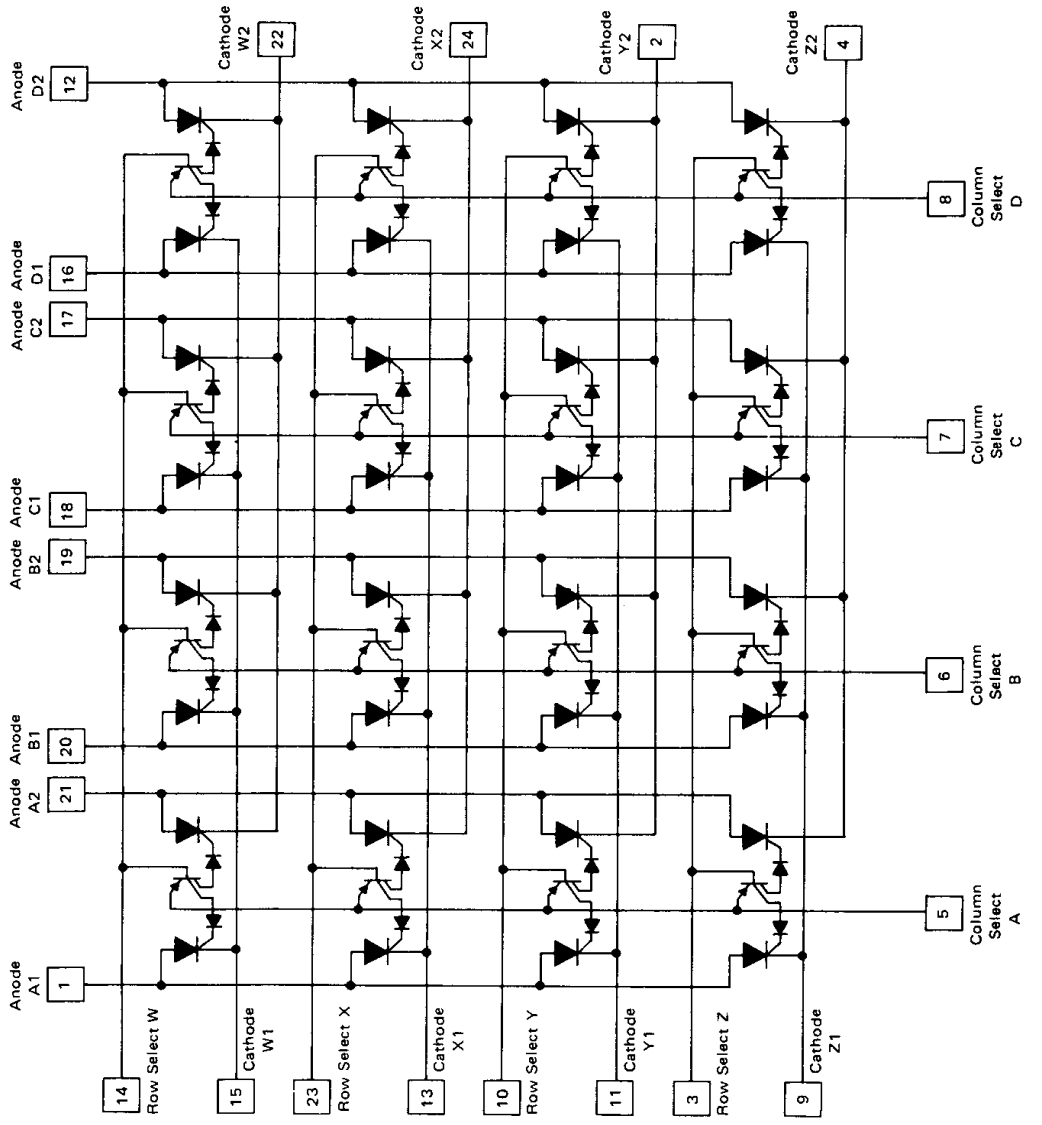


FIGURE 20 – REPRESENTATIVE SCHEMATIC DIAGRAM



TELEPHONE APPLICATION OF THE CROSSPOINT SWITCH

The MC3416 crosspoint switch is designed to provide a low-loss analog switching element for telephony signals. It can be addressed and controlled from standard binary decoders and is CMOS compatible. With proper system organization the MC3416 can significantly reduce the size and cost of existing crosspoint matrices.

SIGNAL PATH CONSIDERATIONS

The MC3416 is a balanced 4 x 4 2-wire crosspoint array. It is ideal for balanced transmission systems, but may be applied effectively in a number of single ended applications. Multiple chips may be interconnected to form larger crosspoint arrays. The major design constraint in using SCR crosspoints is that a forward dc current must be maintained through the SCR to retain an ac signal path. This requires that each subscriber-input to the array be capable of sourcing dc current as well as its ac signal. With each subscriber acting as a dc source, each trunk output then acts as a current sink. The instrument-to-trunk connection in Figure 21 shows this configuration. However, with each subscriber acting as a dc source, some method of interconnecting them without a trunk must be provided. Such a local or intercom termination is shown in Figure 22. Here both subscribers source dc current and exchange ac signals. The central current sink accepts current from both subscribers while the high output impedance of the current sink does not disturb the system.

These configurations are system compatible. The dc

FIGURE 21 – INSTRUMENT-TO-TRUNK CONNECTION

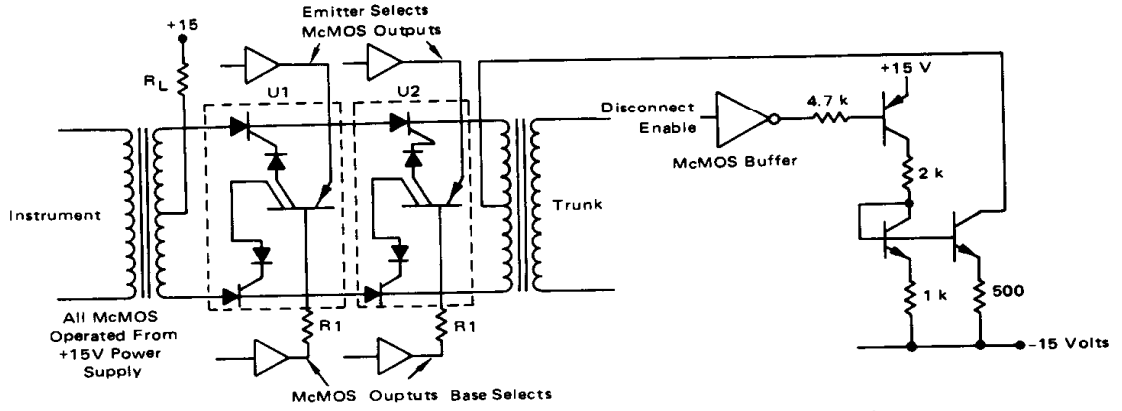
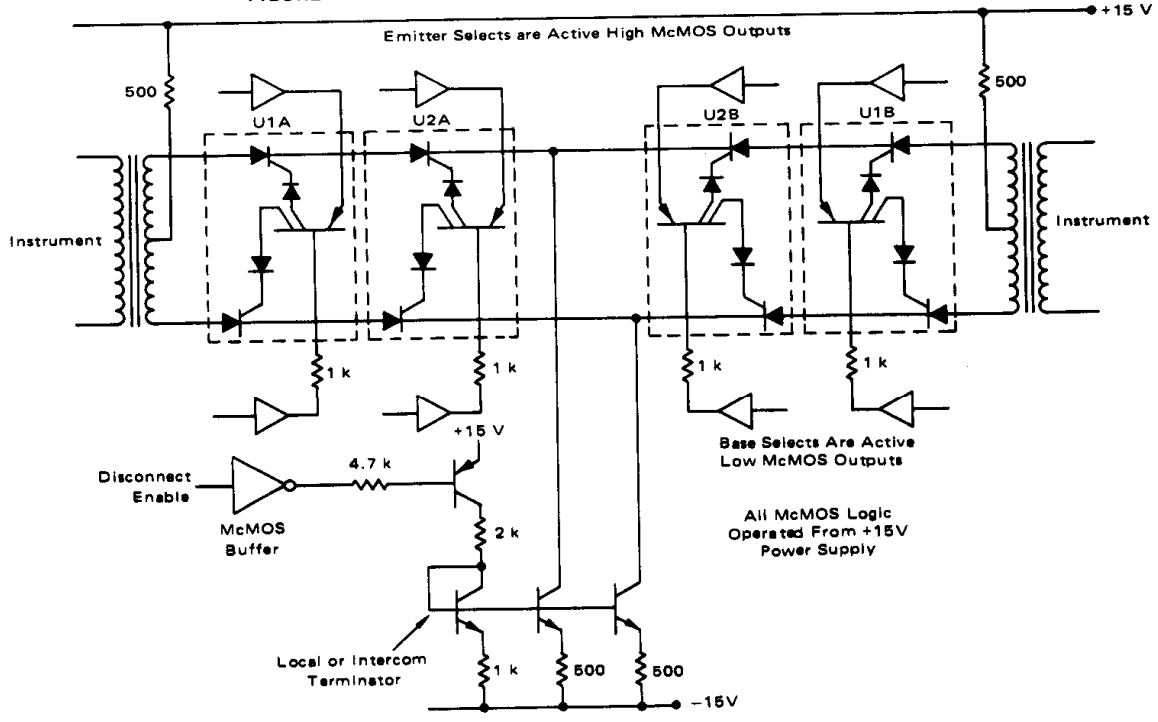


FIGURE 22 – TYPICAL INSTRUMENT TO INSTRUMENT CONNECTION

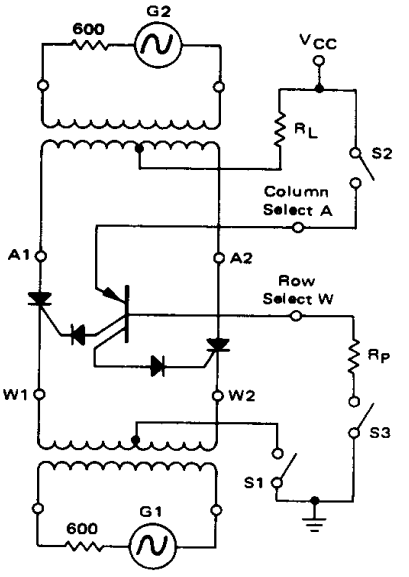


current restriction is not a restriction in the design of an efficient crosspoint array. Because of the current sink terminations, a signal path may use differing numbers of crosspoints in any connection or in two sides of the same connection further relaxing restrictions in array design.

Figure 23 demonstrates circuit operation. S1, S2, and S3 are open. The Crosspoint SCR's are off as they have no gate drive or dc current path through S1. By closing S2 and S3, gate drive is provided, but the SCR's still remain off as there is no dc current path to hold them on. Close S1 and the circuit is enabled, but with S2 and S3 off there is still no signal path. Closing S2 and S3 with S1 closed – current is injected into both gates and they switch on. DC current through R_L splits around the center-tapped winding and flows through each SCR, back through the lower winding and through S1 to ground. If S2 and S3 are opened, that current path still remains and the SCRs remain on. If an ac signal is injected at either G1 or G2, it will be transmitted to the other signal port with negligible loss in the SCR's. To disconnect the ac signal path the SCR's must be commutated off. By opening S1 the dc current path is interrupted and the SCR's switch off. The ac signal path is disconnected. With S1 closed the circuit is enabled and may be addressed again from S2 and S3. This circuit demonstrates a balanced transmission configuration. The transmission characteristics of the SCR's simulate a relay contact in that the ac signal does not incur a contact voltage drop across the crosspoint. The memory characteristics of the crosspoint are demonstrated by the selective application of S1, S2, and S3.

The selection of R_L is governed by the power supply voltage and the desired dc current. If 10 mA is to flow through each SCR then R_L must pass 20 mA. Thus, $(V_{CC} - V_{AK})/R_L = 20$ mA. The selection of Rp is governed by the characteristics for crosspoint turn on. Adequate enable current must be injected into the column select and Rp should drop at least 1.5 Volts. The PNP transistor has a typical gain of one. Thus, Rp should pass at least 2 mA to provide 4 mA column select current.

FIGURE 23– CROSSPOINT OPERATION DEMONSTRATION CIRCUIT



S1	S2	S3	LINE CONDITION
ON	X	OFF	Enabled, Not Connected
ON	OFF	X	Enabled, Not Connected
ON	ON	ON	Addressed and Connected
ON	X	X	G1 Connected to G2
OFF	X	X	Disconnected.
X = irrelevant			

*

ADDRESSING CONSIDERATIONS

The MC3416 crosspoint switch is addressed by selecting and turning on the PNP transistor that controls the SCR pair desired. The drive requirements of the MC3416 can be met with standard McMOS outputs. A particular crosspoint is addressed by putting a logical "1" on the emitter and a logical "0" on the base of the appropriate transistor. A resistor in the base circuit of the transistor is required to limit the current and must also drop 1.5 Volts to assure forward bias of the two diodes in the collector circuits.

The gate current required for SCR turn on is 1 mA typically. The McMOS one-of-n decoders listed in Table I provide both active high and active low outputs and are well suited for standard addressing organizations. The major design constraint in organizing the addressing structure is that any signal path which is to be addressed must create a dc path from a source to a sink. If that path requires two crosspoints they must be addressed simultaneously. Of course, once the path is selected, the addressing hardware is free to initiate other signal paths. To meet the dc path

APPLICATIONS INFORMATION (continued)

requirement, crosspoint arrays should be designed in blocks such that any given dc path requires only one crosspoint per block. A signal path, however, may still use two crosspoints in the same block by sequentially addressing two dc paths to the same terminator. For example, the left or right pairs of crosspoints in Figure 22 must be addressed simultaneously but the left pair may be addressed in sequence after addressing the right pair. This is not a difficult constraint to meet and it does not require unnecessary addressing hardware.

TABLE I

	Active High Outputs	Active Low Outputs
Dual Binary to 1 of 4 4-bit latch/4 to 16 BCD to Decimal Decode	MC14555 MC14514 MC14028	MC14556 MC14515

See Application Note AN-760 for additional applications suggestions.

DISCONNECT TECHNIQUES

Since the crosspoint switch maintains signal paths by keeping dc currents through active SCR's, disconnects are easily accomplished by interrupting the dc current path. This can be done anywhere in the circuit, but if the disconnect is done at the terminator then all signal paths established to that terminator are broken simultaneously. In both Figures 21 and 22 this is done by turning off the current sink circuit with a McMOS buffer gate. MC14049 or MC14050 buffers will drive the transistor switch. Once a disconnect is completed, the terminator may be re-enabled and used for another call. Usage of the terminators may be easily monitored with optoelectronic couplers in the collectors of the current sinks without disturbing transmission characteristics.

2

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient