

T-46-23-12

April 1990  
Edition 3.0



DATA SHEET

# MB8464A-80/-80L/-80LL/-10/-10L/-10LL/-15/-15L/-15LL

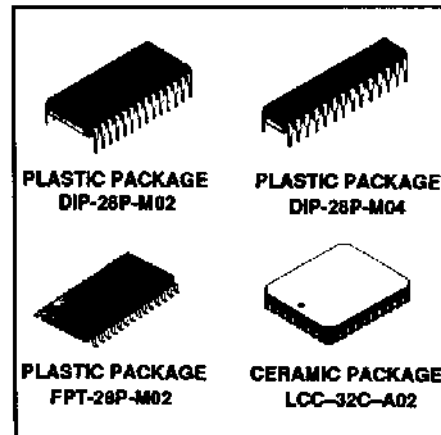
## CMOS 64K BIT LOW POWER SRAM

### 8K Words x 8 Bits CMOS Static RAM with Low Power and Data Retention

The Fujitsu MB8464A is a 8,192 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

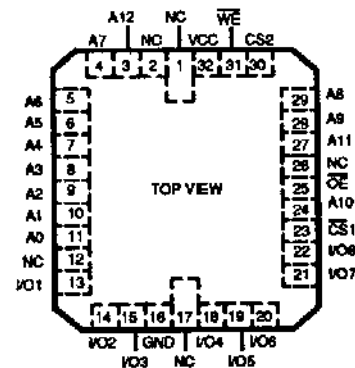
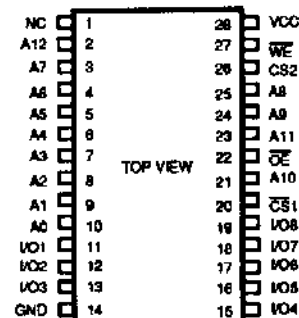
The MB8464A has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 8,192 words x 8 bits
- Access time: 80 ns max. (MB8464A-80/-80L/-80LL)  
100 ns max. (MB8464A-10/-10L/-10LL)  
150 ns max. (MB8464A-15/-15L/-15LL)
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance
- Low power standby: 11 mW max. (MB8464A-80/-10/-15)  
0.55 mW max. (MB8464A-80L/-10L/-15L)  
0.55 mW max. (MB8464A-80LL/-10LL/-15LL)
- Data retention current: 1 mA max. (MB8464A-80/-10/-15)  
25 µA max. (MB8464A-80L/-10L/-15L)  
2 µA max. at 0°C to 40°C (MB8464A-80LL/-10LL/-15LL)
- Data retention: 2.0 V min.
- Standard 28-pin Plastic Packages:
  - DIP (600 mil) MB8464A-xx(L/LL)P
  - Skinny DIP (300 mil) MB8464A-xx(L/LL)PSK
  - SOP (450 mil) MB8464A-xx(L/LL)PF
- Standard 32-pad Ceramic Package:
  - LCC (metal seal) MB8464A-xx(L/LL)CV



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### PIN ASSIGNMENT



### Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.5 to +7.0	V
Input Voltage	V <sub>IN</sub>	-0.5* to V <sub>CC</sub> +0.5	V
Output Voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Temperature Under Bias	T <sub>BIAS</sub>	-10 to +85	°C
Storage Temperature Range	Ceramic	-65 to +150	°C
	Plastic		

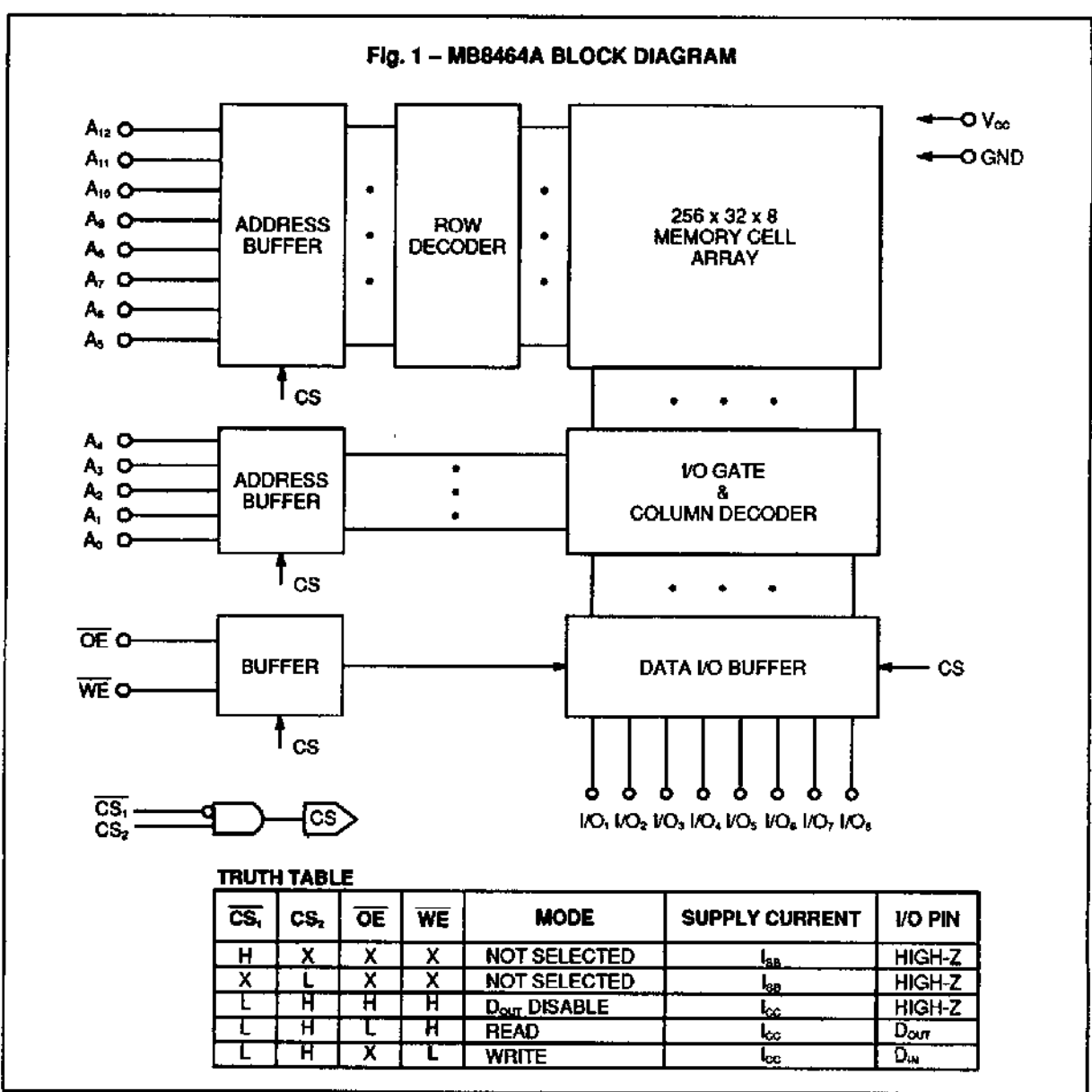
\* -2.0 V for pulse width less than 20 ns.

**Note:** Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB8464A-80/80L/80LL  
 MB8464A-10/10L/10LL  
 MB8464A-15/15L/15LL

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**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ( $V_{IO} = 0V$ )	$C_{IO}$			8	pF
Input Capacitance ( $V_{IN} = 0V$ )	$C_{IN}$			6	pF

MB8464A-80/80L/80LL  
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## RECOMMENDED OPERATING CONDITIONS

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(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Ambient Temperature	$T_A$	0		70	°C

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

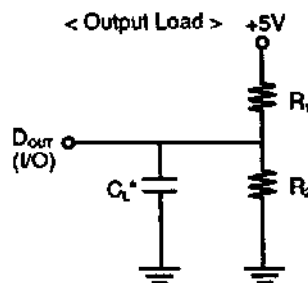
Parameter	Symbol	MB8464A-80/10/15		MB8464A-80L/80LL 10L/10LL/15L/15LL		Unit	Test Condition
		Min	Max	Min	Max		
Standby Supply Current	$I_{BBS}$		2		0.1	mA	$CS_1 \leq 0.2V, \overline{CS}_2 \geq V_{CC} - 0.2V$ ( $CS_2 \leq 0.2V$ or $CS_2 \geq V_{CC} - 0.2V$ )
	$I_{BS2}$		3		3	mA	$\overline{CS}_1 = V_{IH}$ or $CS_2 = V_L$
Active Supply Current	$I_{CC1}$		50		50	mA	$\overline{CS}_1 = V_L, CS_2 = V_{IH}$ $V_{IH} = V_{IH}$ or $V_L, I_{OUT} = 0mA$
Operating Supply Current	$I_{CC2}$		60		60	mA	Cycle=Min., Duty=100% $I_{OUT} = 0mA$
Input Leakage Current	$I_{LI}$	-1	1	-1	-1	μA	$V_{IH} = 0V$ to $V_{CC}$
Output Leakage Current	$I_{LO}$	-2	2	-2	2	μA	$V_{IO} = 0V$ to $V_{CC}$ $\overline{CS}_1 = V_{IH}$ or $CS_2 = V_L$ or $OE = V_{IH}$ or $WE = V_L$
Input Low Voltage	$V_{IL}$	-2.0*	0.8	-2.0*	0.8	V	
Input High Voltage	$V_{IH}$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V	
Output High Voltage	$V_{OH}$	2.4		2.4		V	$I_{OH} = -1.0mA$
Output Low Voltage	$V_{OL}$		0.4		0.4	V	$I_{OL} = 2.1mA$

\* -2.0V Min for pulse width less than 20ns. ( $V_L$  Min. = -0.3V at DC level)

Fig. 2 - AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise and Fall Times: 5ns (Transient Time between 0.8V and 2.2V)
- Timing Reference Levels: Input :  $V_{IL} = 0.8V, V_{IH} = 2.2V$   
Output :  $V_{OL} = 0.8V, V_{OH} = 2.0V$
- Output Load:

	$R_1$	$R_2$	$C_L$	Parameters Measured
Load I	1.8kΩ	990Ω	100pF	except $t_{OLZ}, t_{OLZ}, t_{OHZ}, t_{OHZ}, t_{WLZ}$ and $t_{WHZ}$
Load II	1.8kΩ	990Ω	5pF	$t_{OLZ}, t_{OLZ}, t_{OHZ}, t_{OHZ}, t_{WLZ}$ , and $t_{WHZ}$



\* Including jig and stray capacitance

MB8464A-80/80L/80LL  
 MB8464A-10/10L/10LL  
 MB8464A-15/15L/15LL

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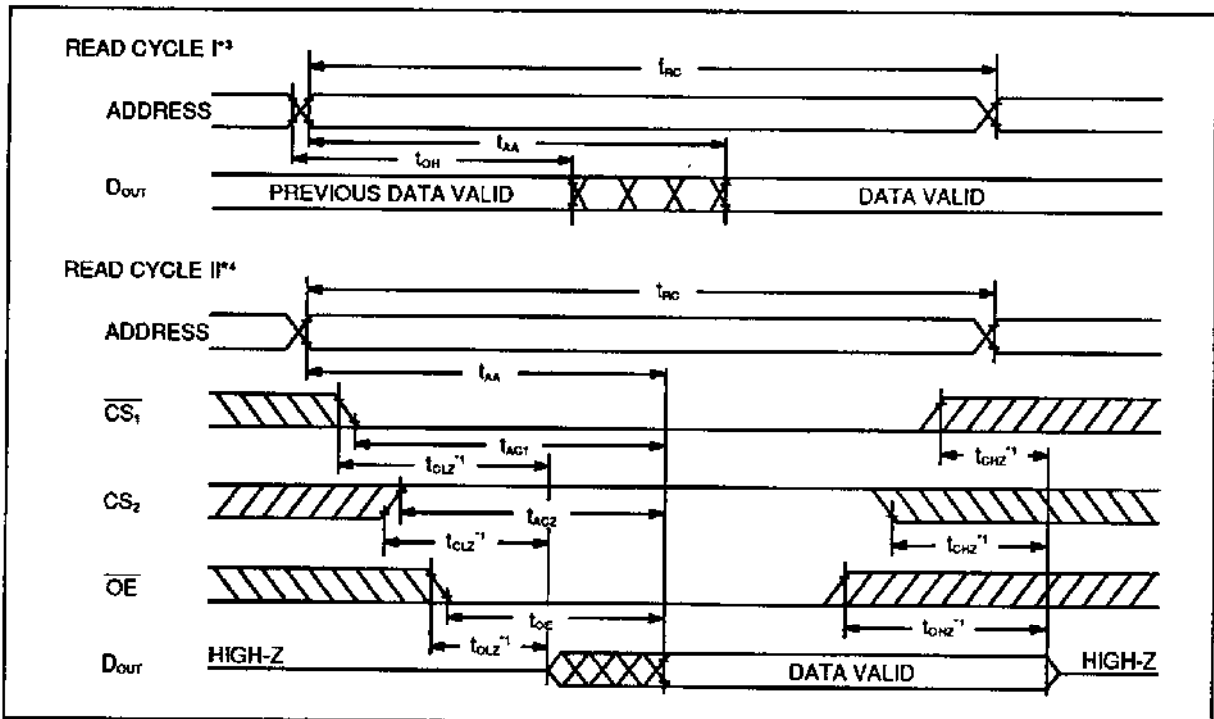
## AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

### READ CYCLE

Parameter	Symbol	MB8464A-80/80L/80LL		MB8464A-10/10L/10LL		MB8464A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{RC}$	80		100		150		ns
Address Access Time	$t_{AA}$		80		100		150	ns
CS <sub>1</sub> Access Time	$t_{AC1}$		80		100		150	ns
CS <sub>2</sub> Access Time	$t_{AC2}$		80		100		150	ns
Output Enable to Output Valid	$t_{OE}$		35		45		55	ns
Output Hold from Address Change	$t_{OH}$	10		10		10		ns
Chip Select to Output Low-Z <sup>*1</sup>	$t_{CLZ}$	10		10		10		ns
Output Enable to Output Low-Z <sup>*1</sup>	$t_{OLZ}$	5		5		5		ns
Chip Select to Output High-Z <sup>*1</sup>	$t_{CHZ}$		35		35		40	ns
Output Enable to Output High-Z <sup>*1</sup>	$t_{OHZ}$		30		35		40	ns

### READ CYCLE TIMING DIAGRAM \*\*



- Note: \*1 Transition is measured at the point of  $\pm 500mV$  from steady state voltage.  
 \*2  $\overline{WE}$  is high for Read Cycle.  
 \*3 Device is continuously selected,  $\overline{CS}_1 = \overline{OE} = V_{IL}$ ,  $CS_2 = V_{IH}$ .  
 \*4 Address valid prior to or coincident with  $\overline{CS}_1$  transition low,  $CS_2$  transition high.

MB8464A-80/80L/80LL

MB8464A-10/10L/10LL

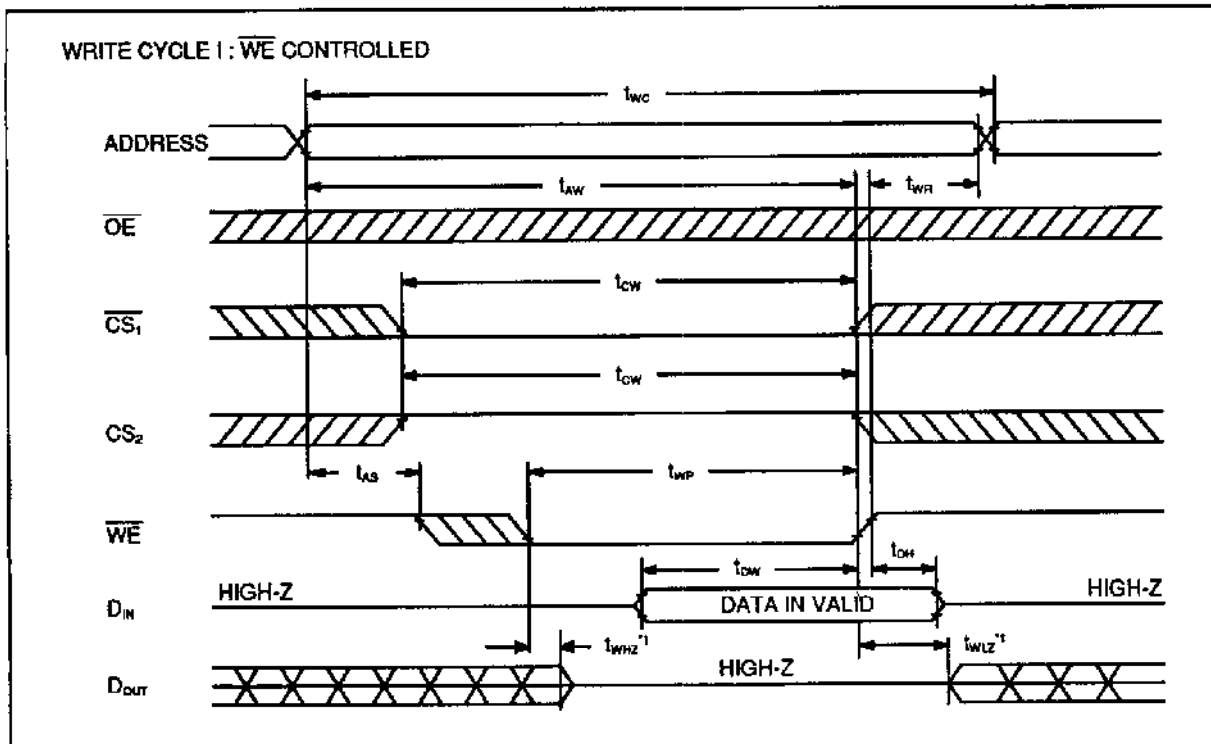
MB8464A-15/15L/15LL

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## WRITE CYCLE

Parameter	Symbol	MB8464A-80/80L/80LL		MB8464A-10/10L/10LL		MB8464A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{wc}$	80		100		150		ns
Address Valid to End of Write	$t_{aw}$	60		80		100		ns
Chip Select to End of Write	$t_{cw}$	60		80		100		ns
Data Valid to End of Write	$t_{dw}$	30		35		40		ns
Data Hold Time	$t_{dh}$	5		5		5		ns
Write Pulse Width	$t_{wp}$	60		70		90		ns
Address Setup Time	$t_{as}$	0		0		0		ns
Write Recovery Time	$t_{wr}$	5		5		5		ns
Write Enable to Output Low-Z <sup>*1</sup>	$t_{wlz}$	5		5		5		ns
Write Enable to Output High-Z <sup>*1</sup>	$t_{whz}$		30		35		40	ns

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WRITE CYCLE TIMING DIAGRAM <sup>\*2</sup>

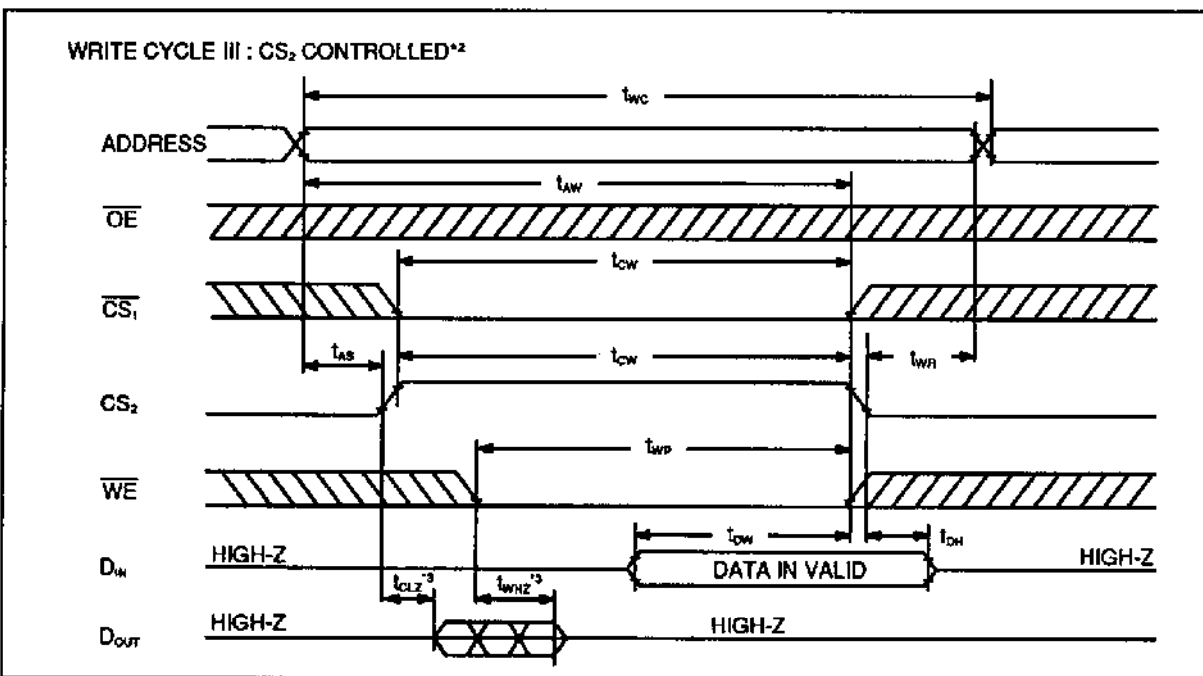
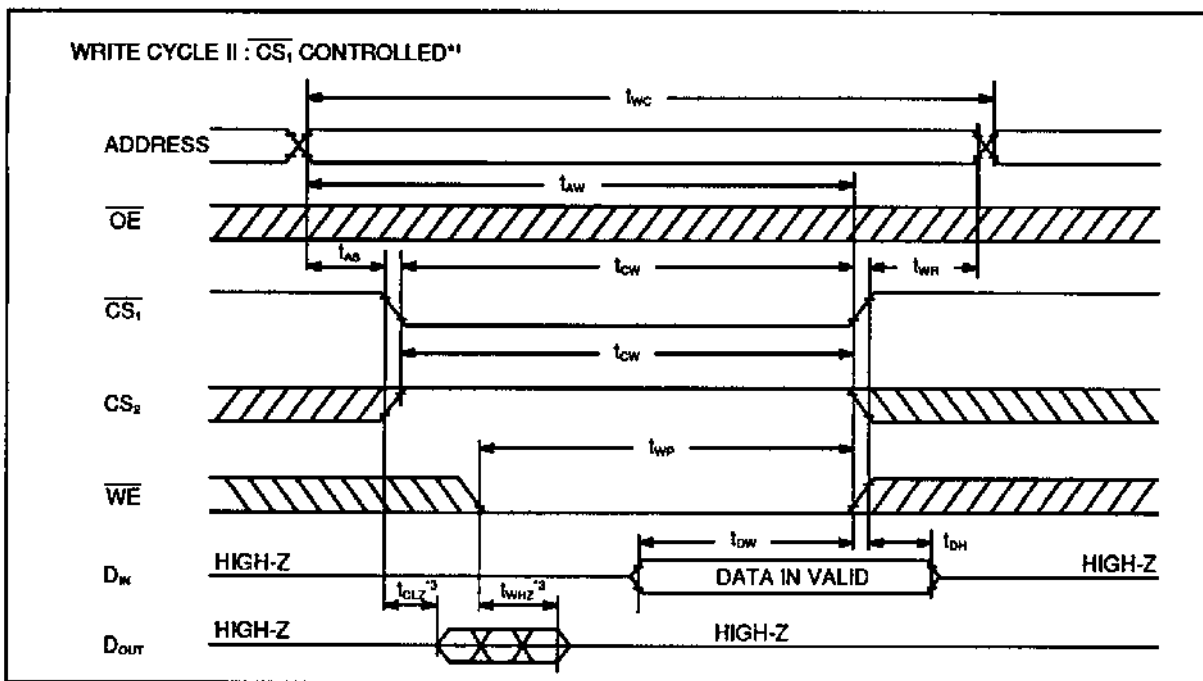
Note: <sup>\*1</sup> Transition is measured at the point of  $\pm 500\text{mV}$  from steady state voltage.

<sup>\*2</sup> If  $\overline{OE}$ ,  $\overline{CS}_1$  and  $\overline{CS}_2$  are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

MB8464A-80/80L/80LL  
 MB8464A-10/10L/10LL  
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- Note:**
- \*1 If  $\overline{OE}$ ,  $\overline{CS}_2$  and  $\overline{WE}$  are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
  - \*2 If  $\overline{OE}$ ,  $\overline{CS}_1$  and  $\overline{WE}$  are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
  - \*3 Transition is measured at the point of  $\pm 500\text{mV}$  from steady state voltage.

MB8464A-80/80L/80LL  
 MB8464A-10/10L/10LL  
 MB8464A-15/15L/15LL

# DATA RETENTION CHARACTERISTICS

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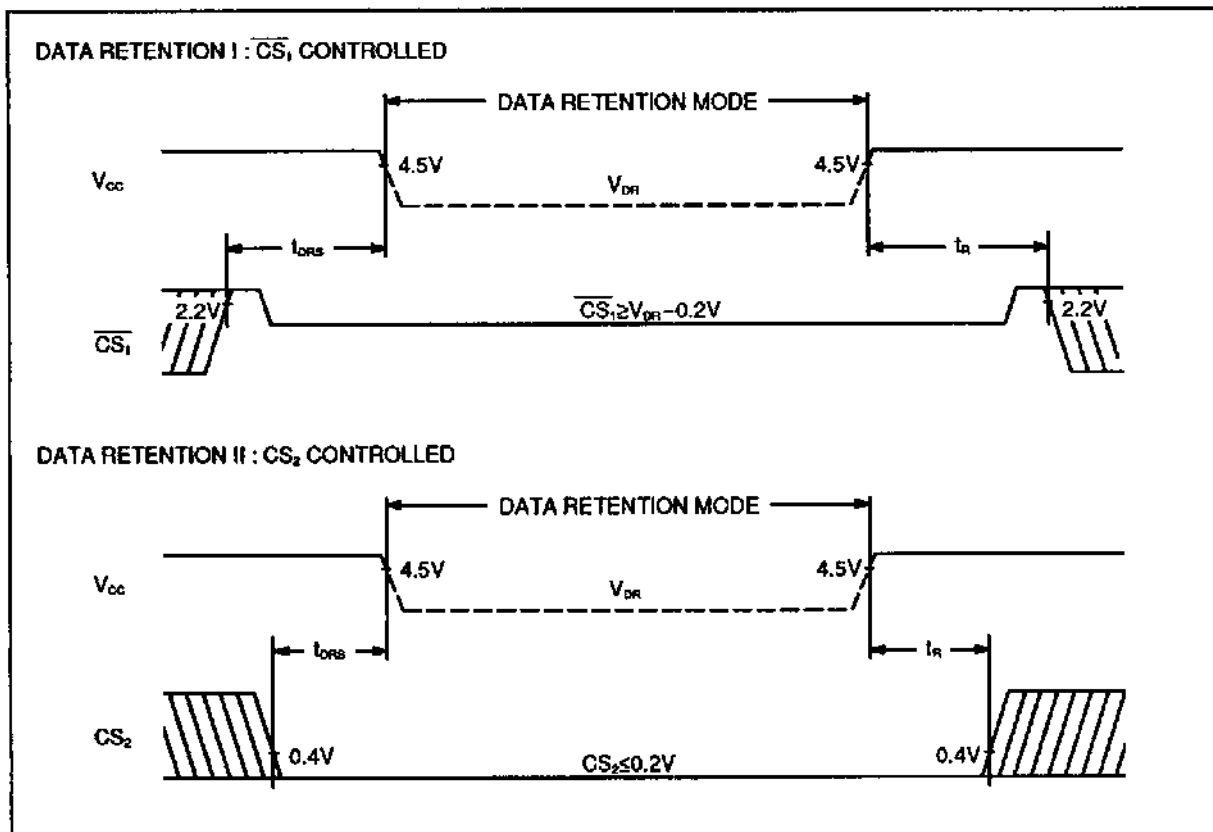
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage	$V_{DR}$	2.0		5.5	V
Data Retention Supply Current*2	Standard			1.0	mA
	L-Version		1.0	25	$\mu$ A
	LL-Version*3		1.0	2.0	$\mu$ A
Data Retention Setup Time	$t_{DRS}$	0			ns
Operation Recovery Time	$t_R$	$t_{RC}$			ns

Note: \*2  $\overline{CS}_2$  controlled:  $V_{DR}=3.0V$ ,  $CS_2 \leq 0.2V$   
 $\overline{CS}_1$  controlled:  $V_{DR}=3.0V$ ,  $\overline{CS}_1 \geq V_{DR} - 0.2V$  ( $CS_2 \leq 0.2V$  or  $CS_2 \geq V_{DR} - 0.2V$ )  
 \*3  $V_{DR}=3.0V$ ,  $T_A=0^\circ C$  to  $40^\circ C$

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## DATA RETENTION TIMING



MB8464A-80/80L/80LL  
 MB8464A-10/10L/10LL  
 MB8464A-15/15L/15LL

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## TYPICAL CHARACTERISTICS CURVES

Fig. 3 - NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

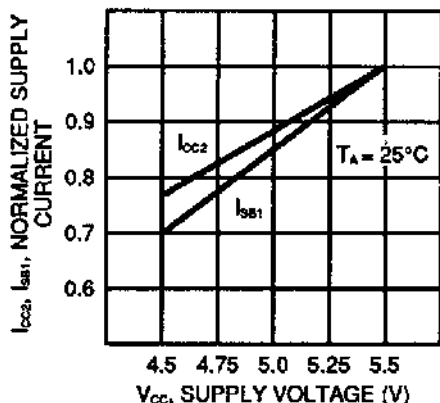


Fig. 4 - NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

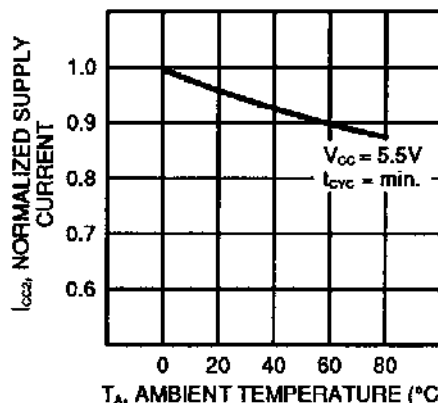


Fig. 5 - NORMALIZED POWER SUPPLY CURRENT vs. CYCLE TIME

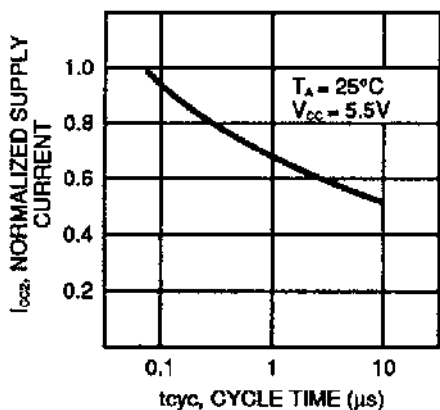


Fig. 6 - NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

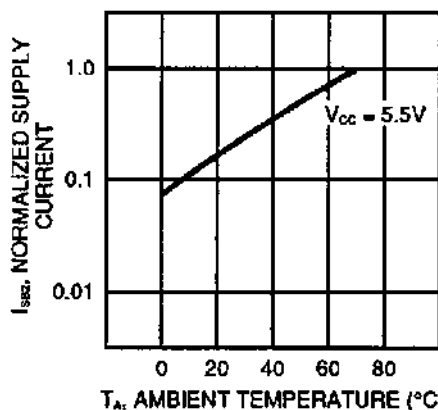


Fig. 7 - NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

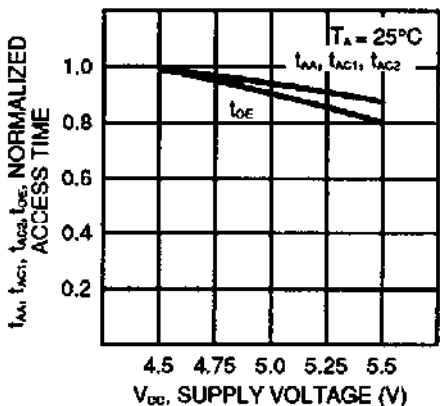
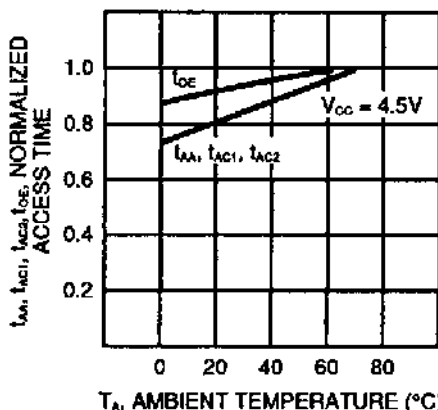


Fig. 8 - NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



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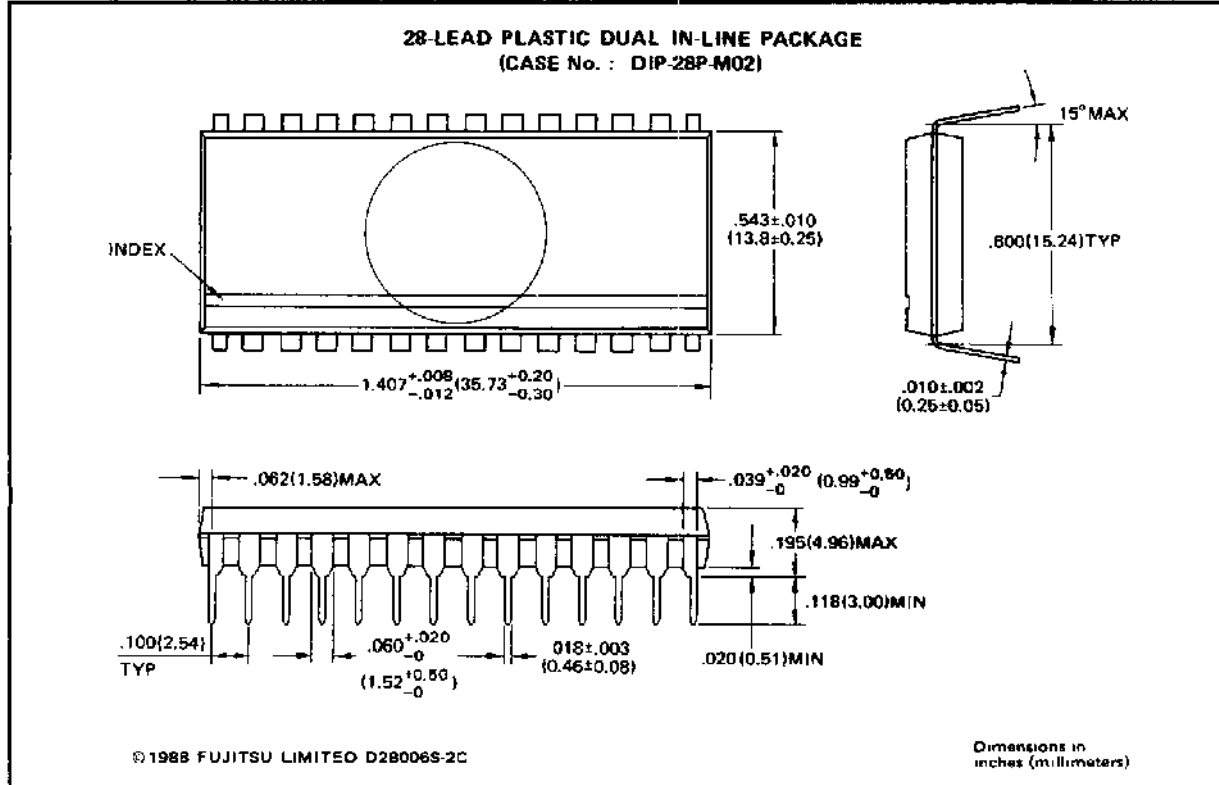


MB8464A-80/80L/80LL  
 MB8464A-10/10L/10LL  
 MB8464A-15/15L/15LL

**PACKAGE DIMENSIONS**

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(Suffix: P)



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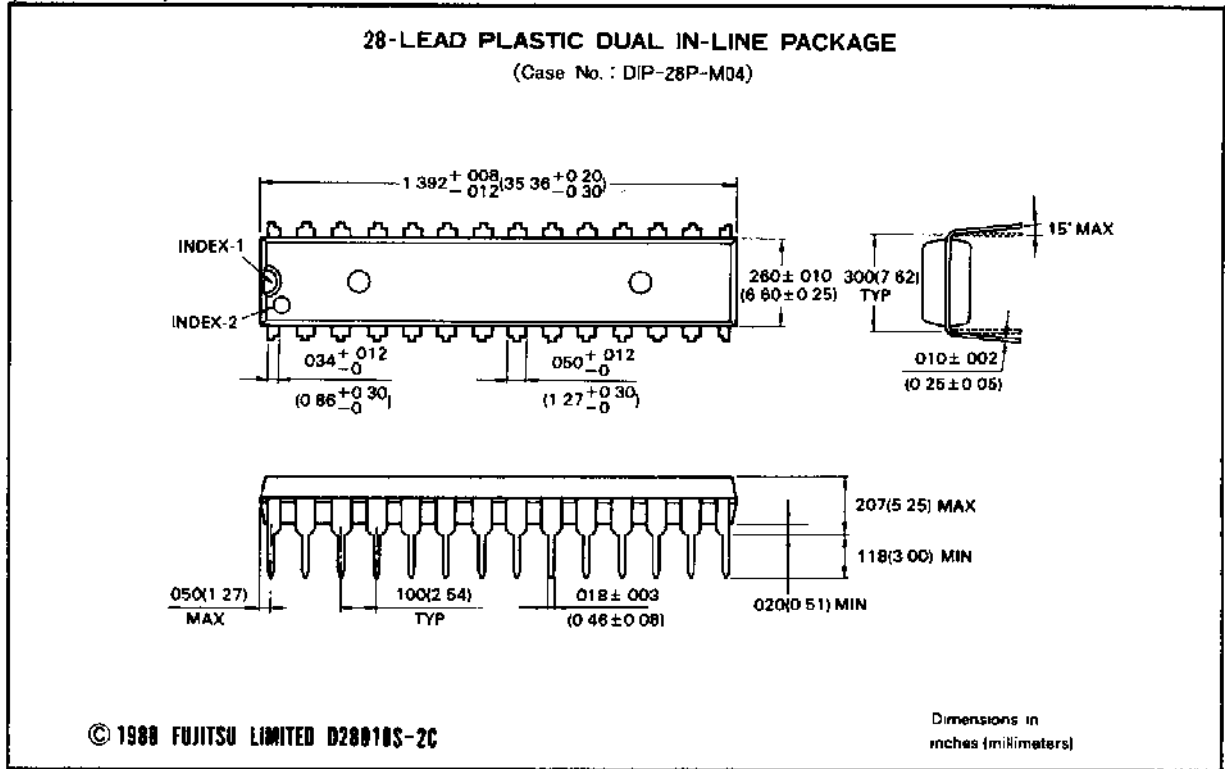


MB8464A-80/80L/80LL  
 MB8464A-10/10L/10LL  
 MB8464A-15/15L/15LL

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# PACKAGE DIMENSIONS

(Suffix: P-SK)



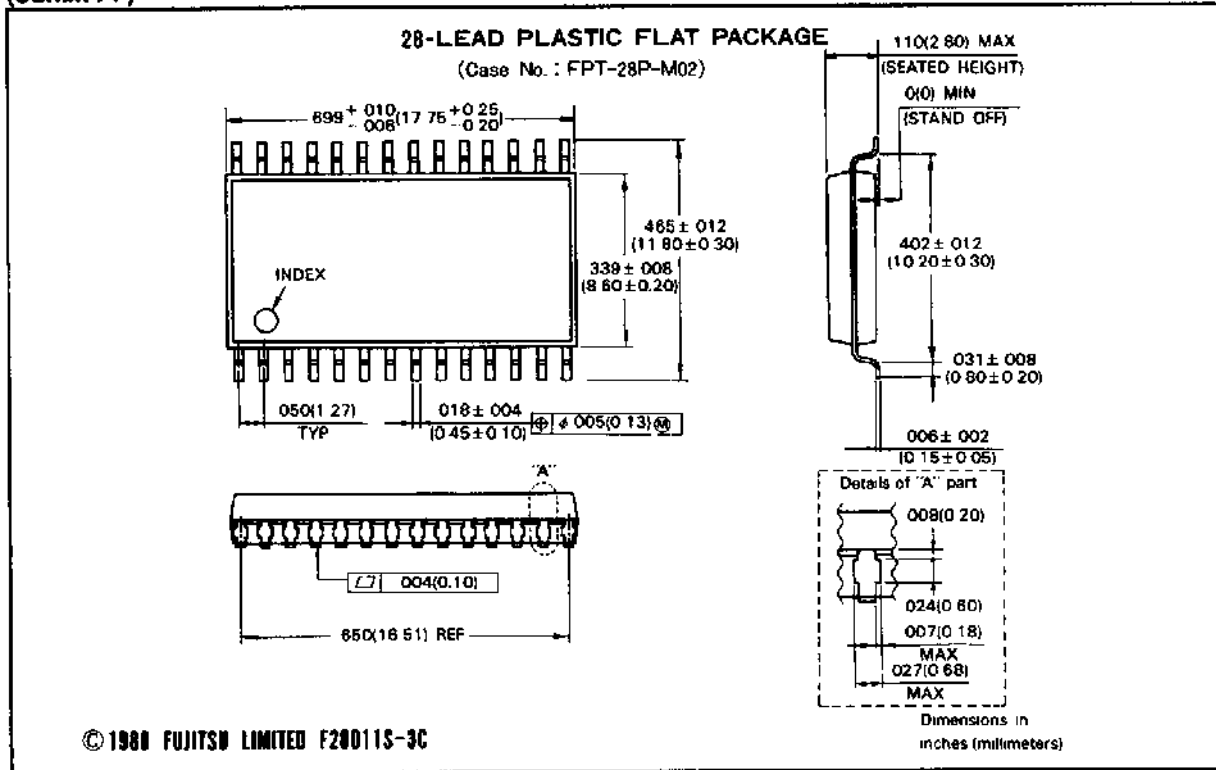
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MB8464A-80/80L/80LL  
 MB8464A-10/10L/10LL  
 MB8464A-15/15L/15LL

**PACKAGE DIMENSIONS (Cont'd)**

T-46-23-12

(Suffix: PF)



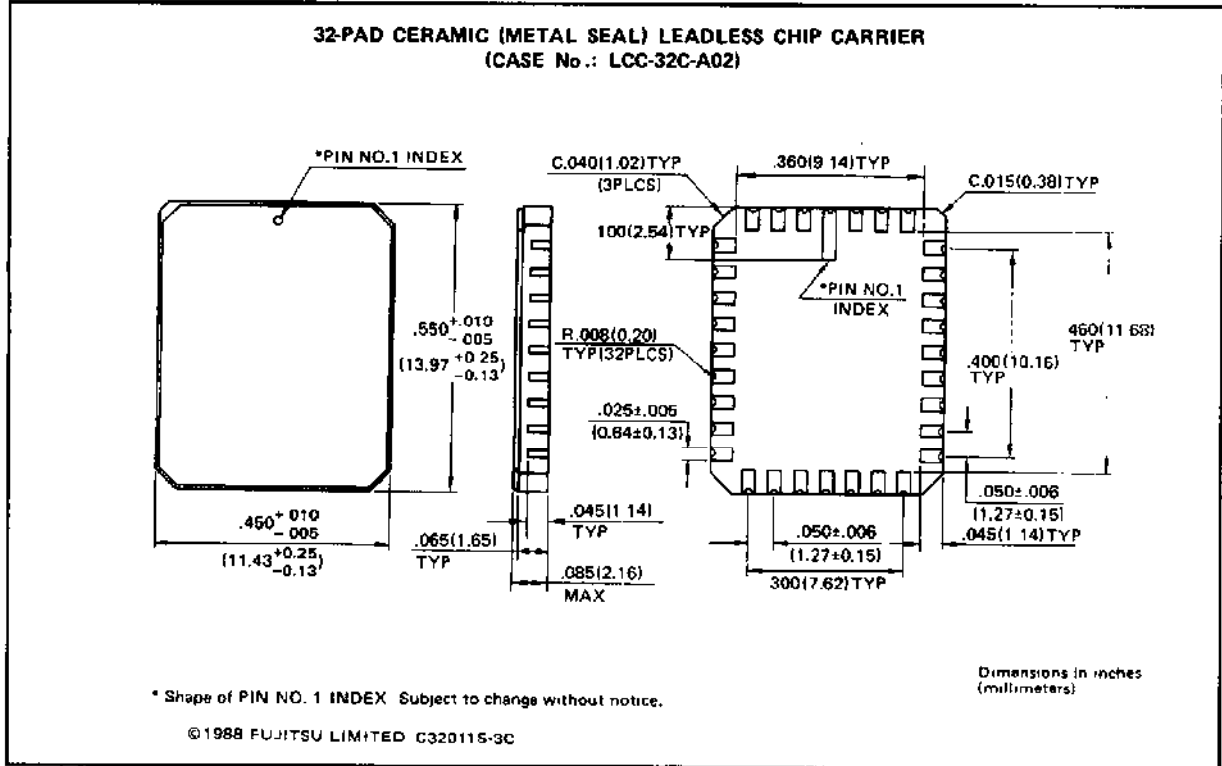
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MB8464A-80/80L/80LL  
 MB8464A-10/10L/10LL  
 MB8464A-15/15L/15LL

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### PACKAGE DIMENSIONS (Cont'd)

(Suffix: CV)



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