M5M5257CP,J-15,-20,-25,-35, -20L,-25L,-35L

262144-BIT (262144-WORD BY 1-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5257C is a family of 262144-word by 1-bit static RAMs, fabricated with the high-performance CMOS silicongate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5257CP,J-15 ····· 15ns(max)
  M5M5257CP,J-20,-20L ····· 20ns(max)
  M5M5257CP,J-25,-25L ····· 25ns(max)
  M5M5257CP,J-35,-35L ····· 35ns(max)
- Low power dissipation
  Active ····· 300mW(typ)
  Stand by(-15,-20,-25,-35) ····· 5mW(typ)
  Stand by(-20L,-25L,-35L) ··· 50μW(typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- All address inputs are changeable with each other

APPLICATION

High-speed memory systems

FUNCTION

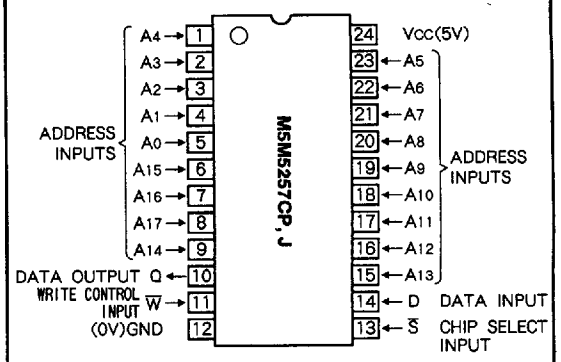
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the Q terminal is maintained in the high impedance state, so it is possible to connect D and Q terminals directly.

In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low if the address signals are stable, the data is available at the Q terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

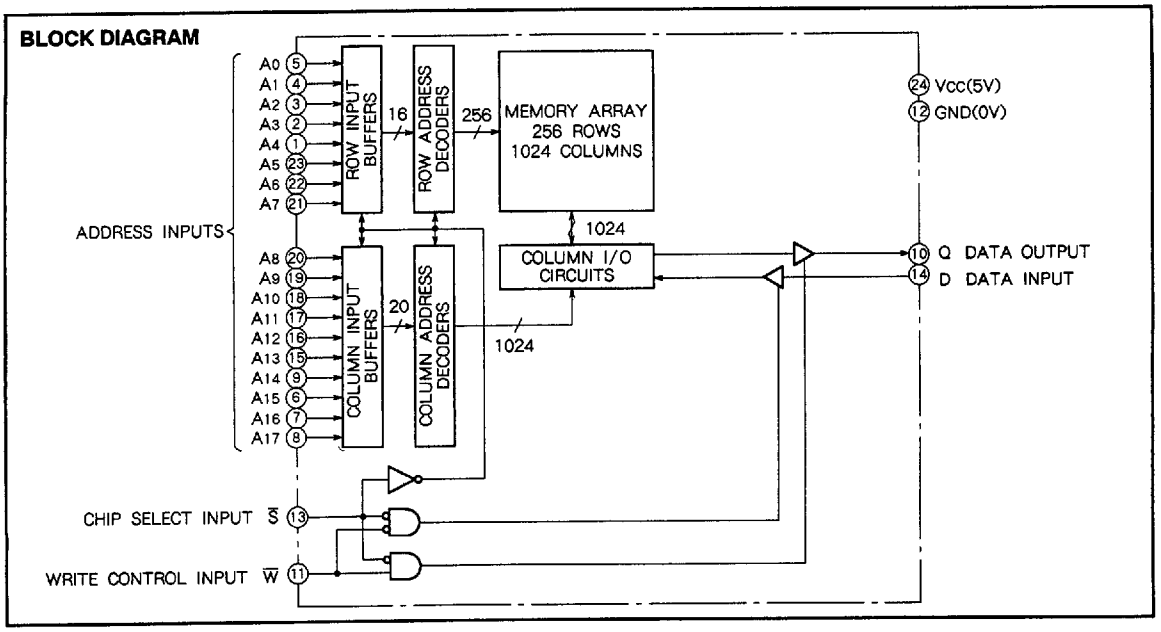
Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4Y(P)
24P0J(J)

BLOCK DIAGRAM



MODE SELECTION

$\overline{S}$	$\overline{W}$	Mode	Data input	Data output	Icc
H	X	Non selection	High-impedance	High-impedance	Stand by
L	L	Write	Din	High-impedance	Active
L	H	Read	High-impedance	Dout	Active

H : V_{IH} L : V_{IL} X : V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 3.5 * ~7	V
V_I	Input voltage		− 3.5 * ~7	V
V_O	Output voltage		− 3.5 * ~7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0~70	℃
$T_{stg(bias)}$	Storage temperature(bias)		− 10~85	℃
T_{stg}	Storage temperature		− 65~150	℃

* Pulse width ≦ 10ns, In case of DC : − 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3	V
V_{IL}	Low-level input voltage			− 0.5 *		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0~Vcc				2	μA
| I_{OZ} |	Off-state output current	$V_{I(\overline{S})} = V_{IH}$, V_O = 0~Vcc				10	μA
I_{CC1}	Supply current from Vcc	$V_{I(\overline{S})} = V_{IL}$ Output open	AC(15ns cycle)			130	mA
			AC(20,25,35ns cycle)			120	
			DC		60	75	
I_{CC2}	Stand by current	$V_{I(\overline{S})} = V_{IH}$	AC(15ns cycle)			50	mA
			AC(20,25,35ns cycle)			40	
			Other $V_I \geqq V_{IH}$ or $\leqq V_{IL}$			30	
I_{CC3}	Stand by current	$V_{I(\overline{S})} = V_{CC} - 0.2V$ Other $V_I \leqq 0.2V$ or $V_I \geqq V_{CC} - 0.2V$	-15,-20,-25,-35		1	10	mA
			-20L,-25L,-35L		10	100	μA

Note 1. Current flow into an IC is positive, out is negative.
* − 3.0V in case of AC (Pulse width ≦ 10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			5	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			7	pF

* C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3V, V_{IL} = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = V_{IL} = 1.5V
Output timing reference levels ····· V_{OH} = V_{OL} = 1.5V
Output loads ····· Fig.1, Fig.2

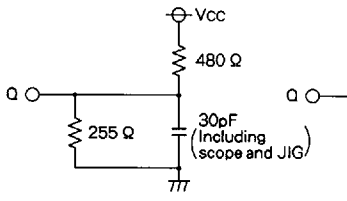


Fig.1 Output load

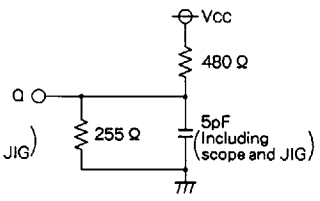


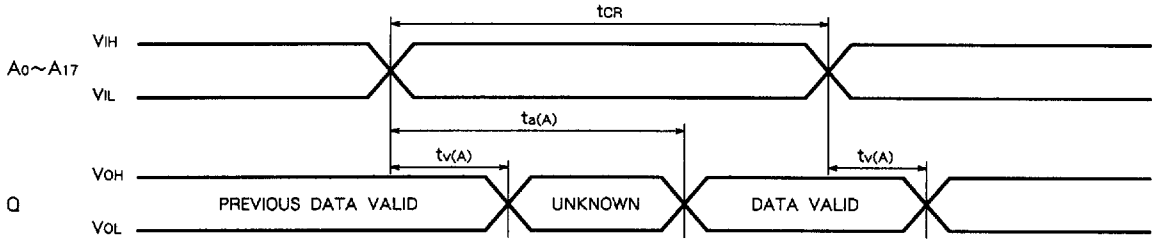
Fig. 2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

Symbol	Parameter	Limits								Unit
		M5M5257C-15		M5M5257C-20,-20L		M5M5257C-25,-25L		M5M5257C-35,-35L		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	15		20		25		35		ns
$t_{a(A)}$	Address access time		15		20		25		35	ns
$t_{a(S)}$	Chip select access time		15		20		25		35	ns
$t_{v(A)}$	Data valid time after addresses	3		3		5		5		ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	3		3		5		5		ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	7	0	8	0	10	0	10	ns
t_{PU}	Power-up time after chip selection	0		0		0		0		ns
t_{PD}	Power-down time after chip deselection		15		20		25		35	ns

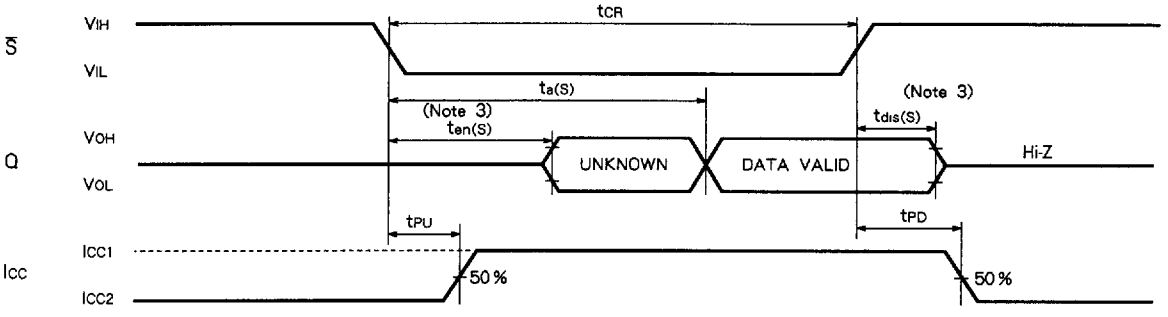
(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



$\overline{S}$ = L
$\overline{W}$ = H

Read cycle 2 (Note 2)



$\overline{W}$ = H

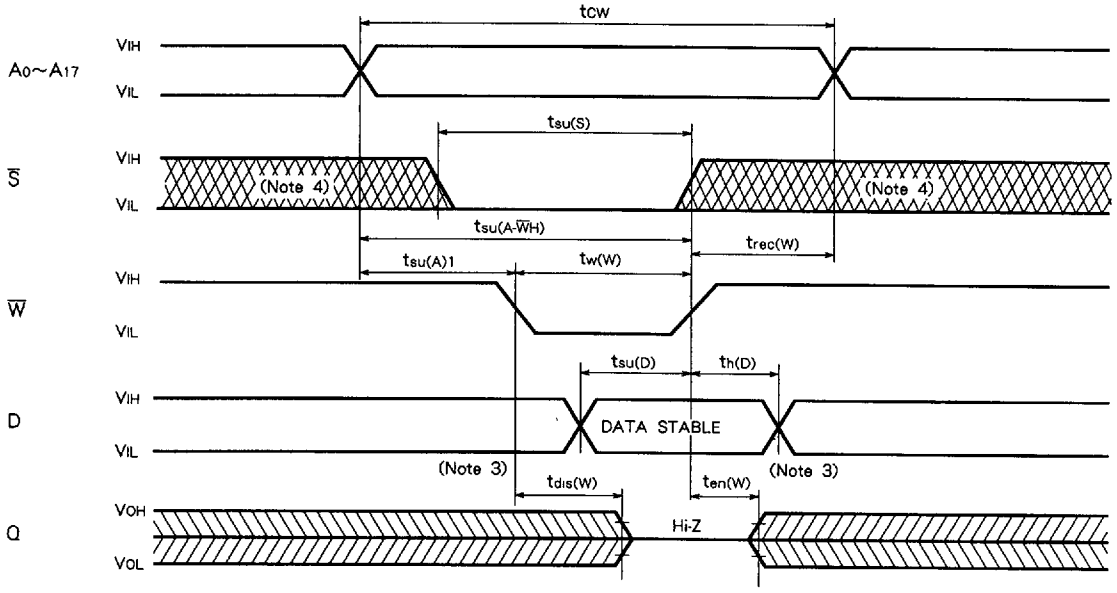
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure2.

(4) WRITE CYCLE

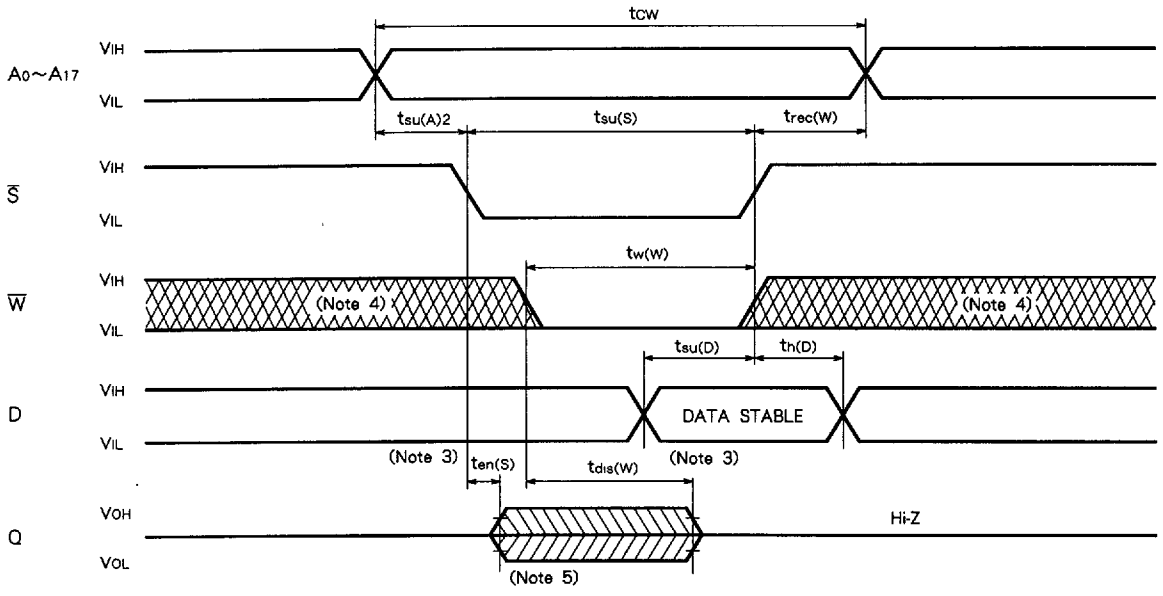
Symbol	Parameter	Limits								Unit
		M5M5257C-15		M5M5257C-20,-20L		M5M5257C-25,-25L		M5M5257C-35,-35L		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	15		20		25		35		ns
$t_{su(S)}$	Chip select setup time	12		15		20		30		ns
$t_{su(A)1}$	Address setup time 1($\overline{W}$ CONTROL)	0		0		0		0		ns
$t_{su(A)2}$	Address setup time 2($\overline{S}$ CONTROL)	0		0		0		0		ns
$t_{w(W)}$	Write pulse width	12		15		20		25		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		ns
$t_{su(D)}$	Data setup time	7		8		10		15		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	7	0	8	0	10	0	10	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	12		15		20		30		ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.
6. ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
$V_{CC(PD)}$	Power down supply voltage	$V_{I(\overline{S})} \geq V_{CC} - 0.2V$, $V_I \geq V_{CC} - 0.2V$ or $0V \leq V_I \leq 0.2V$		2			V
$V_{I(\overline{S})}$	Chip select input voltage			Vcc-0.2			V
$t_{su(PD)}$	Power down setup time			0			ns
$t_{rec(PD)}$	Power down recovery time		-20L	20			ns
			-25L	25			
			-35L	35			
$I_{CC(PD)}$	Power down supply current	Vcc = 3.0V				50	μA
		Vcc = 5.5V				100	

Note 6. This is only M5M5257CP,J-20L,-25L,-35L.

TIMING WAVEFORM FOR POWER DOWN