M5M44100AWJ,J,L,TP,RT-6,-7,-8,-10

FAST PAGE MODE 4194304-BIT(4194304-WORD BY 1-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 1-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

The M5M44100ATP, RT are packaged in a 26-pin very thin and small outline package which is a high reliability and high density surface mount device. Two types of devices are available. M5M44100ATP(normal lead bend type package), M5M44100ART(reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ.mW)
M5M44100AXX-6	60	15	30	120	400
M5M44100AXX-7	70	20	35	140	350
M5M44100AXX-8	80	20	40	160	300
M5M44100AXX-10	100	25	50	190	250

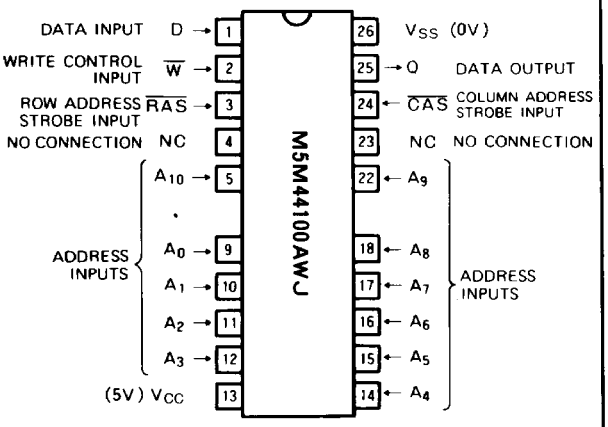
XX=WJ, J, L, TP, RT

- Standard 26 pin SOJ, 20 pin ZIP, 26 pin TSOP
- Single 5V ± 10% supply
- Low stand-by power dissipation
  5.5mW (Max) . . . . . CMOS Input level
- Low operating power dissipation
  M5M44100Axx-6 . . . . . 550.0mW (Max)
  M5M44100Axx-7 . . . . . 467.5mW (Max)
  M5M44100Axx-8 . . . . . 412.5mW (Max)
  M5M44100Axx-10 . . . . . 357.5mW (Max)
- Fast-page mode (2048-bit random access), Read-modify-write, $\overline{RAS}$-only refresh $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write operation gives common I/O capability
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms ($A_0 \sim A_9$)
- 16-bit parallel test mode capability

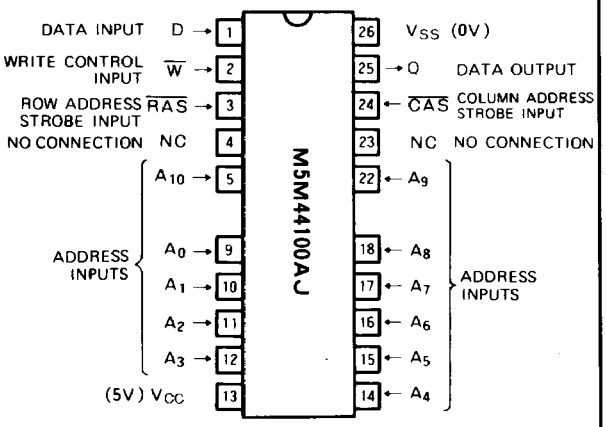
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

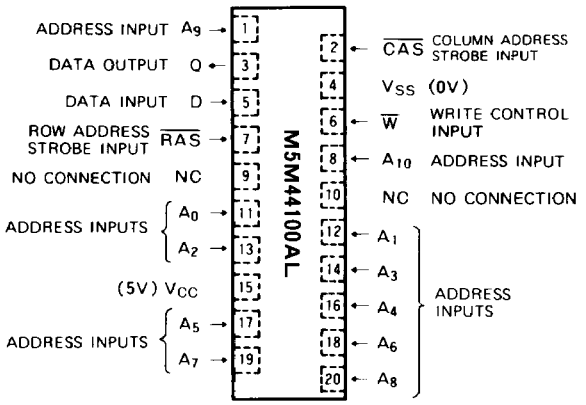
PIN CONFIGURATION (TOP VIEW)



Outline 26P0Z (350 mil SOJ)



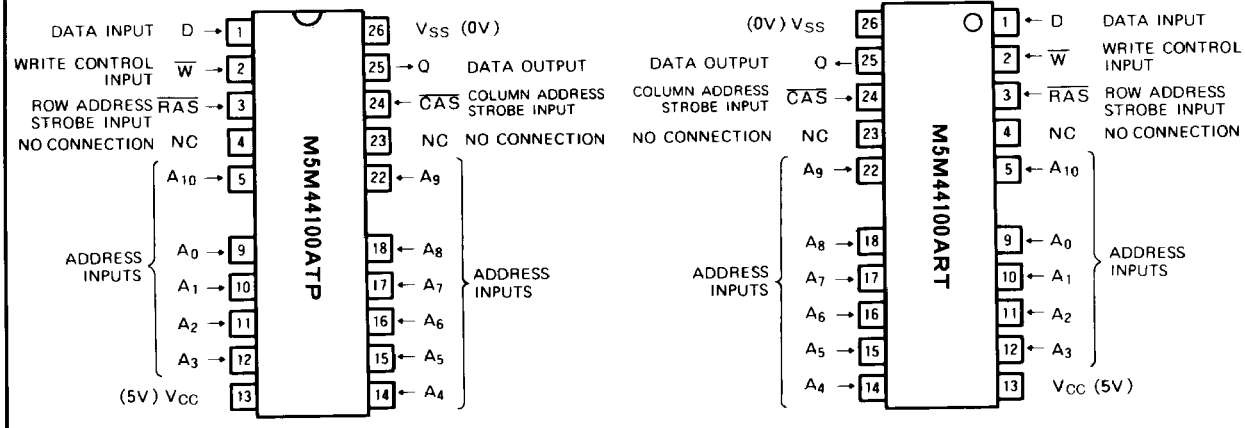
Outline 26P0J (300 mil SOJ)



Outline 20P5L-B (ZIP)

FAST PAGE MODE 4194304-BIT(4194304-WORD BY 1-BIT)DYNAMIC RAM

PIN CONFIGURATION (TOP VIEW)



Outline 26P3Z (TSOP) Outline 26P3Z (TSOP)

FUNCTION

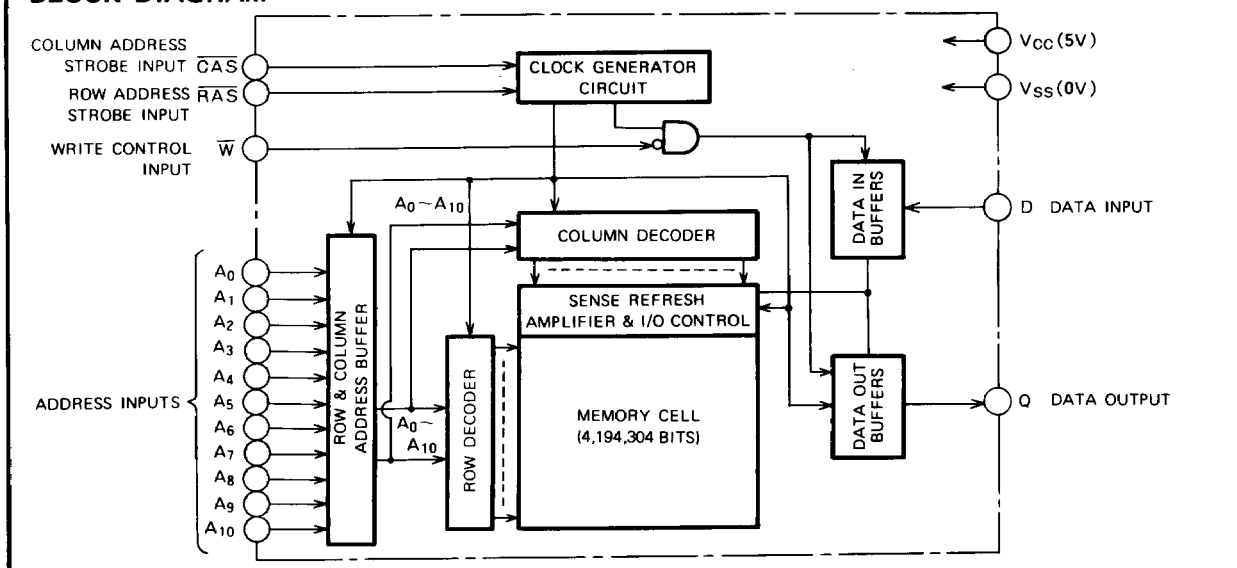
The M5M44100AWJ, J, L, TP, RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	VLD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, IVD: invalid, APD: applied, OPN: open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FAST PAGE MODE 4194304-BIT(4194304-WORD BY 1-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5, Other input pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M44100A-6	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min. output open			100	mA
		M5M44100A-7				85	
		M5M44100A-8				75	
		M5M44100A-10				65	
I_{CC2}	Supply current from V_{CC}, stand-by (Note 5)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧V_{CC}−0.5, output open			1	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M44100A-6	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min. output open			100	mA
		M5M44100A-7				85	
		M5M44100A-8				75	
		M5M44100A-10				65	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4)	M5M44100A-6	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min. output open			100	mA
		M5M44100A-7				85	
		M5M44100A-8				75	
		M5M44100A-10				65	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44100A-6	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min. output open			85	mA
		M5M44100A-7				75	
		M5M44100A-8				65	
		M5M44100A-10				55	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M44100AWJ, J, TP, RT	V_I=V_{SS} f=1MHz V_i=25mVrms			5	pF
		M5M44100AL				6	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(\overline{W})}$	Input capacitance, write control input					7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input					7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input					7	pF
C_O	Output capacitance		V_O=V_{SS}, f=1MHz, V_i=25mVrms			7	pF

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Notes 5, 12, 13)

Symbol	Parameter		Limits								Unit
			M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		15		20		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		60		70		80		100	ns
t_{AA}	Column address access time	(Note 6, 9)		30		35		40		50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		35		40		45		55	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	0	20	0	20	0	25	ns

Note 5: An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

8: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.

9: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

10: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

11: $t_{OFF(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq |\pm 10\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Notes 12, 13)

Symbol	Parameter		Limits								Unit
			M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			16.4		16.4		16.4		16.4	ms
t_{RP}	$\overline{RAS}$ high pulse width		50		60		70		80		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	20	45	20	50	20	60	25	75	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 15)	15	30	15	35	15	40	20	50	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	0	15	0	20	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		10		10		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		15		15		20		ns
t_T	Transition time	(Note 17)	1	50	1	50	1	50	1	50	ns

Note 12: The timing requirements are assumed t_T = 5ns.

13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.

15: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

16: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

17: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits								Unit
			M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		120		140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		20		25		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 18)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 18)	10		10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		30		35		40		50		ns

Note 18: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter		Limits								Unit
			M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		120		140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		20		25		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 21)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		15		15		20		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		20		25		ns
t_{WP}	Write pulse width		10		15		15		20		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits								Unit
			M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write cycle time	(Note 19)	140		165		185		220		ns
t_{RMWC}	Read modify write cycle time	(Note 20)	140		165		185		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width		85	10000	95	10000	105	10000	130	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		40	10000	45	10000	45	10000	55	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		85		95		105		130		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		40		45		45		55		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 21)	15		20		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 21)	60		70		80		100		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 21)	30		35		40		50		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		20		25		ns
t_{WP}	Write pulse width		10		15		15		20		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		10		15		15		20		ns

Note 19: t_{RWC} is specified as $t_{RWC(min)} = t_{RCD(max)} + t_{CWD(min)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
20: t_{RMWC} is specified as $t_{RMWC(min)} = t_{RAC(max)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
21: t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} do not define the limits of operation, but are included as electrical characteristics only.
When $t_{WCS} \geqq t_{WCS(min)}$, an early-write cycle is performed, and the data output keeps the high-impedance state. When $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), a read-write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above condition (delayed write) is satisfied, the condition of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indetermnate.

Fast Page Mode Cycle (Read, Write, Read-Write and Read-Modify-Write Cycles) (Note 22)

Symbol	Parameter		Limits								Unit
			M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		50		60		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		60		70		75		90		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note 23)	105	200000	115	200000	130	200000	160	200000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 24)	10	15	10	20	10	20	10	25	ns
t_{CPPH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		45		55		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 21)	35		40		45		55		ns

Note 22: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
23: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
24: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 25)

Symbol	Parameter	Limits								Unit
		M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		15		20		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		15		20		ns
t_{CAS}	$\overline{CAS}$ low pulse width	25		30		30		35		ns

Note 25: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

TEST MODE SPECIFICATION (Note 26)

ELECTRICAL CHARACTERISTICS ($Ta=0\sim70℃$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M44100A-6	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}=t_{WC}=$min. output open			115	mA
		M5M44100A-7				100	
		M5M44100A-8				85	
		M5M44100A-10				75	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M44100A-6	$\overline{RAS}$ cycling, $\overline{CAS}=V_{IH}$ $t_{RC}=$min output open			115	mA
		M5M44100A-7				100	
		M5M44100A-8				85	
		M5M44100A-10				75	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4)	M5M44100A-6	$\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling $t_{PC}=$min. output open			115	mA
		M5M44100A-7				100	
		M5M44100A-8				85	
		M5M44100A-10				75	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44100A-6	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{RC}=$min. output open			100	mA
		M5M44100A-7				85	
		M5M44100A-8				75	
		M5M44100A-10				65	

Note 26: All previously specified electrical characteristics, switching characteristics and timing requirements are applicable to that of test mode.

SWITCHING CHARACTERISTICS ($Ta=0\sim70℃$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted) (Notes 5, 12, 13)

Symbol	Parameter		Limits M5M44100A-6 Min	M5M44100A-6 Max	M5M44100A-7 Min	M5M44100A-7 Max	M5M44100A-8 Min	M5M44100A-8 Max	M5M44100A-10 Min	M5M44100A-10 Max	Unit
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		20		25		25		30	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		65		75		85		105	ns
t_{AA}	Column address access time	(Note 6, 9)		35		40		45		55	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		40		45		50		60	ns

TIMING REQUIREMENTS ($Ta=0\sim70℃$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted) (Notes 12, 13)

Read and Refresh Cycles

Symbol	Parameter	Limits M5M44100A-6 Min	M5M44100A-6 Max	M5M44100A-7 Min	M5M44100A-7 Max	M5M44100A-8 Min	M5M44100A-8 Max	M5M44100A-10 Min	M5M44100A-10 Max	Unit
t_{RC}	Read cycle time	125		145		165		195		ns
t_{RAS}	$\overline{RAS}$ low pulse width	65	10000	75	10000	85	10000	105	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	25	10000	25	10000	30	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	65		75		85		105		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		25		25		30		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	35		40		45		55		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits								Unit
			M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write cycle time	(Note 19)	145		170		190		225		ns
t_{RMWC}	Read modify write cycle time	(Note 20)	145		170		190		225		ns
t_{RAS}	$\overline{RAS}$ low pulse width		90	10000	100	10000	110	10000	135	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		45	10000	50	10000	50	10000	60	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		90		100		110		135		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		45		50		50		60		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 21)	20		25		25		30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 21)	65		75		85		105		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 21)	35		40		45		55		ns

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 22)

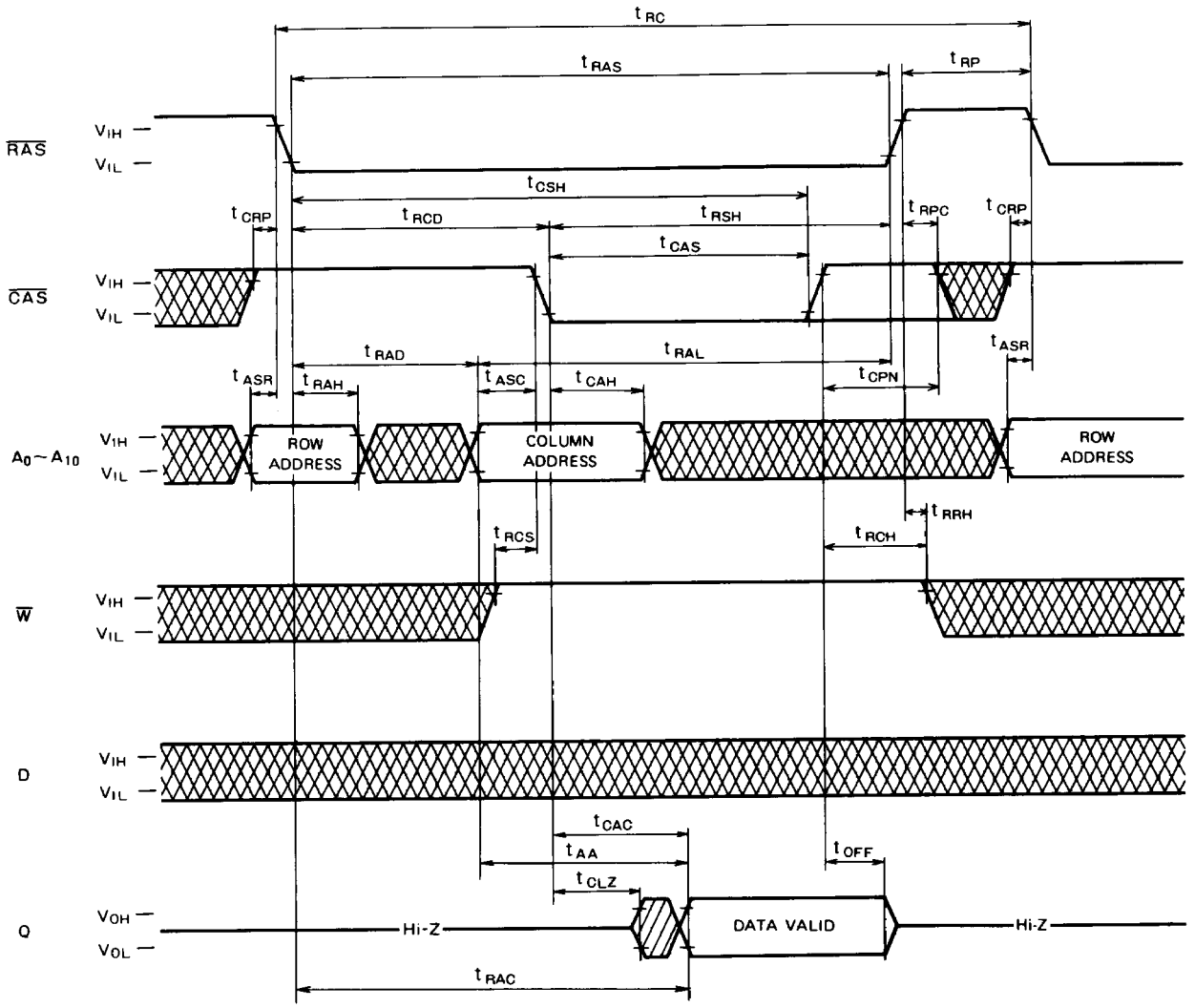
Symbol	Parameter		Limits								Unit
			M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		45		50		55		65		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		65		75		80		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note 23)	115	200000	125	200000	140	200000	170	200000	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		40		45		50		60		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 21)	40		45		50		60		ns

Test Mode Set Cycle

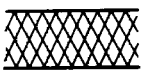
Symbol	Parameter	Limits								Unit
		M5M44100A-6		M5M44100A-7		M5M44100A-8		M5M44100A-10		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WSR}	Write setup time before $\overline{RAS}$ low	10		10		10		10		ns
t_{WHR}	Write hold time after $\overline{RAS}$ low	10		15		15		20		ns

Timing Diagrams (Note 27)

Read Cycle



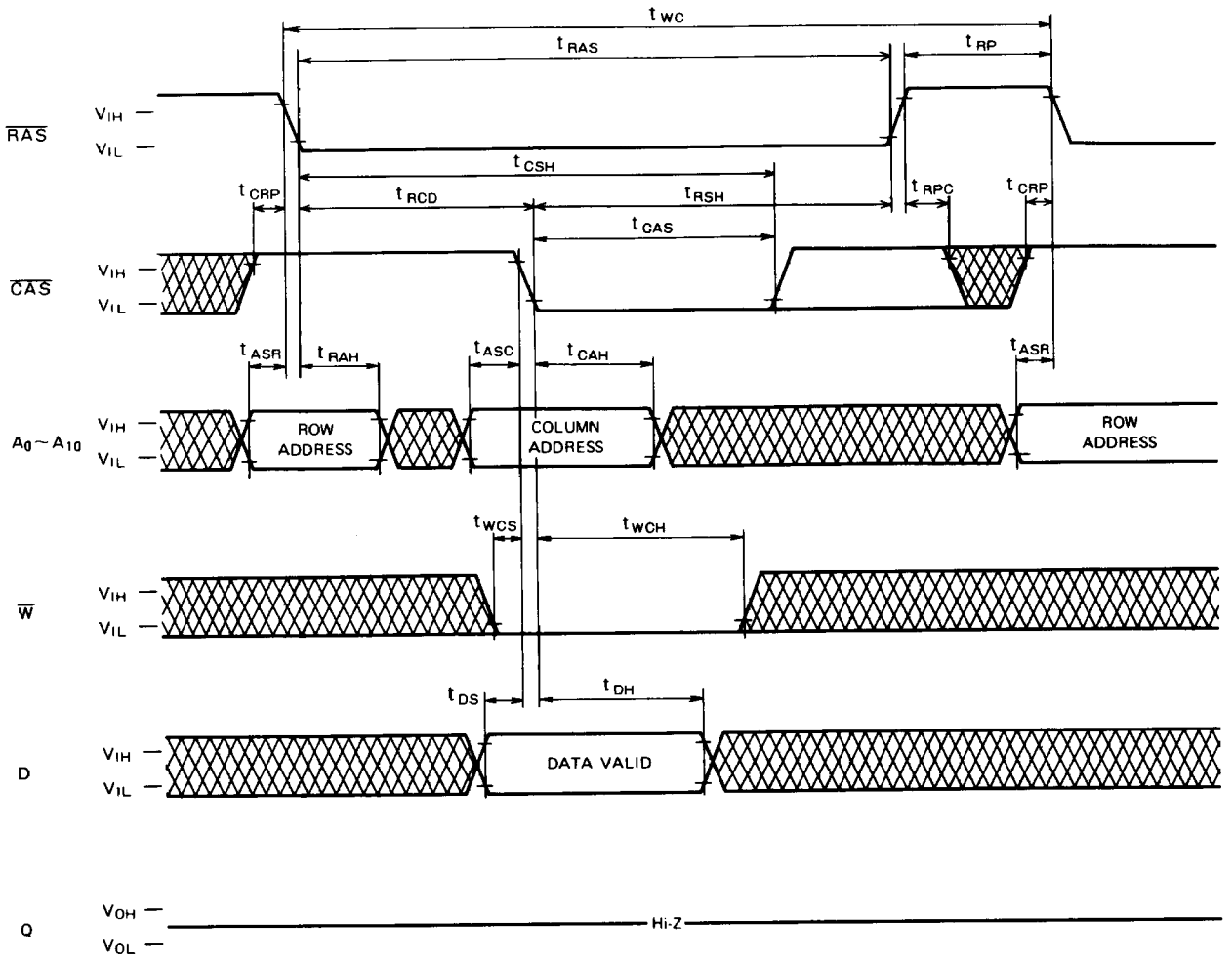
Note 27



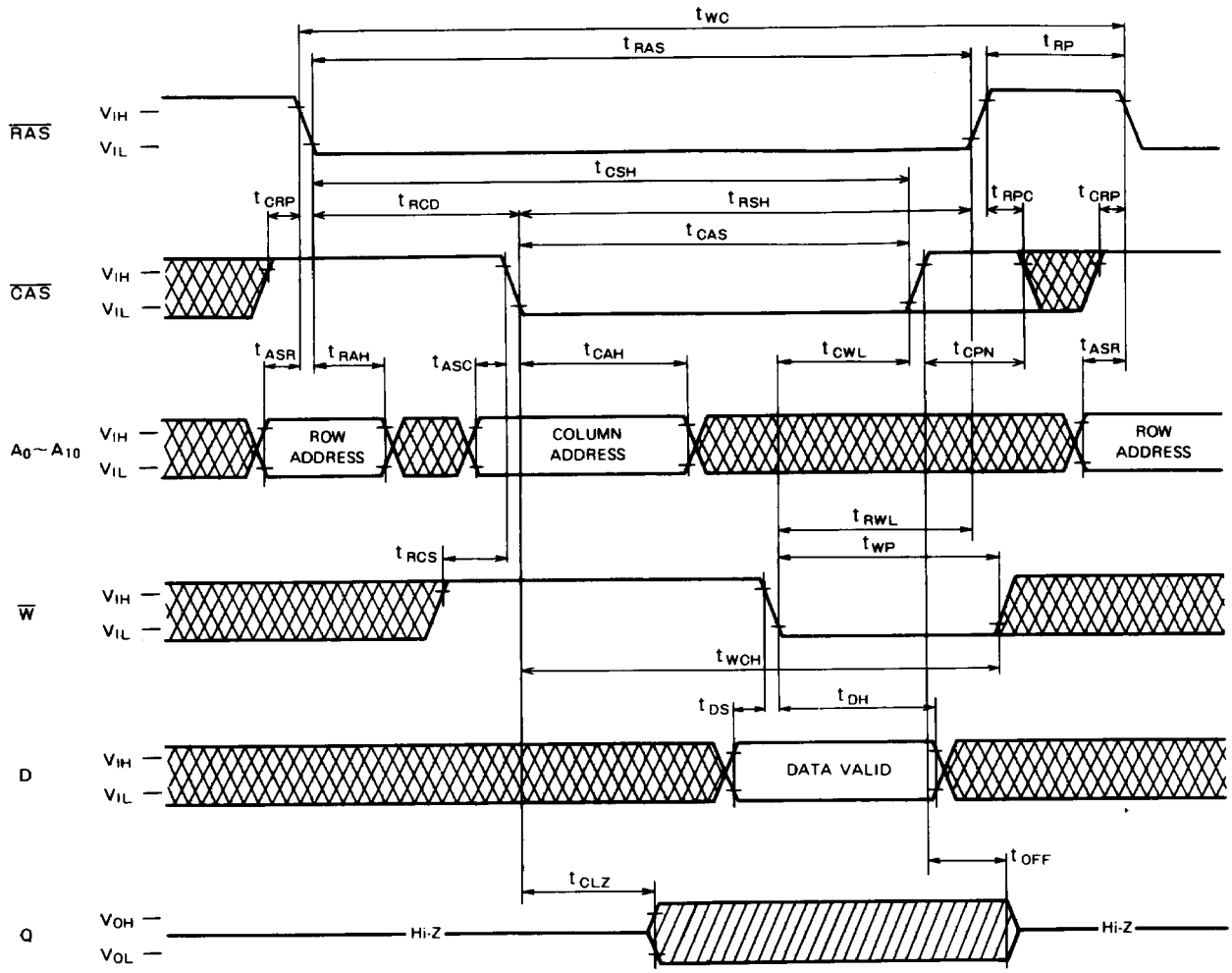
Indicates the don't care input.
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

Indicates the invalid output.

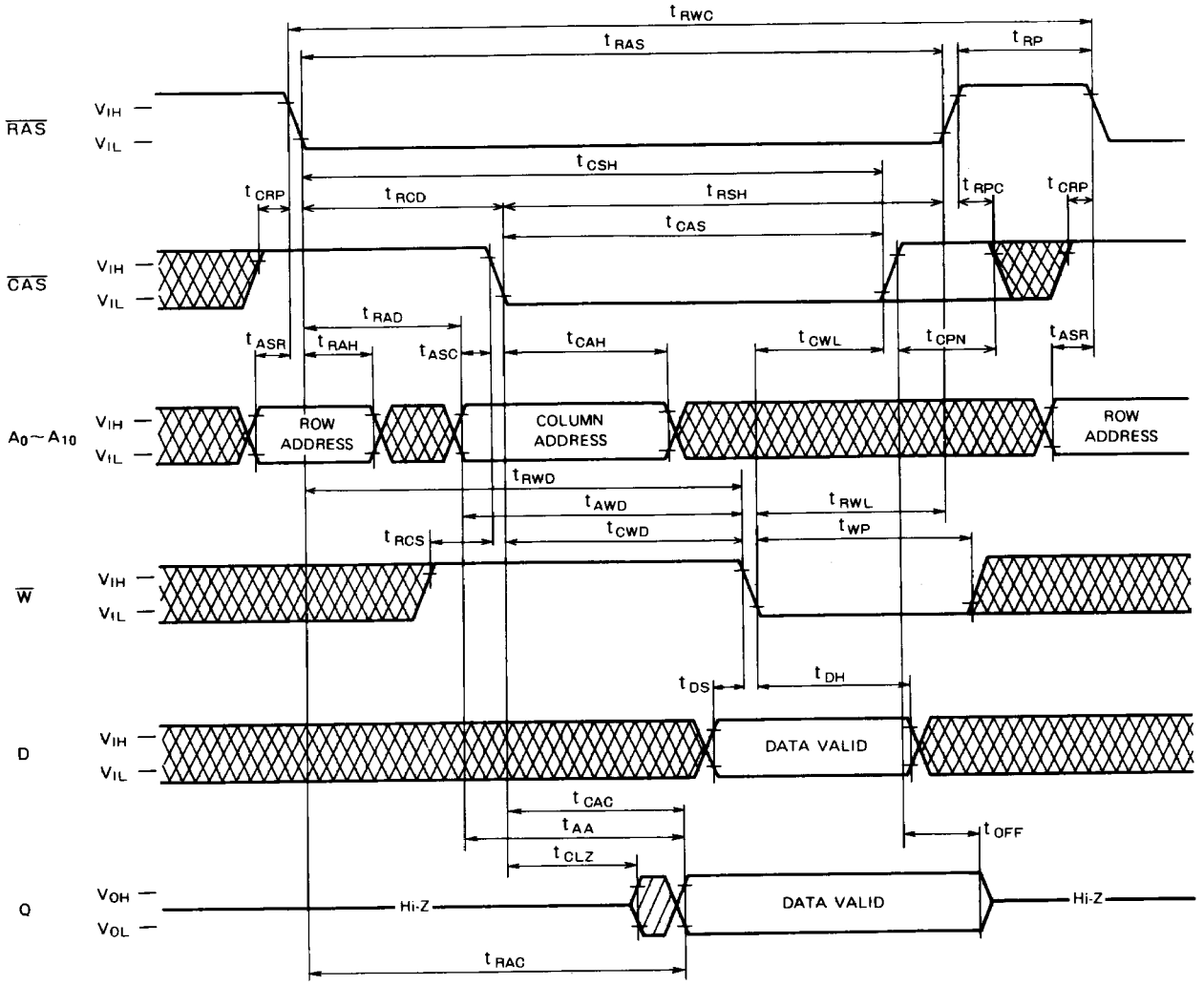
Write Cycle (Early Write)



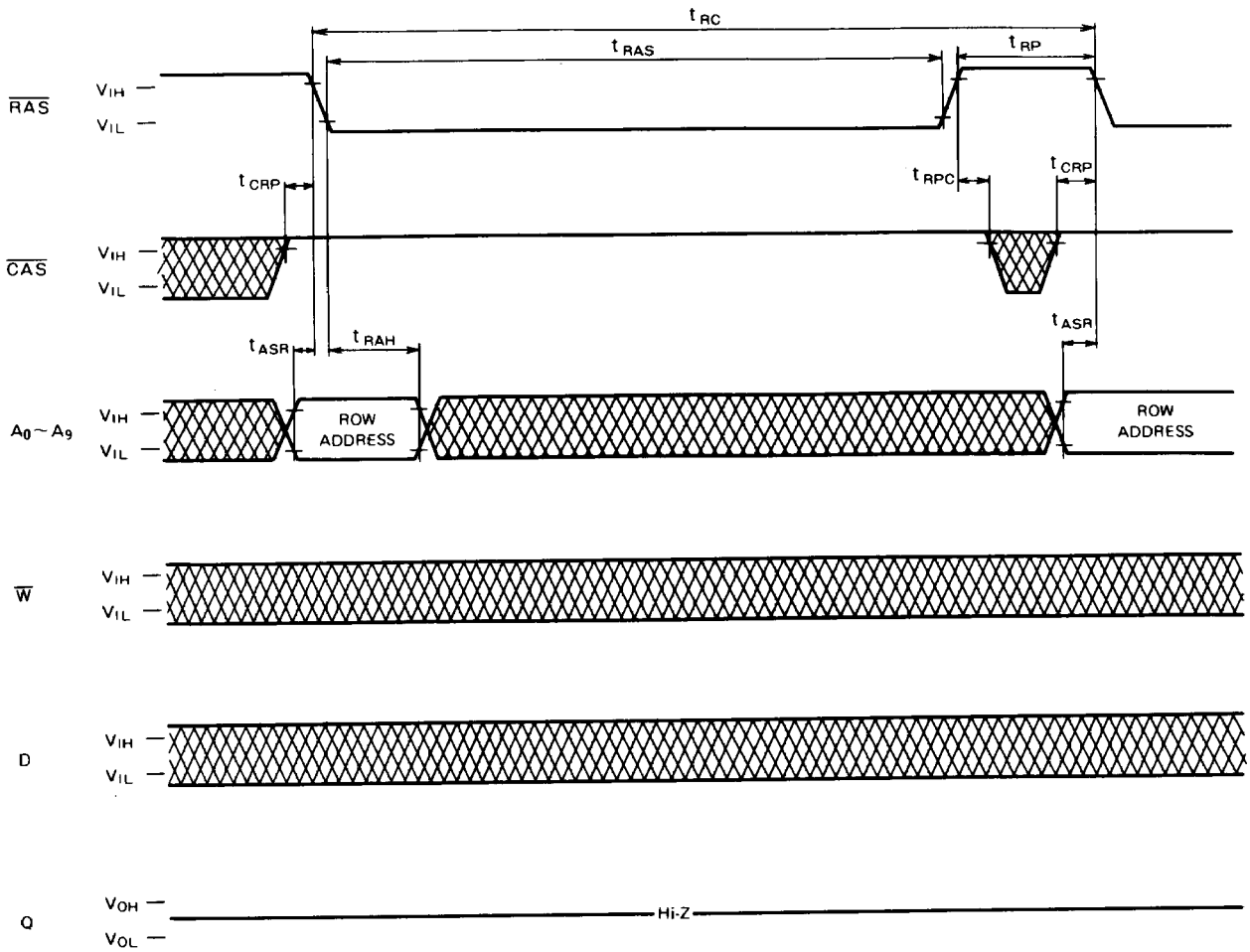
Write Cycle (Delayed Write)



Read-Write, Read-Modify-Write Cycle

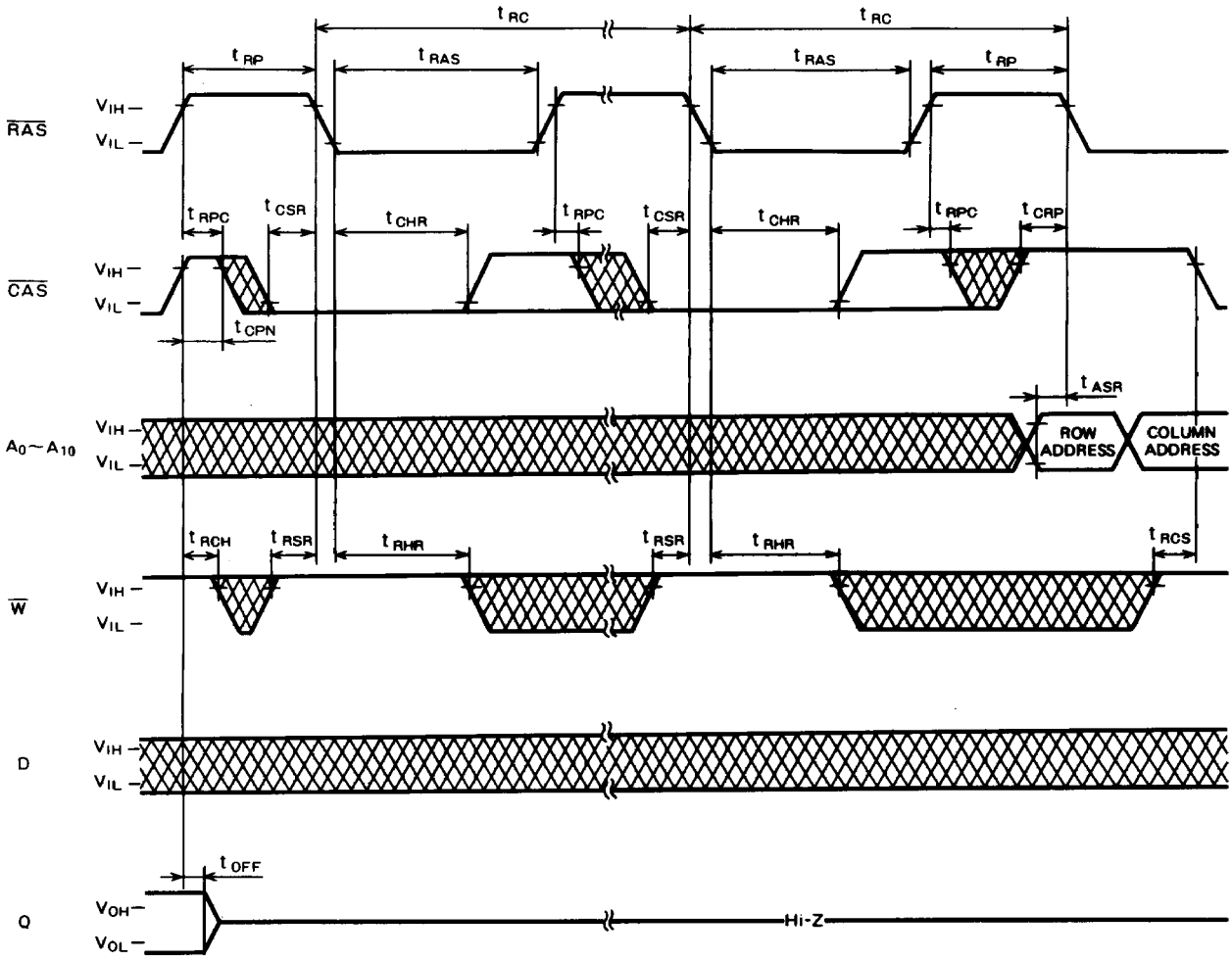


$\overline{RAS}$-only-Refresh Cycle (Note 28)

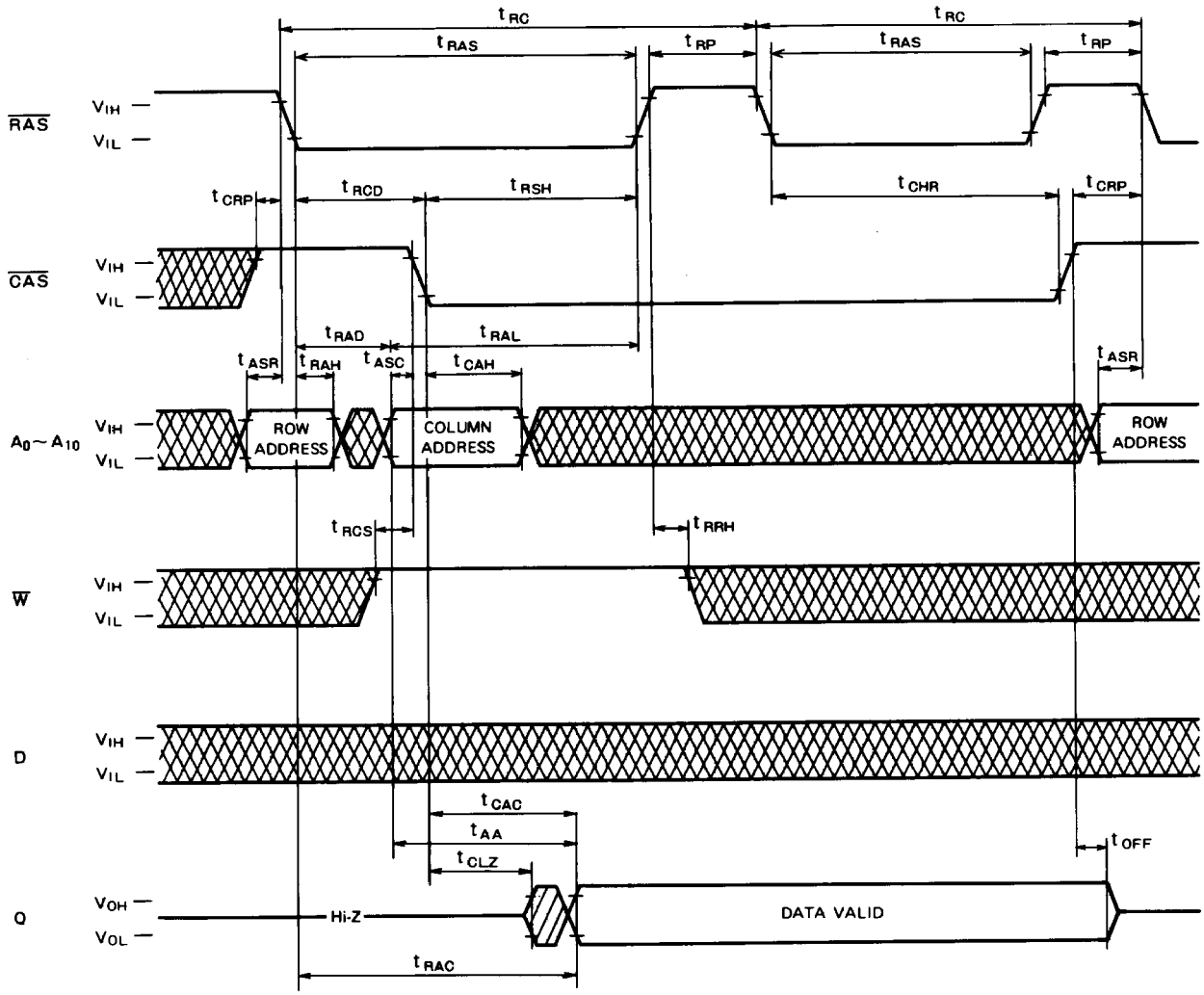


Note 28: A_{10} may be V_{IH} or V_{IL}. Refresh address: A_0 (ROW)~A_9 (ROW).

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

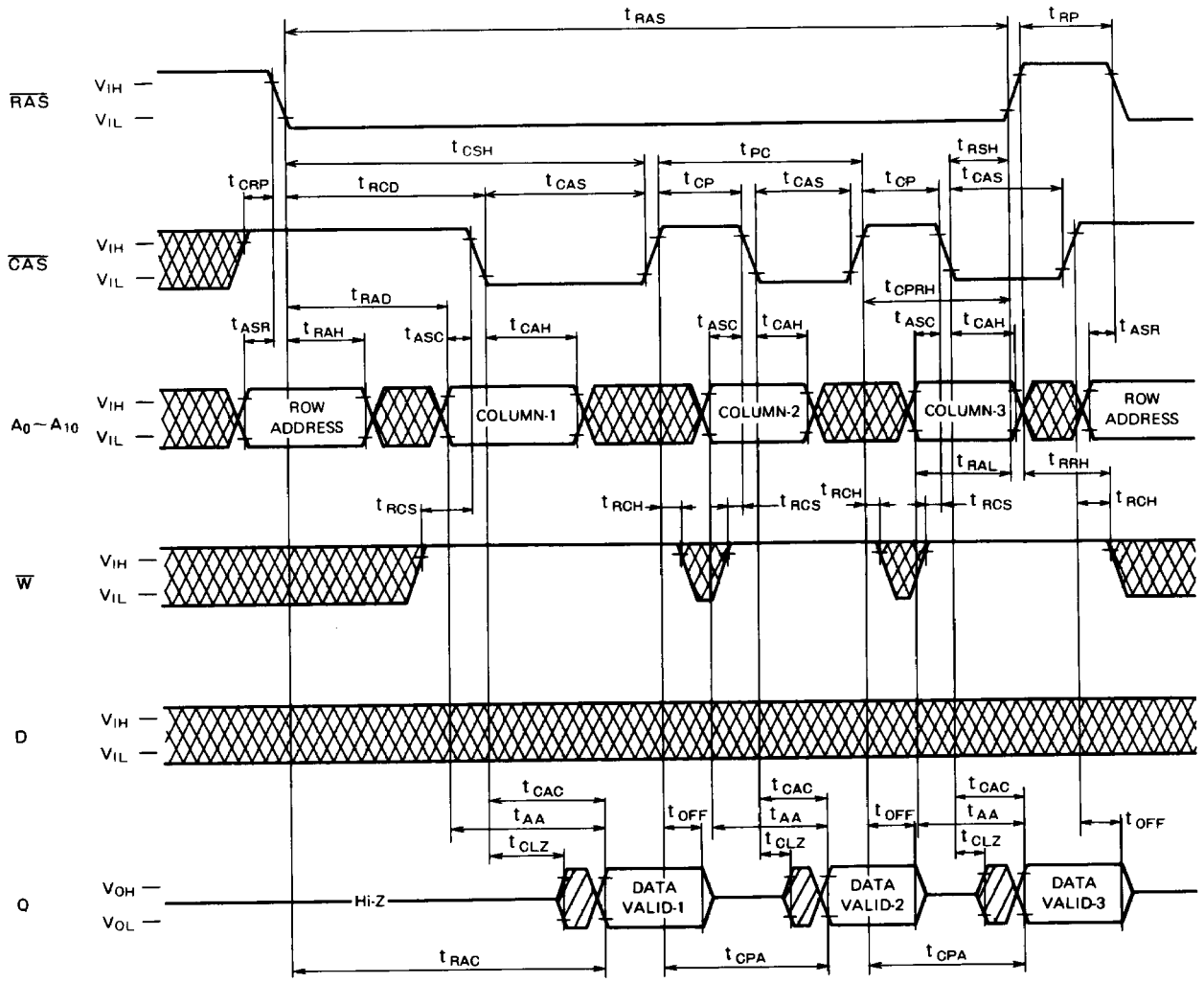


Hidden Refresh Cycle (Read) (Note 29)

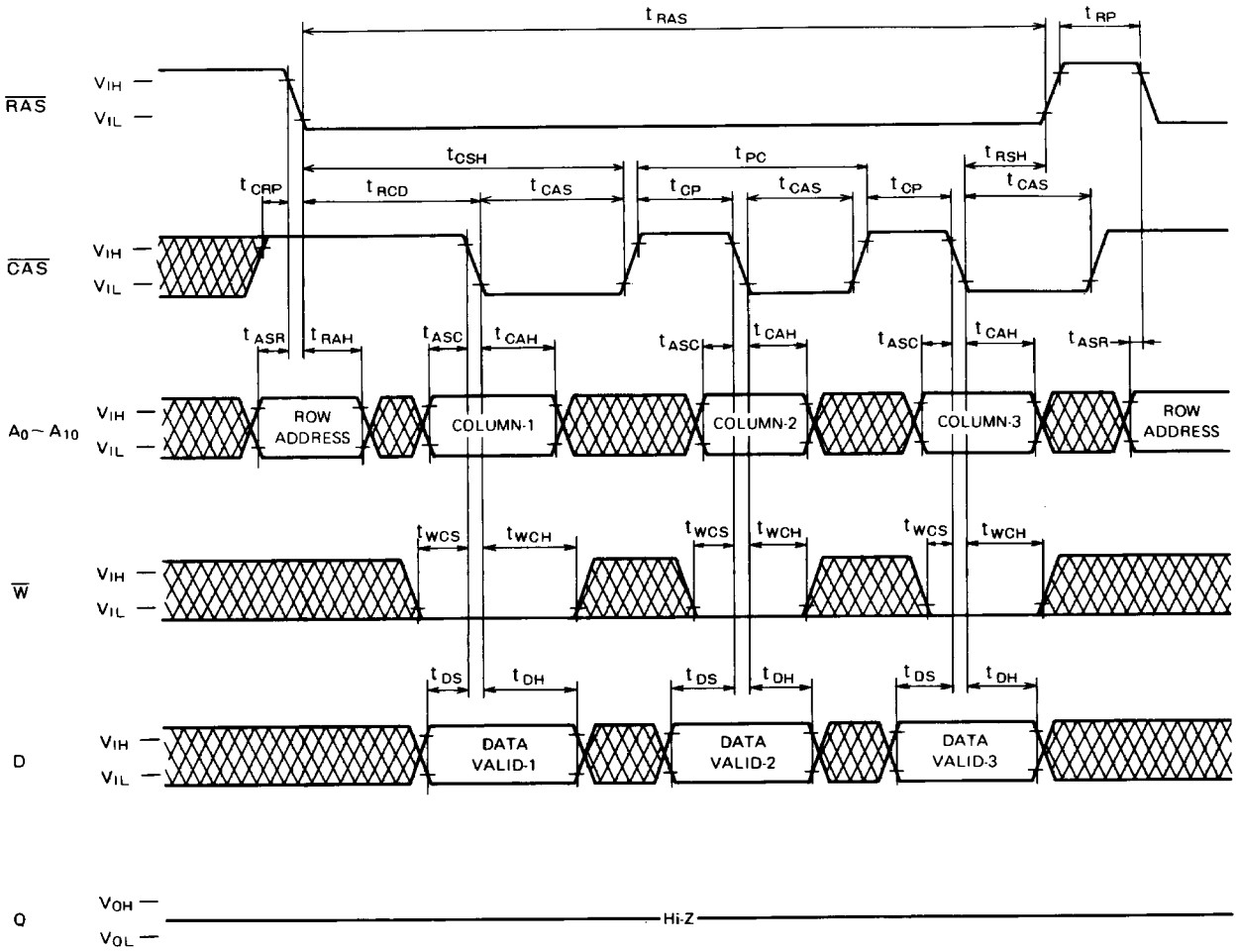


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

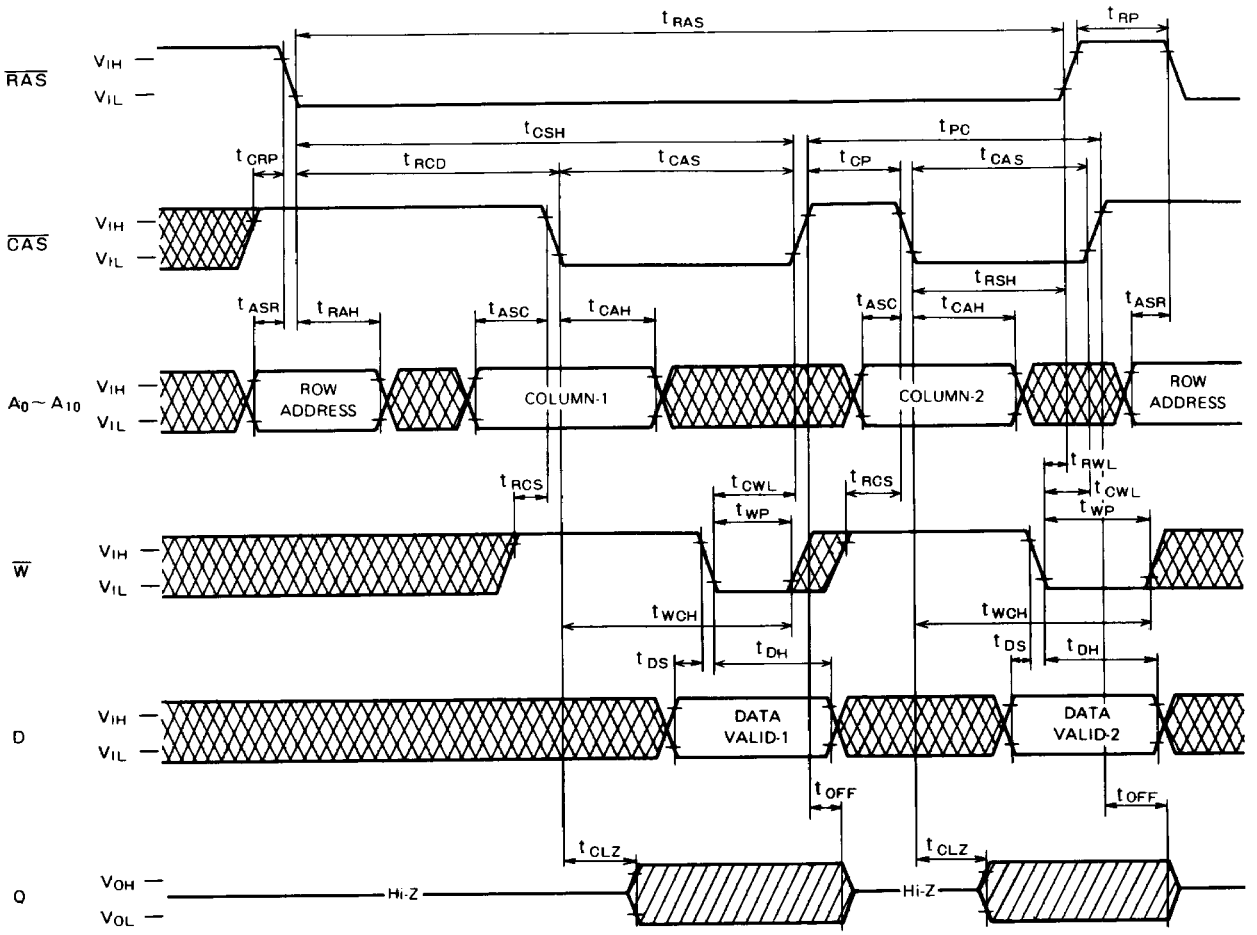
Fast-Page-Mode Read Cycle



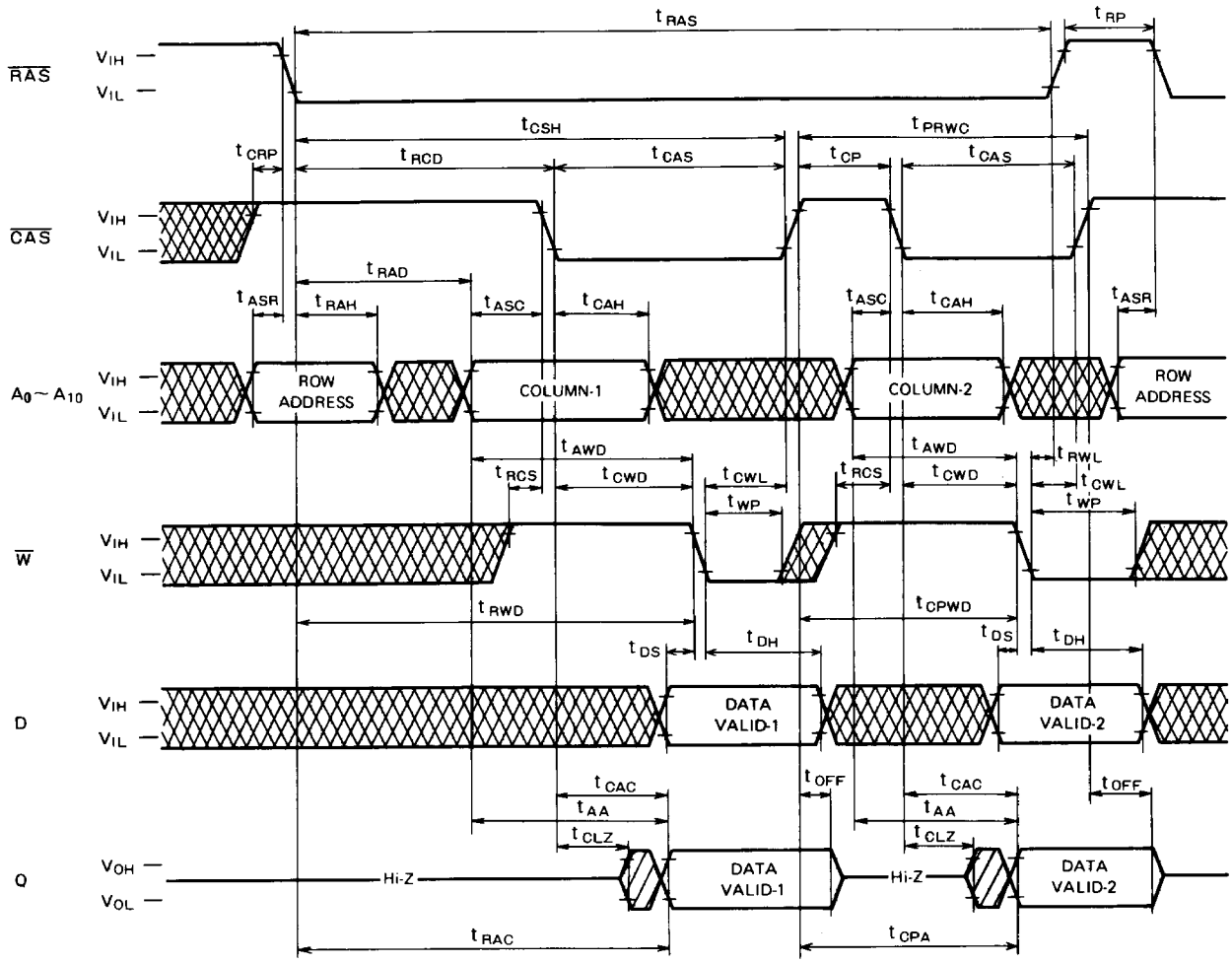
Fast-Page-Mode Write Cycle (Early Write)



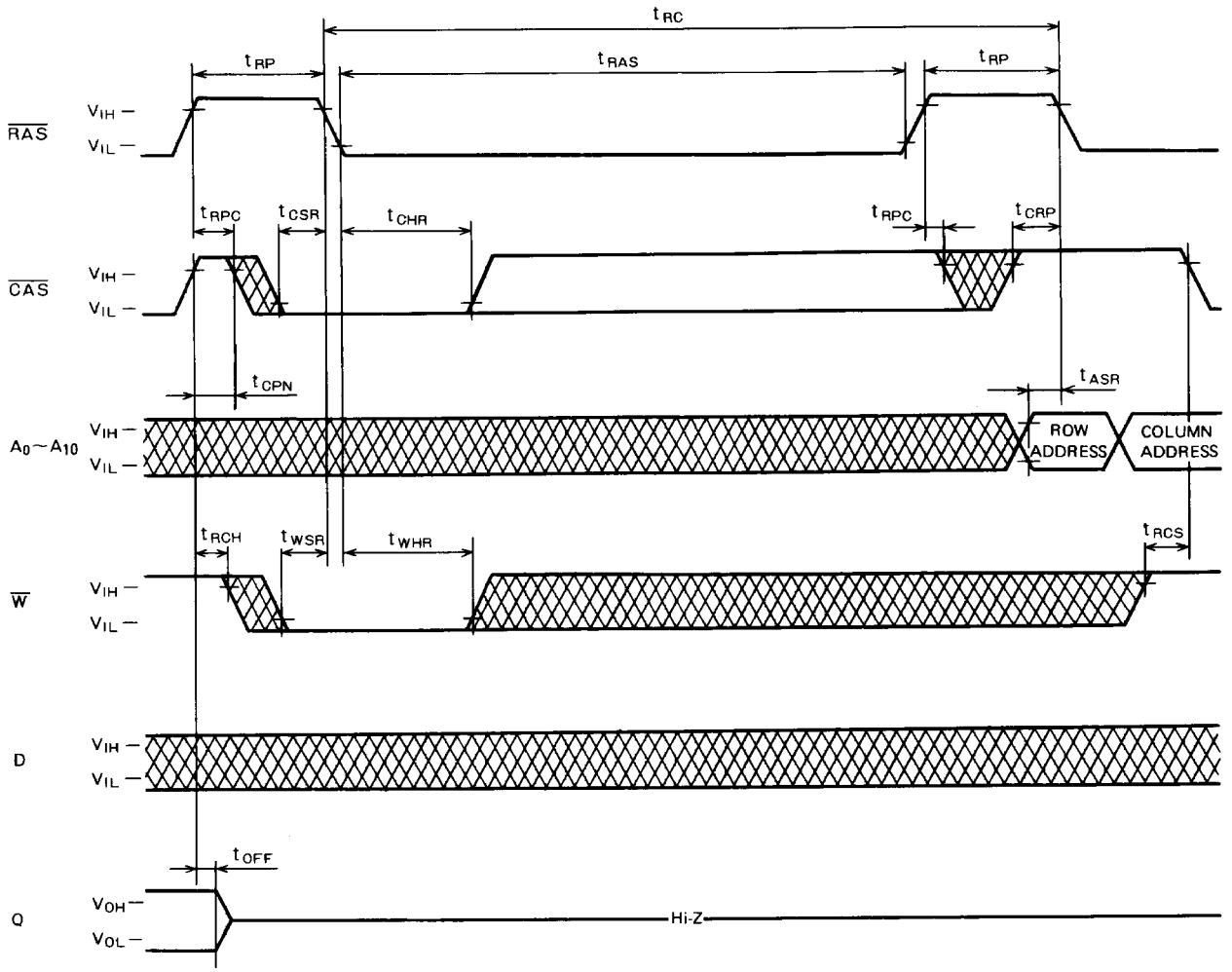
Fast-Page-Mode Write Cycle (Delayed Write)



Fast-Page-Mode Read-Write, Read-Modify-Write Cycle

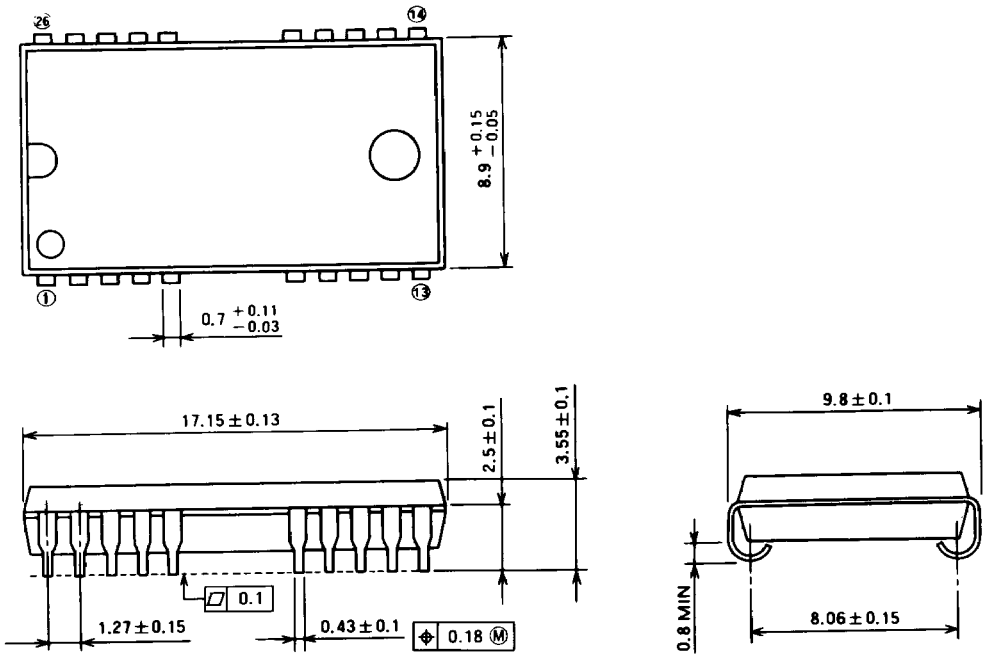


Test Mode Set Cycle (Note 30)

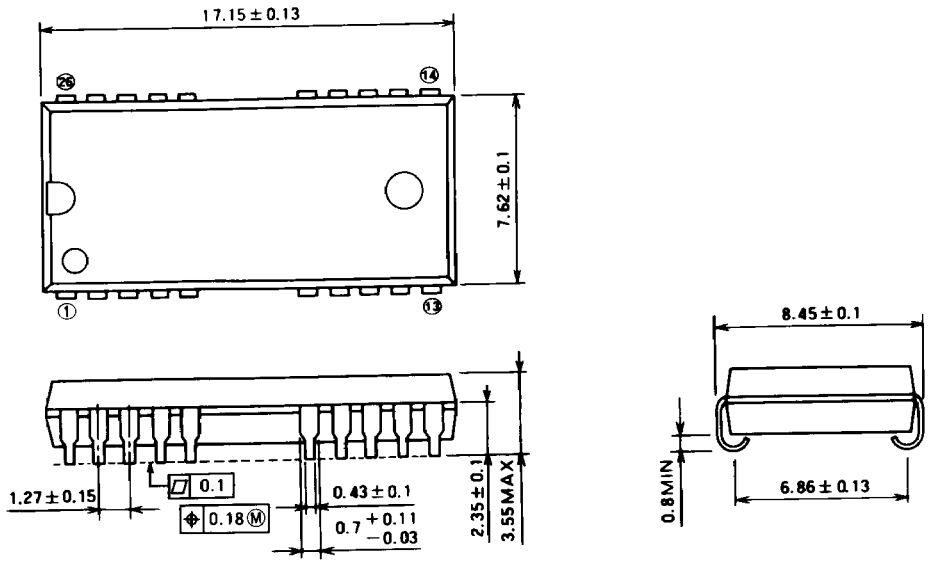


Note 30: This cycle is also available for the initialization cycle, but in this case device enters test mode.
The test mode function is initiated with a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified above timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (256 kilobytes deep). No addressing of A_{10} (both row and column) and A_0, A_1 (column only) is required.
During a write cycle, data on the input pin is written in parallel into all 16 bits. During a read cycle, the output pin indicates a HIGH state if all 16 bits are equal, and a LOW state if any bits differ.
During the test mode operation, a WCBR cycle is used to perform refresh.

26P0Z **Plastic 26pin 350mil SOJ** Dimension in mm

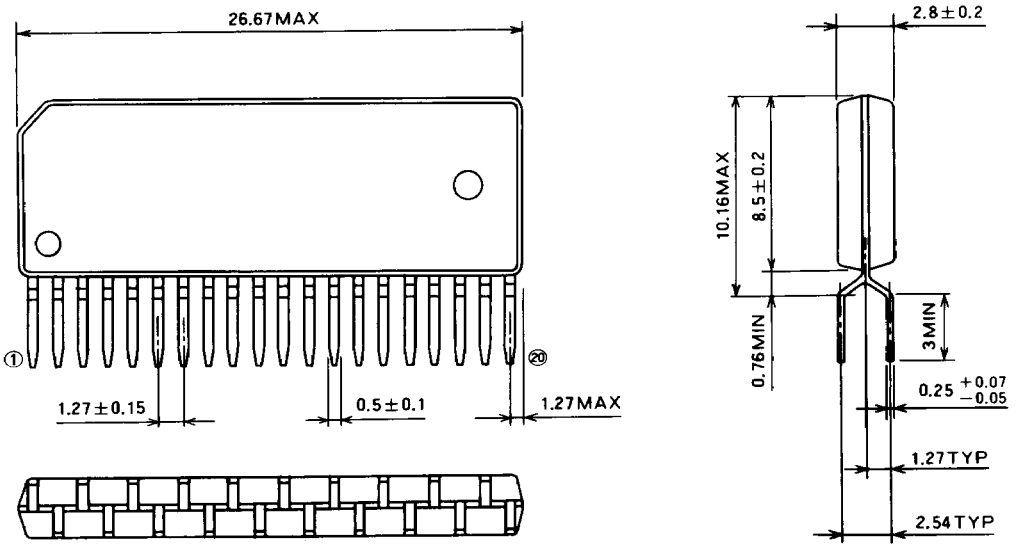


26P0J **Plastic 26pin 300mil SOJ** Dimension in mm



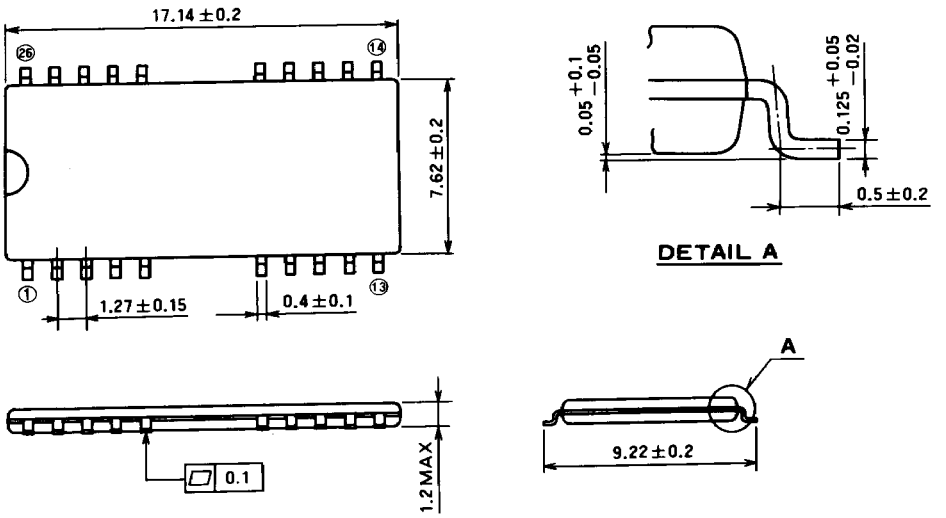
20P5L-B Plastic 20pin 400mil ZIP

Dimension in mm

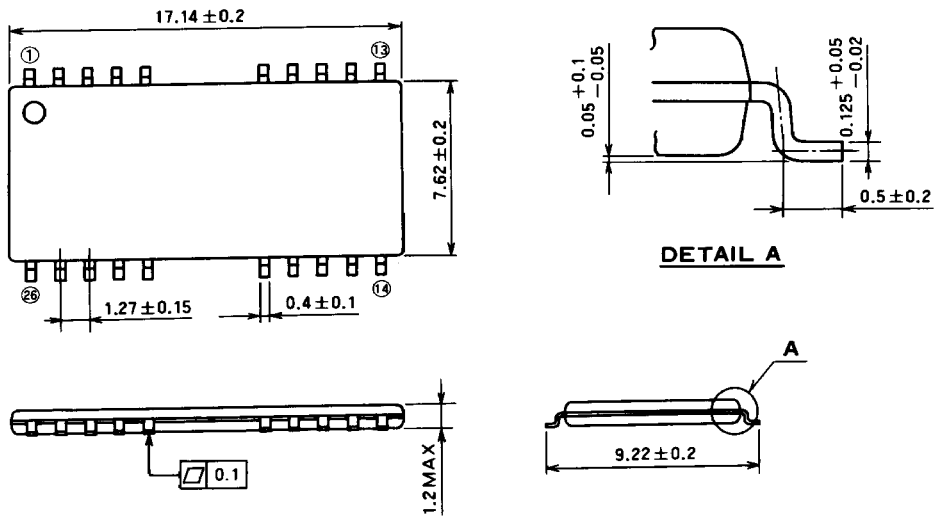


26P3Z Plastic 26pin 300mil TSOP (II)

Dimension in mm



26P3Z **Plastic 26pin 300mil TSOP (II) (Reverse Bend Type)** Dimension in mm



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