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Discovery™ II MV64360, MV64361 and MV64362 (PowerPC®) System Controllers

The Marvell® Discovery™ II MV64360, MV64361 and MV64362 devices are full-featured system controllers that combine high-performance system and communications peripherals on a single chip. The devices are designed for PowerPC® processors such as the Motorola® MPC74xx and MPC75x families and the IBM® 750Cxe/FX series CPUs, and support both the 60x and the advanced Motorola MPX bus protocols. They are the only system controllers to support Symmetrical Multi-Processing (SMP) in both 60x and MPX modes, resulting in highest processor performance.

The Discovery II MV64360 device is a full-featured system controller, offering a 72-bit Double Data Rate (DDR) memory controller with a 183 MHz clock rate (366 Mbps data rate), on-board 2 Megabits Static Random Access Memory (SRAM), dual 64-bit PCI/PCI-X interfaces, PCI bridge and arbiter, three 10/100/1000 Megabits per second (Mbps) Ethernet controllers, two multi-protocol serial channels, and TWSI (Two Wire Serial Interface) and interrupt controllers.

The Discovery II MV64361 controller offers a 72-bit DDR memory controller with a 183 MHz clock rate (366 MHz data rate), on-board 2 Megabits SRAM, dual 32-bit PCI/PCI-X interfaces, PCI bridge and arbiter, two 10/100/1000 Mbps Ethernet controllers, two multi-protocol serial channels, and TWSI and interrupt controllers.

The Discovery II MV64362 device provides a 72-bit DDR

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memory controller with a 183 MHz clock rate (366 MHz data rate), single 64-bit PCI/PCI-X interface, PCI bridge and arbiter, a single 10/100/1000 Mbps Ethernet controller, two multi-protocol serial channels, TWSI and interrupt controllers. They are targeted for system solutions employing a single processor and requiring minimal communications functionality.

The Marvell Discovery II MV64360, MV64361 and MV64362 architecture employs a high-speed crossbar fabric to enable non-blocking concurrent transactions between the CPU, PCI, Local Area Network (LAN), Wide Area Network (WAN), and memory, greatly enhancing overall system performance. The internal crossbar fabric provides an aggregate throughput of up to 100 Gigabits per second (Gbps) to deliver unprecedented performance for next-generation communications equipment.

Key Features

High-performance controller for PowerPC-based communications systems

- 64-bit 133 MHz 60X/MPC CPU bus interface
- 72-bit (64-bit with 8-bit ECC) 183 MHz DDR SDRAM controller
- Dual 64-bit 66 MHz PCI /133 MHz PCI-X interfaces (for MV64360)
- Dual 32-bit 66 Mhz PC/133 Mhz PCI-X Interfaces (for MV64361)
- Single 64-bit 66 Mhz PCI/133 MHz PCI-X interface (for MV64362)
- Advanced internal crossbar fabric
- 32-bit 133 MHz peripheral device bus interface

Integrated systems peripherals

- Interrupt controller
- 4 channel DMA controller
- Device bus controller
- PCI arbiter
- Master/slave TWSI controller
- DDR SDRAM controller
- Timers

Integrated 2 Megabits SRAM

(MV64360 and MV64361 only)

Advanced communications unit

- One 10/100/1000 Mbps Ethernet controllers with packet filtering and priority queuing (for MV64362)
- Two 10/100/1000 Mbps Ethernet controllers with packet filtering and priority queuing (for MV64361)
- Three 10/100/1000 Mbps Ethernet controllers with packet filtering and priority queuing (for MV64360)
- Two Multi-Protocol Serial Controllers (MPSC)

64-bit PowerPC CPU bus interface

- Motorola MPC750, 755, 74xx and IBM PPC750, 750CXe, 750FX processor support
- 60x and MPX bus protocol support
- 133 MHz CPU bus frequency (2.5v or 3.3v configuration)
- Configurable cache coherency
- Supports split-read transactions with out-of-order completion

High-performance DDR SDRAM controller

- 183 MHz memory interface
- 8 Gigabyte address space
- Supports DRAM bank interleaving
- Supports up to 16 open pages

Data integrity support between CPU, PCI and DRAM interfaces

- ECC on 64-bit wide SDRAM
- Parity support on CPU and PCI buses
- Parity support on integrated SRAM
- Full error reporting including error counters
- Transaction bridging between PCI interfaces
- Supports PCI delayed read transactions

Advanced 0.18u process

- 1.8v core
- 2.5v/3.3v CPU interface
- 3.3v input/output (I/O)
- 5v tolerant PCI interface

724-pin Plastic Ball Grid Array (PGBA) package

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