

# DRAM

# 1 MEG x 16 DRAM

3.3V, EDO PAGE MODE,  
OPTIONAL EXTENDED REFRESH

## FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance CMOS silicon-gate process
- Single +3.3V  $\pm 0.3V$  power supply
- All device pins are TTL-compatible
- Refresh modes:  $\overline{\text{RAS}}$  ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  (CBR), HIDDEN; optional Extended
- BYTE WRITE access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Low power, 0.3mW standby; 180mW active, typical
- Extended Data-Out (EDO) PAGE access cycle
- 5V-tolerant I/Os (5.5V maximum  $V_{IH}$  level)

## OPTIONS

- Timing
  - 60ns access -6
  - 70ns access -7
- Refresh Rate
  - Standard 16ms period None
  - Extended 128ms period L
- Packages
  - Plastic TSOP (400 mil) TG
  - Plastic SOJ (400 mil) DJ\*
- Part Number Example: MT4LC1M16E5TG-6 L

## MARKING

## KEY TIMING PARAMETERS

SPEED	$t_{RC}$	$t_{RAC}$	$t_{PC}$	$t_{AA}$	$t_{CAC}$	$t_{CAS}$
-6	105ns	60ns	25ns	30ns	15ns	12ns
-7	125ns	70ns	30ns	35ns	20ns	12ns

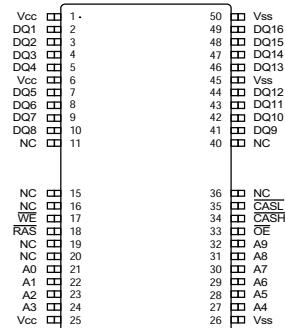
## GENERAL DESCRIPTION

The MT4LC1M16E5(L) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. The MT4LC1M16E5(L) has both BYTE WRITE and WORD WRITE access cycles via two  $\overline{\text{CAS}}$  pins ( $\overline{\text{CASL}}$  and  $\overline{\text{CASH}}$ ). These function in a similar manner to a single  $\overline{\text{CAS}}$  of other DRAMs in that either  $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$  will generate an internal  $\overline{\text{CAS}}$ .

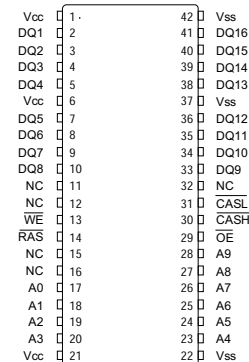
The MT4LC1M16E5(L)  $\overline{\text{CAS}}$  function and timing are determined by the first  $\overline{\text{CAS}}$  ( $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$ ) to transition

## PIN ASSIGNMENT (Top View)

### 44/50-Pin TSOP (DB-5)



### 42-Pin SOJ\* (DA-7)



\*Consult factory for availability

LOW and the last  $\overline{\text{CAS}}$  to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle.  $\overline{\text{CASL}}$  transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and  $\overline{\text{CASH}}$  transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time.  $\overline{\text{RAS}}$  is used to latch the first 10 bits and  $\overline{\text{CAS}}$  the latter 10 bits. The  $\overline{\text{CAS}}$  function also determines whether the cycle will be a refresh cycle ( $\overline{\text{RAS}}$  ONLY) or an active cycle (READ, WRITE or READ WRITE) once  $\overline{\text{RAS}}$  goes LOW.

**GENERAL DESCRIPTION (continued)**

The  $\overline{\text{CASL}}$  and  $\overline{\text{CASH}}$  inputs internally generate a  $\overline{\text{CAS}}$  signal functioning in a similar manner to the single  $\overline{\text{CAS}}$  input of other DRAMs. The key difference is each  $\overline{\text{CAS}}$  input ( $\overline{\text{CASL}}$  and  $\overline{\text{CASH}}$ ) controls its corresponding 8 DQ inputs during WRITE accesses.  $\overline{\text{CASL}}$  controls DQ1 through DQ8 and  $\overline{\text{CASH}}$  controls DQ9 through DQ16. The two  $\overline{\text{CAS}}$  controls give the MT4LC1M16E5(S) both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or  $\overline{\text{CAS}}$  ( $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$ ), whichever occurs last. An EARLY WRITE occurs when WE is taken LOW prior to either  $\overline{\text{CAS}}$  falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE falls after  $\overline{\text{CAS}}$  ( $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$ ) was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of  $\overline{\text{OE}}$ . During LATE WRITE or READ-MODIFY-WRITE cycles,  $\overline{\text{OE}}$  must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping  $\overline{\text{OE}}$  LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by  $\overline{\text{OE}}$  and  $\overline{\text{WE}}$ .

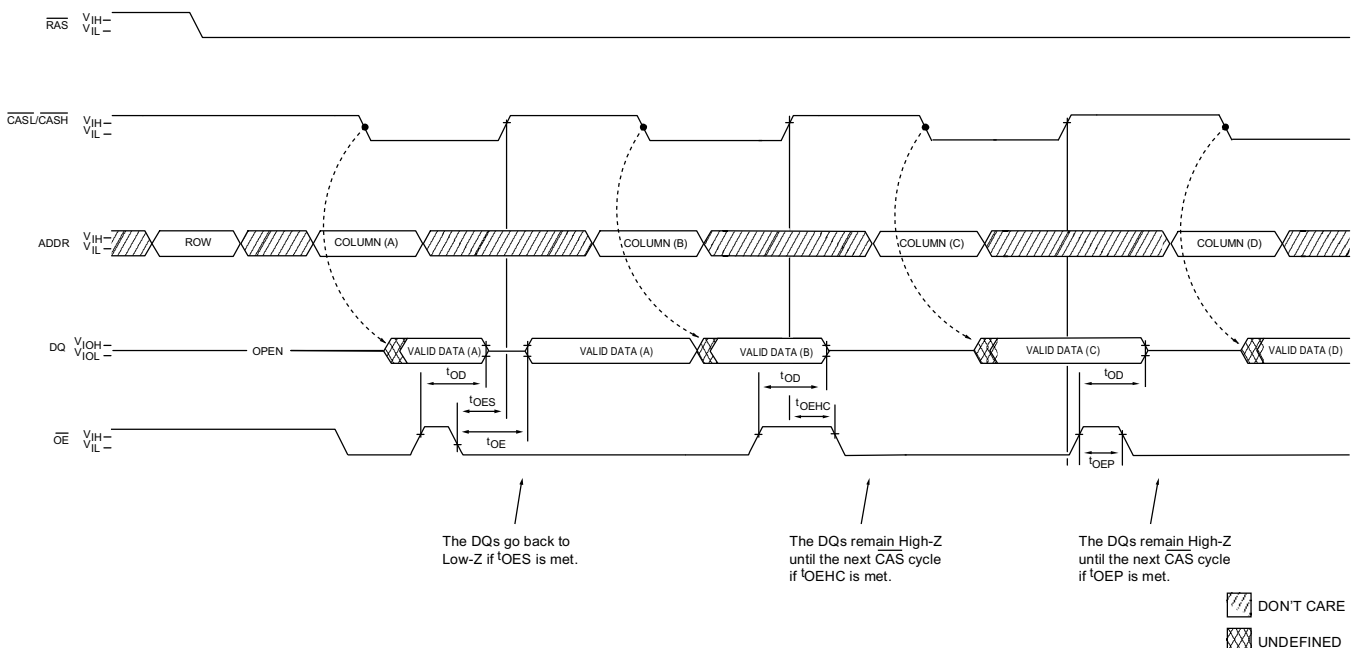
**PAGE ACCESS**

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The PAGE cycle is always initiated with a row-address strobed-in by  $\overline{\text{RAS}}$  followed by a column-address strobed-in by  $\overline{\text{CAS}}$ .  $\overline{\text{CAS}}$  may be toggled-in by holding  $\overline{\text{RAS}}$  LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning  $\overline{\text{RAS}}$  HIGH terminates the PAGE MODE of operation.

**EDO PAGE MODE**

The MT4LC1M16E5(L) provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after  $\overline{\text{CAS}}$  returns HIGH. EDO provides for  $\overline{\text{CAS}}$  precharge time ( $t_{\text{CP}}$ ) to occur without the output data going invalid. This elimination of  $\overline{\text{CAS}}$  output control provides for pipeline READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of  $\overline{\text{CAS}}$ . EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after  $\overline{\text{CAS}}$  goes HIGH during READs, provided  $\overline{\text{RAS}}$  and  $\overline{\text{OE}}$  are held LOW. If  $\overline{\text{OE}}$  is pulsed while  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are LOW, data will toggle from valid data to High-Z and back to the same valid data. If  $\overline{\text{OE}}$  is toggled or pulsed after  $\overline{\text{CAS}}$  goes HIGH while  $\overline{\text{RAS}}$  remains LOW, data will transition to and remain High-Z (refer to Figure 1).



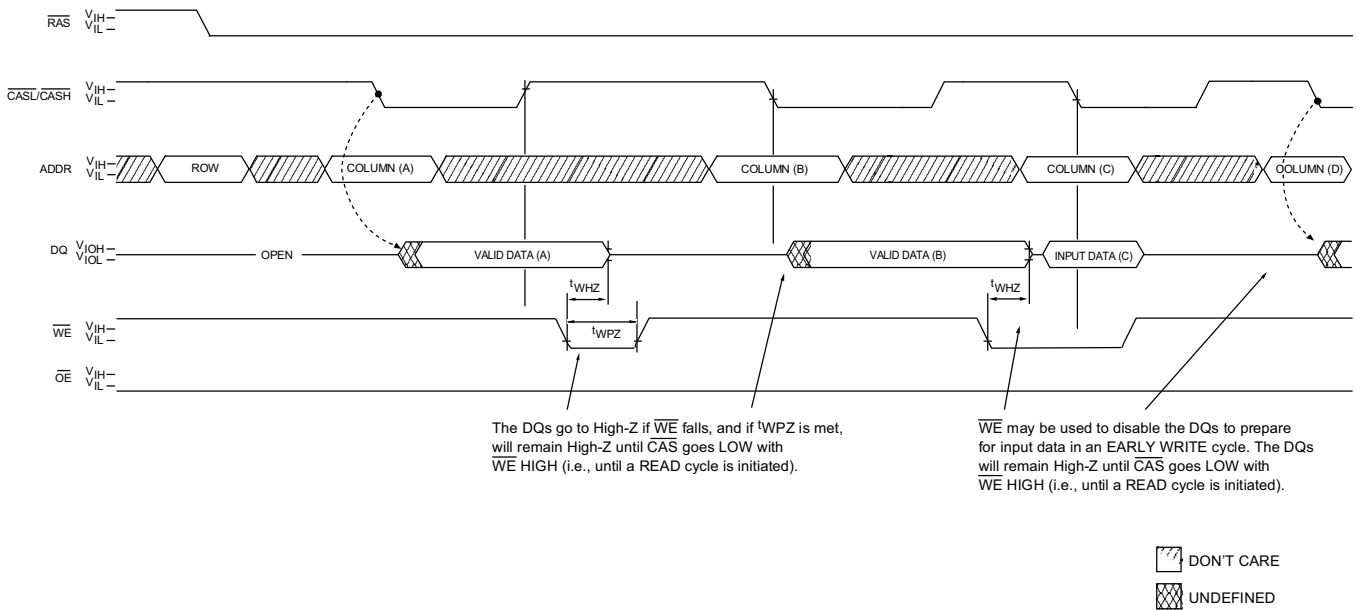
**Figure 1**  
**OUTPUT ENABLE AND DISABLE**

**EDO PAGE MODE (continued)**

$\overline{WE}$  can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

During an application, if the DQ outputs are wire OR'd,  $\overline{OE}$  must be used to disable idle banks of DRAMs. Alterna-

tively, pulsing  $\overline{WE}$  to the idle banks during  $\overline{CAS}$  HIGH time will also High-Z the outputs. Independent of  $\overline{OE}$  control, the outputs will disable after 'OFF', which is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.



**Figure 2**  
 **$\overline{WE}$  CONTROL OF DQs**

**BYTE ACCESS CYCLE**

The BYTE WRITES and BYTE READS are determined by the use of  $\overline{\text{CASL}}$  and  $\overline{\text{CASH}}$ . Enabling  $\overline{\text{CASL}}$  will select a lower BYTE access (DQ1-DQ8). Enabling  $\overline{\text{CASH}}$  will select an upper BYTE access (DQ9-DQ16). Enabling both  $\overline{\text{CASL}}$  and  $\overline{\text{CASH}}$  selects a WORD WRITE cycle.

The MT4LC1M16E5(L) may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the CAS inputs. Figure 3 illustrates the BYTE WRITE and WORD WRITE cycles.

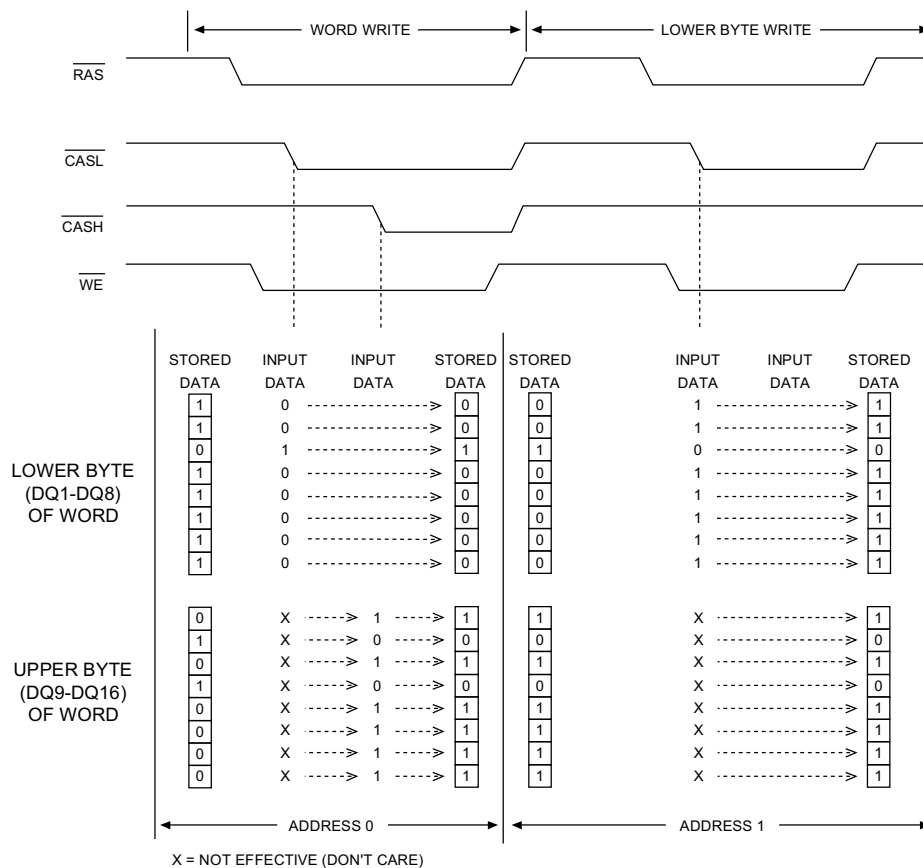
Additionally, both bytes must always be of the same mode of operation if both bytes are active. A  $\overline{\text{CAS}}$  precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte is not allowed during the same cycle. However, an EARLY

WRITE on one byte and, after a  $\overline{\text{CAS}}$  precharge has been satisfied, a LATE WRITE on the other byte is permissible.

**REFRESH**

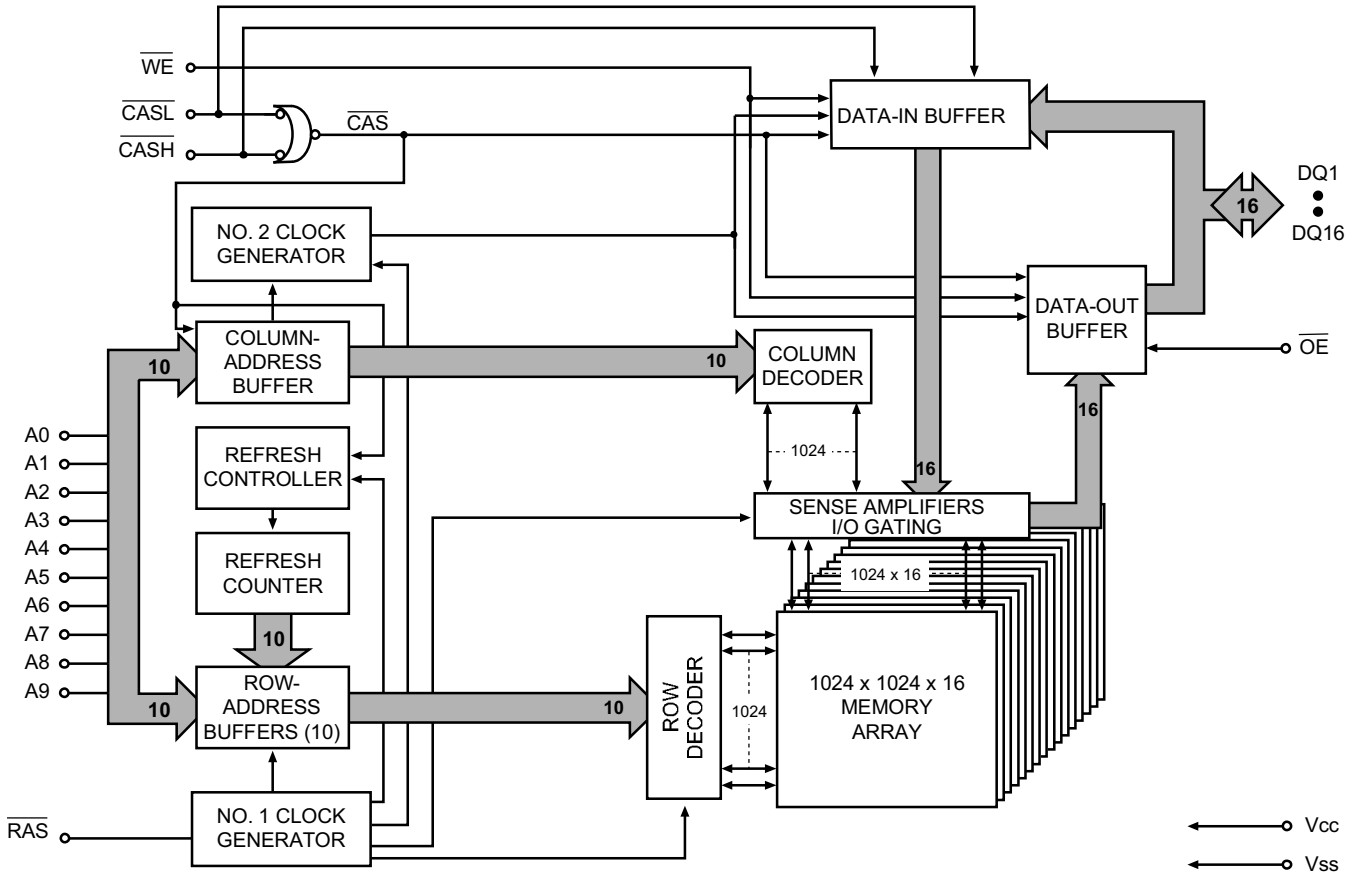
Preserve correct memory cell data by maintaining power and executing a  $\overline{\text{RAS}}$  cycle (READ, WRITE) or  $\overline{\text{RAS}}$  refresh cycle ( $\overline{\text{RAS}}$  ONLY, CBR, or HIDDEN) so that all 1,024 combinations of  $\overline{\text{RAS}}$  addresses are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic  $\overline{\text{RAS}}$  addressing.

An optional Extended Refresh mode is also available on the MT4LC1M16E5 L. The "L" version allows the user a dynamic refresh mode at the extended refresh period of 128ms eight times longer than the standard 16ms specification.



**Figure 3**  
**WORD AND BYTE WRITE EXAMPLE**

**FUNCTIONAL BLOCK DIAGRAM**



**TRUTH TABLE**

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CASL}}$	$\overline{\text{CASH}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES		DQs	NOTES
							t <sub>R</sub>	t <sub>C</sub>		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Upper Byte, Data-Out	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
	Any Cycle	L	L→H	L→H	H	L	n/a	n/a	Data-Out	2
EDO-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{\text{RAS}}$ -ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	4

- NOTE:**
1. These WRITE cycles may also be BYTE WRITE cycles (either  $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$  active).
  2. These READ cycles may also be BYTE READ cycles (either  $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$  active).
  3. EARLY WRITE only.
  4. Only one CAS must be active ( $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$ ).

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc pin Relative to Vss ..... -1V to +4.6V  
 Voltage on NC, Inputs or I/O pins  
 Relative to Vss ..... -1V to +5.5V  
 Operating Temperature, T<sub>A</sub> (ambient) ..... 0°C to +70°C  
 Storage Temperature (plastic) ..... -55°C to +150°C  
 Power Dissipation ..... 1W  
 Short Circuit Output Current ..... 50mA

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Notes: 1, 2, 3) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V <sub>IH</sub>	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V <sub>IL</sub>	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V <sub>IN</sub> ≤ 5.5V (All other pins not under test = 0V)	I <sub>I</sub>	-2	2	μA	4
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V <sub>OUT</sub> ≤ 5.5V)	I <sub>OZ</sub>	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I <sub>OUT</sub> = -2.0mA)	V <sub>OH</sub>	2.4		V	
Output Low Voltage (I <sub>OUT</sub> = 2.0mA)	V <sub>OL</sub>		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES
		-6	-7		
STANDBY CURRENT: (TTL) ( $\overline{RAS} = \overline{CAS} = V_{IH}$ )	I <sub>CC1</sub>	2	2	mA	
STANDBY CURRENT: (CMOS) ( $\overline{RAS} = \overline{CAS} = \text{other inputs} = V_{CC} - 0.2V$ )	I <sub>CC2</sub>	500	500	μA	
	L only I <sub>CC2</sub>	300	300	μA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ( $\overline{RAS}, \overline{CAS}$ address cycling: t <sub>RC</sub> = t <sub>RC</sub> [MIN])	I <sub>CC3</sub>	170	155	mA	5, 6
OPERATING CURRENT: EDO PAGE MODE Average power supply current ( $\overline{RAS} = V_{IL}, \overline{CAS}$ , address cycling: t <sub>PC</sub> = t <sub>PC</sub> [MIN])	I <sub>CC4</sub>	120	110	mA	5, 6
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ( $\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ : t <sub>RC</sub> = t <sub>RC</sub> [MIN])	I <sub>CC5</sub>	160	145	mA	5, 6
REFRESH CURRENT: CBR Average power supply current ( $\overline{RAS}, \overline{CAS}$ address cycling: t <sub>RC</sub> = t <sub>RC</sub> [MIN])	I <sub>CC6</sub>	150	140	mA	5, 7
REFRESH CURRENT: Extended (L version only) Average power supply current: $\overline{CAS} = 0.2V$ or CBR cycling; $\overline{RAS} = t_{RAS} (MIN)$ ; $\overline{WE} = V_{CC} - 0.2V$ ; $\overline{OE}, A0-A9$ and $D_{IN} = V_{CC} - 0.2V$ or $0.2V$ ( $D_{IN}$ may be left open); t <sub>RC</sub> = 125μs (1,024 rows at 125μs = 128ms)	I <sub>CC7</sub> (L only)	150	150	μA	5, 7

**CAPACITANCE**

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C <sub>I1</sub>	5	pF	8
Input Capacitance: $\overline{RAS}$ , $\overline{CAS}$ , $\overline{CASH}$ , $\overline{WE}$ , $\overline{OE}$	C <sub>I2</sub>	7	pF	8
Input/Output Capacitance: DQ	C <sub>I0</sub>	7	pF	8

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 2, 3, 6, 9, 10, 11, 12,) ( $V_{CC} = +3.3V \pm 0.3V$ )

AC CHARACTERISTICS PARAMETER	SYM	-6		-7		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Access time from column-address	$t_{AA}$		30		35	ns	
Column-address set-up to $\overline{CAS}$ precharge	$t_{ACH}$	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$ )	$t_{AR}$	45		50		ns	
Column-address setup time	$t_{ASC}$	0		0		ns	25
Row-address setup time	$t_{ASR}$	0		0		ns	25
Column-address to $\overline{WE}$ delay time	$t_{AWD}$	55		60		ns	13
Access time from $\overline{CAS}$	$t_{CAC}$		15		20	ns	14, 26
Column-address hold time	$t_{CAH}$	10		12		ns	25
$\overline{CAS}$ pulse width	$t_{CAS}$	12	10,000	13	10,000	ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	$t_{CHR}$	10		12		ns	7, 28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	$t_{CLCH}$	10		10		ns	29
$\overline{CAS}$ to output in Low-Z	$t_{CLZ}$	0		0		ns	26
Data output hold after next $\overline{CAS}$ LOW	$t_{COH}$	3		3		ns	
$\overline{CAS}$ precharge time	$t_{CP}$	10		10		ns	15, 30
Access time from $\overline{CAS}$ precharge	$t_{CPA}$		35		40	ns	26
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5		5		ns	28
$\overline{CAS}$ hold time	$t_{CSH}$	50		55		ns	28
$\overline{CAS}$ setup time (CBR REFRESH)	$t_{CSR}$	5		5		ns	7, 25
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	35		40		ns	13, 25
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	15		15		ns	28
Data-in hold time	$t_{DH}$	10		12		ns	16, 26
Data-in hold time (referenced to $\overline{RAS}$ )	$t_{DHR}$	45		55		ns	
Data-in setup time	$t_{DS}$	0		0		ns	16, 26
Output disable	$t_{OD}$	0	15	0	15	ns	
Output Enable	$t_{OE}$		15		20	ns	17, 26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	$t_{OEHL}$	12		12		ns	18
$\overline{OE}$ HIGH hold from $\overline{CAS}$ HIGH	$t_{OEHC}$	10		10		ns	18
$\overline{OE}$ HIGH pulse width	$t_{OEP}$	10		10		ns	



**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

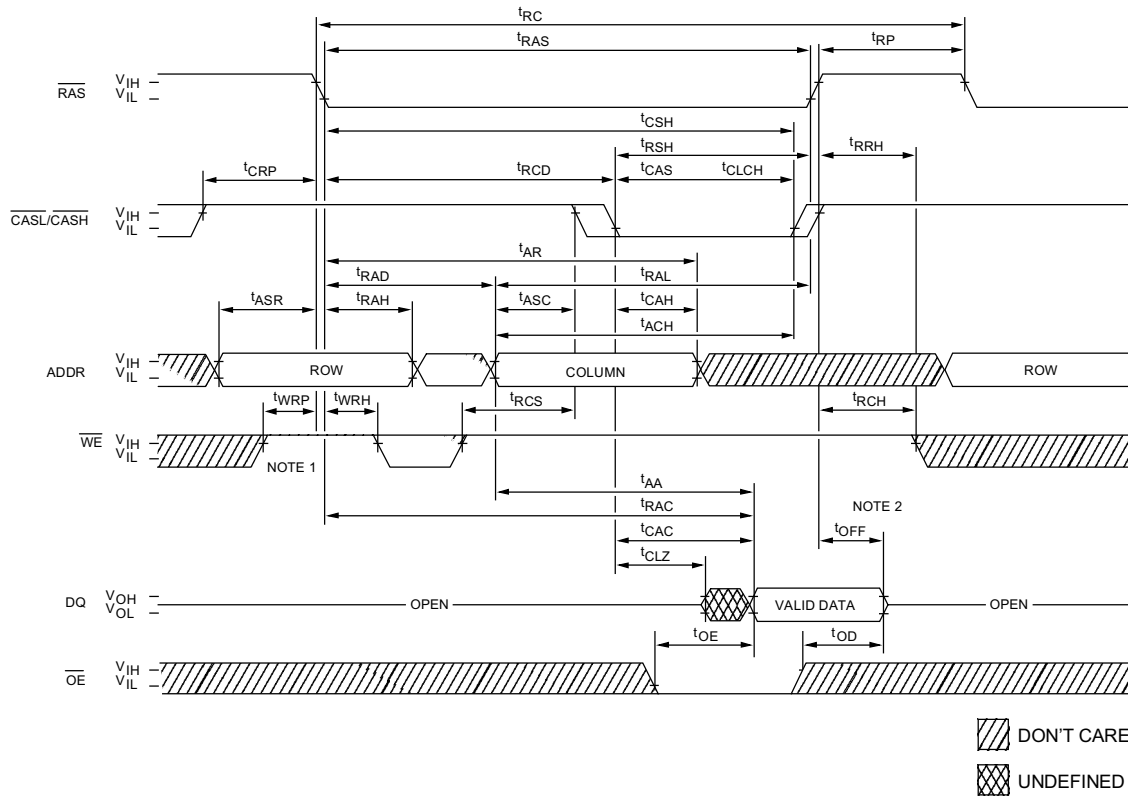
(Notes: 2, 3, 6, 9, 10, 11, 12, 20) ( $V_{CC} = +3.3V \pm 0.3V$ )

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	$t_{OES}$	5		5		ns	
Output buffer turn-off delay	$t_{OFF}$	3	15	3	15	ns	20, 26
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	$t_{ORD}$	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	$t_{PC}$	25		30		ns	31
EDO-PAGE-MODE READ-WRITE cycle time	$t_{PRWC}$	75		85		ns	31
Access time from $\overline{RAS}$	$t_{RAC}$		60		70	ns	19
$\overline{RAS}$ to column-address delay time	$t_{RAD}$	12	30	12	35	ns	21
Row-address hold time	$t_{RAH}$	10		10		ns	
Column-address to $\overline{RAS}$ lead time	$t_{RAL}$	30		35		ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	$t_{RASP}$	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	$t_{RC}$	105		125		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	14	45	14	50	ns	22, 25
Read command hold time (referenced to $\overline{CAS}$ )	$t_{RCH}$	0		0		ns	23, 28
Read command setup time	$t_{RCS}$	0		0		ns	25
Refresh period (1,024 cycles)	$t_{REF}$		16		16	ms	
Refresh period (1,024 cycles) L version	$t_{REF}$		128		128	ms	
$\overline{RAS}$ precharge time	$t_{RP}$	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{RPC}$	5		5		ns	
Read command hold time (referenced to $\overline{RAS}$ )	$t_{RRH}$	0		0		ns	23
$\overline{RAS}$ hold time	$t_{RSH}$	13		15		ns	32
READ WRITE cycle time	$t_{RWC}$	145		170		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	80		90		ns	13
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	15		15		ns	
Transition time (rise or fall)	$t_T$	2	50	2	50	ns	
Write command hold time	$t_{WCH}$	10		12		ns	32
Write command hold time (referenced to $\overline{RAS}$ )	$t_{WCR}$	45		55		ns	
$\overline{WE}$ command setup time	$t_{WCS}$	0		0		ns	13, 25
Output disable delay from $\overline{WE}$	$t_{WHZ}$	0	13	0	15	ns	
Write command pulse width	$t_{WP}$	10		12		ns	
$\overline{WE}$ pulse width to disable at $\overline{CAS}$ HIGH	$t_{WPZ}$	10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	$t_{WRH}$	10		10		ns	
$\overline{WE}$ setup time (CBR REFRESH)	$t_{WRP}$	10		10		ns	

## NOTES

1. All voltages referenced to  $V_{SS}$ .
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ) is assured.
3. An initial pause of 100 $\mu\text{s}$  is required after power-up followed by eight RAS refresh cycles ( $\overline{\text{RAS}}$  ONLY or CBR with  $\overline{\text{WE}}$  HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the  $t_{\text{REF}}$  refresh requirement is exceeded.
4. NC pins are assumed to be left floating and are not tested for leakage.
5.  $I_{CC}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. Column address changed once each cycle.
7. Enables on-chip refresh and address counters.
8. This parameter is sampled.  $V_{CC} = +3.0\text{V}$ ;  $f = 1\text{ MHz}$ .
9. AC characteristics assume  $t_T = 2.5\text{ns}$ .
10.  $V_{IH}$  (MIN) and  $V_{IL}$  (MAX) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ).
11. In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
12. Measured with a load equivalent to two TTL gates, 100pF and  $V_{OL} = 0.8\text{V}$  and  $V_{OH} = 2.0\text{V}$ .
13.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CWD}}$  are not restrictive operating parameters.  $t_{\text{WCS}}$  applies to EARLY WRITE cycles.  $t_{\text{RWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CWD}}$  apply to READ-MODIFY-WRITE cycles. If  $t_{\text{WCS}} \geq t_{\text{WCS}}$  (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  $t_{\text{WCS}} < t_{\text{WCS}}$  (MIN) and  $t_{\text{RWD}} \geq t_{\text{RWD}}$  (MIN),  $t_{\text{AWD}} \geq t_{\text{AWD}}$  (MIN) and  $t_{\text{CWD}} \geq t_{\text{CWD}}$  (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate.  $\overline{\text{OE}}$  held HIGH and  $\overline{\text{WE}}$  taken LOW after  $\overline{\text{CAS}}$  goes LOW results in a LATE WRITE ( $\overline{\text{OE}}$ -controlled) cycle.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$  and  $t_{\text{AWD}}$  are not applicable in a LATE WRITE cycle.
14. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}$  (MAX).
15. If  $\overline{\text{CAS}}$  is LOW at the falling edge of  $\overline{\text{RAS}}$ , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer,  $\overline{\text{CAS}}$  must be pulsed HIGH for  $t_{\text{CP}}$ .
16. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in EARLY WRITE cycles and  $\overline{\text{WE}}$  leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
17. If  $\overline{\text{OE}}$  is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally,  $\overline{\text{WE}}$  must be pulsed during  $\overline{\text{CAS}}$  HIGH time in order to place I/O buffers in High-Z.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{\text{OD}}$  and  $t_{\text{OE}} \text{H}$  met ( $\overline{\text{OE}}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if  $\overline{\text{CAS}}$  remains LOW and  $\overline{\text{OE}}$  is taken back LOW after  $t_{\text{OE}} \text{H}$  is met. If  $\overline{\text{CAS}}$  goes HIGH prior to  $\overline{\text{OE}}$  going back LOW, the DQs will remain open.
19. Assumes that  $t_{\text{RCD}} < t_{\text{RCD}}$  (MAX). If  $t_{\text{RCD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  will increase by the amount that  $t_{\text{RCD}}$  exceeds the value shown.
20.  $t_{\text{OFF}}$  (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to  $V_{OH}$  or  $V_{OL}$ . It is referenced from the rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$ , whichever occurs last.
21. Operation within the  $t_{\text{RAD}}$  (MAX) limit ensures that  $t_{\text{RAC}}$  (MIN) and  $t_{\text{CAC}}$  (MIN) can be met.  $t_{\text{RAD}}$  (MAX) is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}$  (MAX) limit, then access time is controlled exclusively by  $t_{\text{AA}}$ , provided  $t_{\text{RCD}}$  is not exceeded.
22. Operation within the  $t_{\text{RCD}}$  (MAX) limit ensures that  $t_{\text{RAC}}$  (MAX) can be met.  $t_{\text{RCD}}$  (MAX) is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}$  (MAX) limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ , provided  $t_{\text{RAD}}$  is not exceeded.
23. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a READ cycle.
24. The first  $\overline{\text{CAS}}_x$  edge to transition LOW.
25. Output parameter (DQx) is referenced to corresponding  $\overline{\text{CAS}}$  input; DQ1-DQ8 by  $\overline{\text{CAS}}_1$  and DQ9-DQ16 by  $\overline{\text{CAS}}_2$ .
26. Each  $\overline{\text{CAS}}_x$  must meet minimum pulse width.
27. The last  $\overline{\text{CAS}}_x$  edge to transition HIGH.
28. Last falling  $\overline{\text{CAS}}_x$  edge to first rising  $\overline{\text{CAS}}_x$  edge.
29. Last rising  $\overline{\text{CAS}}_x$  edge to first falling  $\overline{\text{CAS}}_x$  edge.
30. Last rising  $\overline{\text{CAS}}_x$  edge to next cycle's last rising  $\overline{\text{CAS}}_x$  edge.
31. Last  $\overline{\text{CAS}}_x$  to go LOW.
32. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case,  $\overline{\text{WE}} = \text{LOW}$  and  $\overline{\text{OE}} = \text{HIGH}$ .

**READ CYCLE**



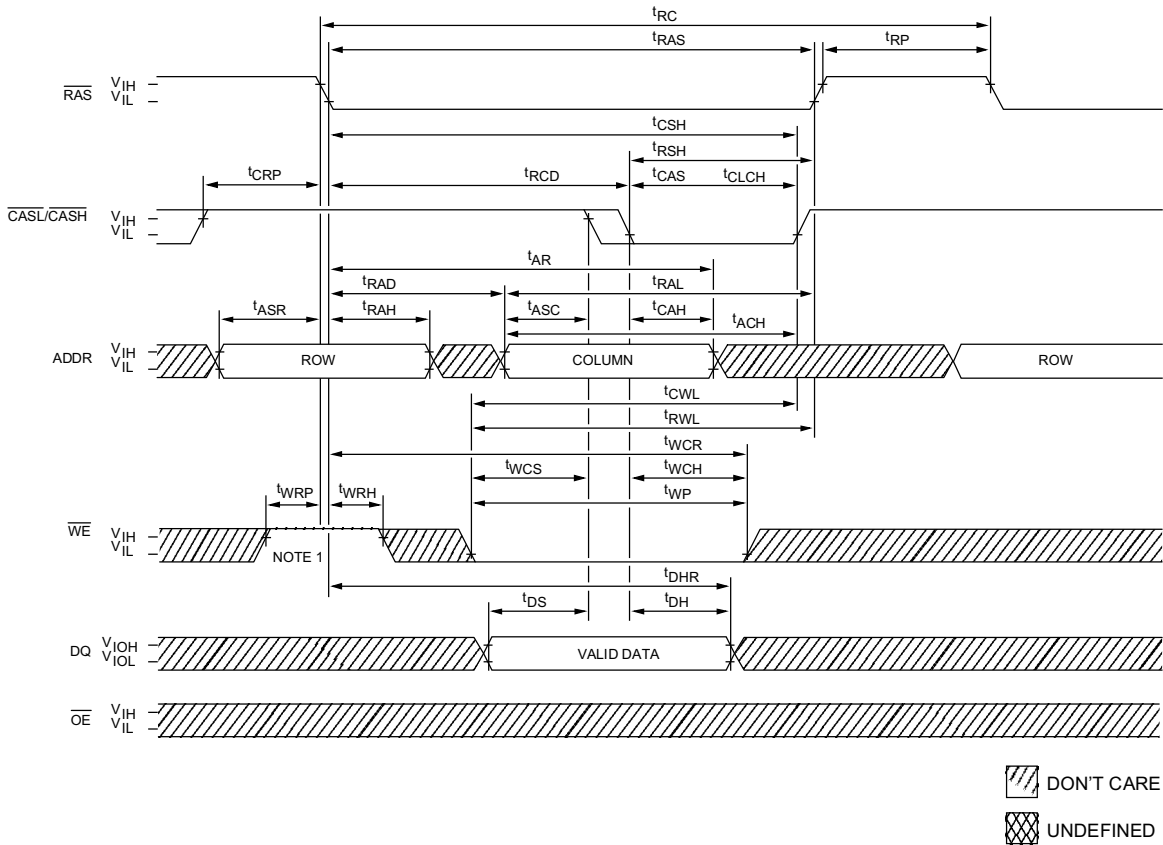
- NOTE:**
- Although  $\overline{WE}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (READ or WRITE), the system designer should implement  $\overline{WE}$  HIGH for  $t_{WRP}$  and  $t_{WRH}$ . This design implementation will facilitate compatibility with future EDO DRAMs.
  - $t_{OFF}$  is referenced from rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.

**TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{AA}$		30		35	ns
$t_{ACH}$	15		15		ns
$t_{AR}$	45		50		ns
$t_{ASC}$	0		0		ns
$t_{ASR}$	0		0		ns
$t_{CAC}$		15		20	ns
$t_{CAH}$	10		12		ns
$t_{CAS}$	12	10,000	13	10,000	ns
$t_{CLCH}$	10		10		ns
$t_{CLZ}$	0		0		ns
$t_{CRP}$	5		5		ns
$t_{CSH}$	50		55		ns
$t_{OD}$	0	15	0	15	ns
$t_{OE}$		15		20	ns
$t_{OFF}$	3	15	3	15	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{RAC}$		60		70	ns
$t_{RAD}$	12	30	12	35	ns
$t_{RAH}$	10		10		ns
$t_{RAL}$	30		35		ns
$t_{RAS}$	60	10,000	70	10,000	ns
$t_{RC}$	105		125		ns
$t_{RCD}$	14	45	14	50	ns
$t_{RCH}$	0		0		ns
$t_{RCS}$	0		0		ns
$t_{RP}$	40		50		ns
$t_{RRH}$	0		0		ns
$t_{RSH}$	13		15		ns
$t_{WRH}$	10		10		ns
$t_{WRP}$	10		10		ns

**EARLY WRITE CYCLE**



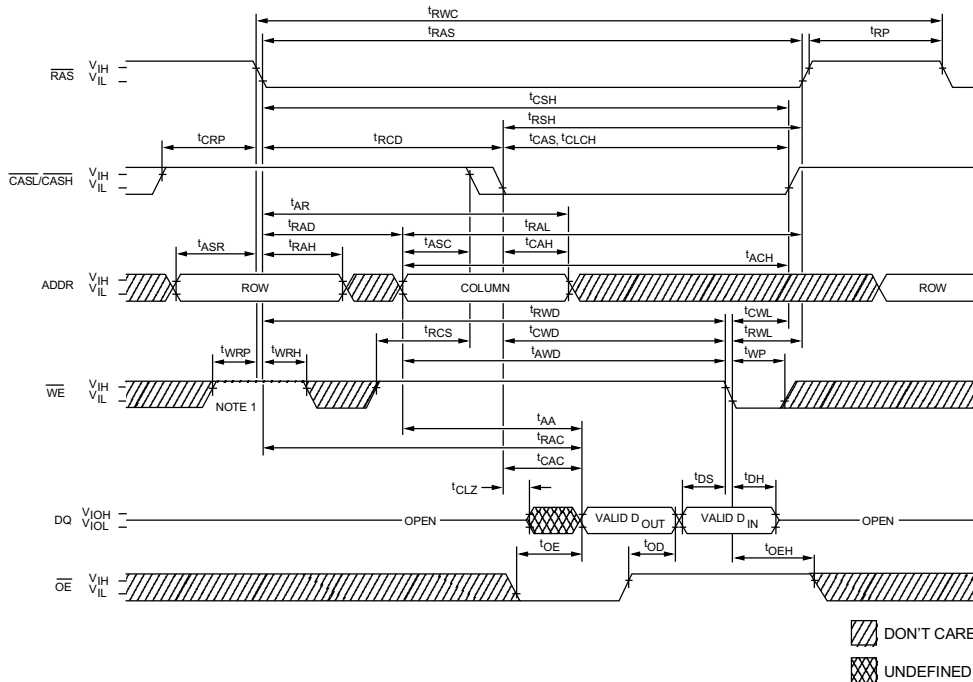
**NOTE:** 1. Although  $\overline{WE}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (READ or WRITE), the system designer should implement  $\overline{WE}$  HIGH for  $t_{WRP}$  and  $t_{WRH}$ . This design implementation will facilitate compatibility with future EDO DRAMs.

**TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{ACH}$	15		15		ns
$t_{AR}$	45		50		ns
$t_{ASC}$	0		0		ns
$t_{ASR}$	0		0		ns
$t_{CAH}$	10		12		ns
$t_{CAS}$	12	10,000	13	10,000	ns
$t_{CLCH}$	10		10		ns
$t_{CRP}$	5		5		ns
$t_{CSH}$	50		55		ns
$t_{CWL}$	15		15		ns
$t_{DH}$	10		12		ns
$t_{DHR}$	45		55		ns
$t_{DS}$	0		0		ns
$t_{RAD}$	12	30	12	35	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{RAH}$	10		10		ns
$t_{RAL}$	30		35		ns
$t_{RAS}$	60	10,000	70	10,000	ns
$t_{RC}$	105		125		ns
$t_{RCD}$	14	45	14	50	ns
$t_{RP}$	40		50		ns
$t_{RSH}$	13		15		ns
$t_{RWL}$	15		15		ns
$t_{WCH}$	10		12		ns
$t_{WCR}$	45		55		ns
$t_{WCS}$	0		0		ns
$t_{WP}$	10		12		ns
$t_{WRH}$	10		10		ns
$t_{WRP}$	10		10		ns

**READ WRITE CYCLE**  
(LATE WRITE and READ-MODIFY-WRITE cycles)



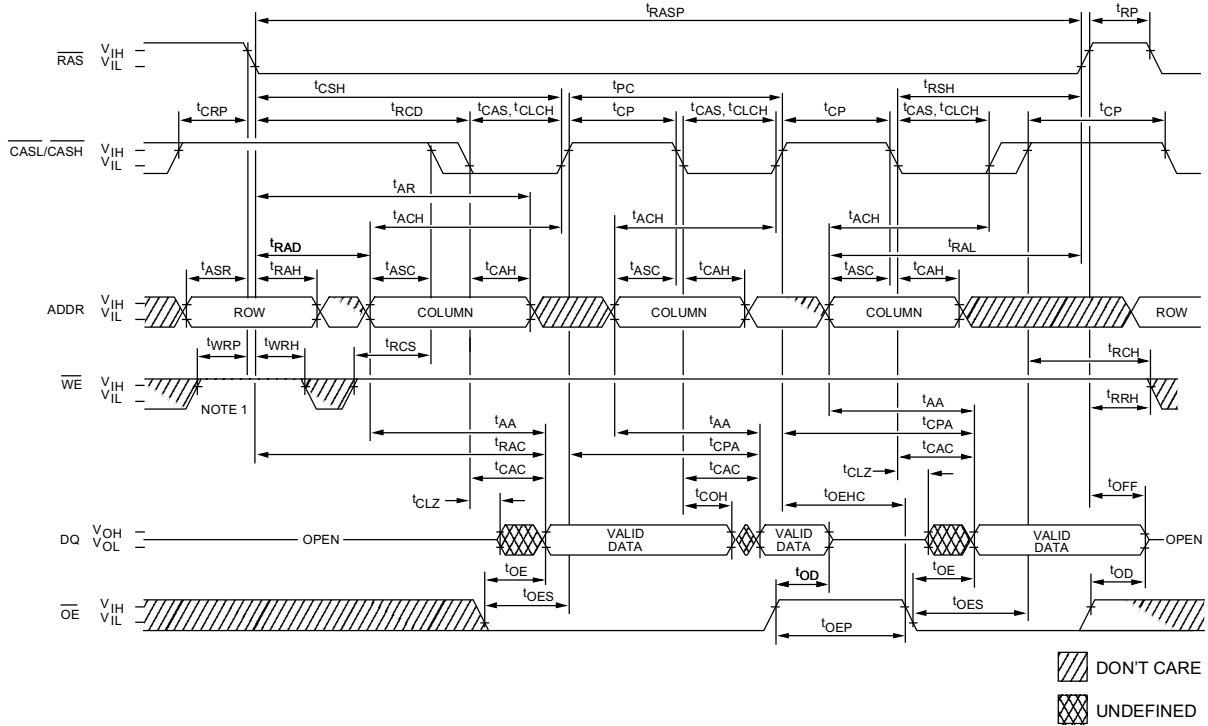
**NOTE:** 1. Although  $\overline{WE}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (READ or WRITE), the system designer should implement  $\overline{WE}$  HIGH for  $t_{WRP}$  and  $t_{WRH}$ . This design implementation will facilitate compatibility with future EDO DRAMs.

**TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{AA}$		30		35	ns
$t_{ACH}$	15		15		ns
$t_{AR}$	45		50		ns
$t_{ASC}$	0		0		ns
$t_{ASR}$	0		0		ns
$t_{AWD}$	55		60		ns
$t_{CAC}$		15		20	ns
$t_{CAH}$	10		12		ns
$t_{CAS}$	12	10,000	13	10,000	ns
$t_{CLCH}$	10		10		ns
$t_{CLZ}$	0		0		ns
$t_{CRP}$	5		5		ns
$t_{CSH}$	50		55		ns
$t_{CWD}$	35		40		ns
$t_{CWL}$	15		15		ns
$t_{DH}$	10		12		ns
$t_{DS}$	0		0		ns
$t_{OD}$	0	15	0	15	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{OE}$		15		20	ns
$t_{OEH}$	12		12		ns
$t_{RAC}$		60		70	ns
$t_{RAD}$	12	30	12	35	ns
$t_{RAH}$	10		10		ns
$t_{RAL}$	30		35		ns
$t_{RAS}$	60	10,000	70	10,000	ns
$t_{RCD}$	14	45	14	50	ns
$t_{RCS}$	0		0		ns
$t_{RP}$	40		50		ns
$t_{RSH}$	13		15		ns
$t_{RWC}$	145		170		ns
$t_{RWD}$	80		90		ns
$t_{RWL}$	15		15		ns
$t_{WP}$	10		12		ns
$t_{WRH}$	10		10		ns
$t_{WRP}$	10		10		ns

**EDO-PAGE-MODE READ CYCLE**



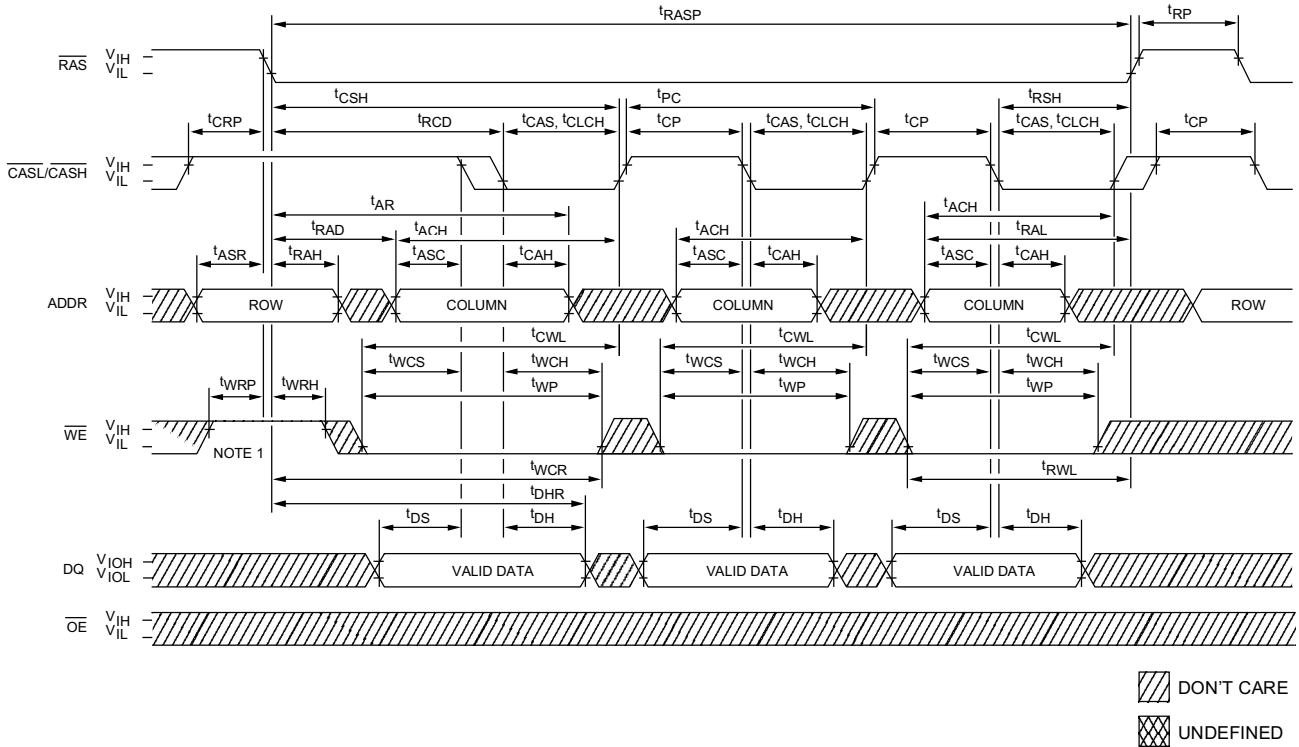
**NOTE:** 1. Although  $\overline{WE}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (READ or WRITE), the system designer should implement  $\overline{WE}$  HIGH for  $t_{WRP}$  and  $t_{WRH}$ . This design implementation will facilitate compatibility with future EDO DRAMs.

**TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t <sub>AA</sub>		30		35	ns
t <sub>ACH</sub>	15		15		ns
t <sub>AR</sub>	45		50		ns
t <sub>ASC</sub>	0		0		ns
t <sub>ASR</sub>	0		0		ns
t <sub>CAC</sub>		15		20	ns
t <sub>CAH</sub>	10		12		ns
t <sub>CAS</sub>	12	10,000	13	10,000	ns
t <sub>CLCH</sub>	10		10		ns
t <sub>CLZ</sub>	0		0		ns
t <sub>COH</sub>	3		3		ns
t <sub>CP</sub>	10		10		ns
t <sub>CPA</sub>		35		40	ns
t <sub>CRP</sub>	5		5		ns
t <sub>CSH</sub>	50		55		ns
t <sub>OD</sub>	0	15	0	15	ns
t <sub>OE</sub>		15		20	ns
t <sub>OEHC</sub>	10		10		ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t <sub>OEP</sub>	10		10		ns
t <sub>OES</sub>	5		5		ns
t <sub>OFF</sub>	3	15	3	15	ns
t <sub>PC</sub>	25		30		ns
t <sub>RAC</sub>		60		70	ns
t <sub>RAD</sub>	12	30	12	35	ns
t <sub>RAH</sub>	10		10		ns
t <sub>RAL</sub>	30		35		ns
t <sub>RASP</sub>	60	125,000	70	125,000	ns
t <sub>RCD</sub>	14	45	14	50	ns
t <sub>RCH</sub>	0		0		ns
t <sub>RCS</sub>	0		0		ns
t <sub>RP</sub>	40		50		ns
t <sub>RRH</sub>	0		0		ns
t <sub>RSH</sub>	13		15		ns
t <sub>WRH</sub>	10		10		ns
t <sub>WRP</sub>	10		10		ns

**EDO-PAGE-MODE EARLY-WRITE CYCLE**



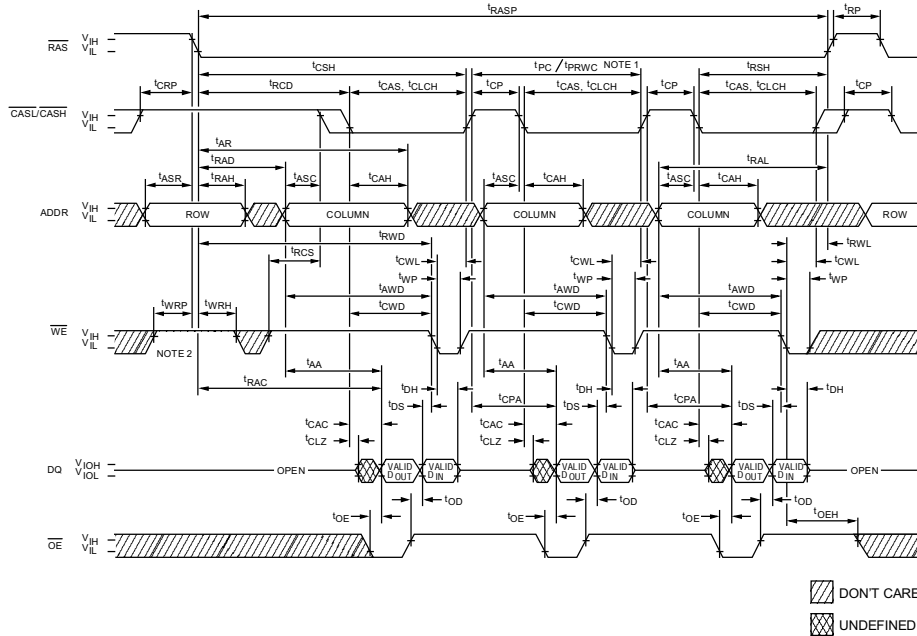
**NOTE:** 1. Although  $\overline{WE}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (READ or WRITE), the system designer should implement  $\overline{WE}$  HIGH for  $t_{WRP}$  and  $t_{WRH}$ . This design implementation will facilitate compatibility with future EDO DRAMs.

**TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{ACH}$	15		15		ns
$t_{AR}$	45		50		ns
$t_{ASC}$	0		0		ns
$t_{ASR}$	0		0		ns
$t_{CAH}$	10		12		ns
$t_{CAS}$	12	10,000	13	10,000	ns
$t_{CLCH}$	10		10		ns
$t_{CP}$	10		10		ns
$t_{CRP}$	5		5		ns
$t_{CSH}$	50		55		ns
$t_{CWL}$	15		15		ns
$t_{DH}$	10		12		ns
$t_{DHR}$	45		55		ns
$t_{DS}$	0		0		ns
$t_{PC}$	25		30		ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{RAD}$	12	30	12	35	ns
$t_{RAH}$	10		10		ns
$t_{RAL}$	30		35		ns
$t_{RASP}$	60	125,000	70	125,000	ns
$t_{RCD}$	14	45	14	50	ns
$t_{RP}$	40		50		ns
$t_{RSH}$	13		15		ns
$t_{RWL}$	15		15		ns
$t_{WCH}$	10		12		ns
$t_{WCR}$	45		55		ns
$t_{WCS}$	0		0		ns
$t_{WP}$	10		12		ns
$t_{WRH}$	10		10		ns
$t_{WRP}$	10		10		ns

**EDO-PAGE-MODE READ-WRITE CYCLE**  
**(LATE WRITE and READ-MODIFY-WRITE cycles)**



- NOTE:**
1.  $t_{PC}$  is for LATE WRITE cycles only.
  2. Although  $\overline{WE}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (READ or WRITE), the system designer should implement  $\overline{WE}$  HIGH for  $t_{WRP}$  and  $t_{WRH}$ . This design implementation will facilitate compatibility with future EDO DRAMs.

**TIMING PARAMETERS**

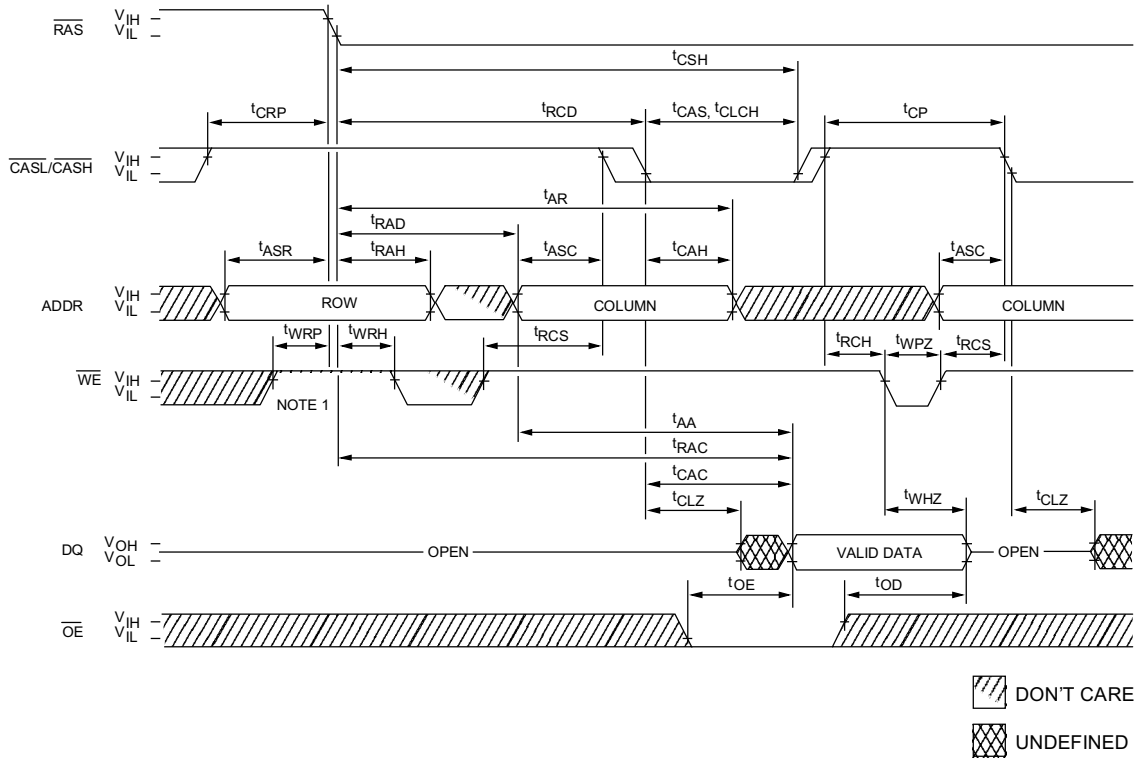
SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{AA}$		30		35	ns
$t_{AR}$	45		50		ns
$t_{ASC}$	0		0		ns
$t_{ASR}$	0		0		ns
$t_{AWD}$	55		60		ns
$t_{CAC}$		15		20	ns
$t_{CAH}$	10		12		ns
$t_{CAS}$	12	10,000	13	10,000	ns
$t_{CLCH}$	10		10		ns
$t_{CLZ}$	0		0		ns
$t_{CP}$	10		10		ns
$t_{CPA}$		35		40	ns
$t_{CRP}$	5		5		ns
$t_{CSH}$	50		55		ns
$t_{CWD}$	35		40		ns
$t_{CWL}$	15		15		ns
$t_{DH}$	10		12		ns
$t_{DS}$	0		0		ns
$t_{OD}$	0	15	0	15	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{OE}$		15		20	ns
$t_{OEHL}$	12		12		ns
$t_{PC}$	25		30		ns
$t_{PRWC}$	75		85		ns
$t_{RAC}$		60		70	ns
$t_{RAD}$	12	30	12	35	ns
$t_{RAH}$	10		10		ns
$t_{RAL}$	30		35		ns
$t_{RASP}$	60	125,000	70	125,000	ns
$t_{RCD}$	14	45	14	50	ns
$t_{RCS}$	0		0		ns
$t_{RP}$	40		50		ns
$t_{RSH}$	13		15		ns
$t_{RWD}$	80		90		ns
$t_{RWL}$	15		15		ns
$t_{WP}$	10		12		ns
$t_{WRH}$	10		10		ns
$t_{WRP}$	10		10		ns





**READ CYCLE**  
(with  $\overline{WE}$ -controlled disable)



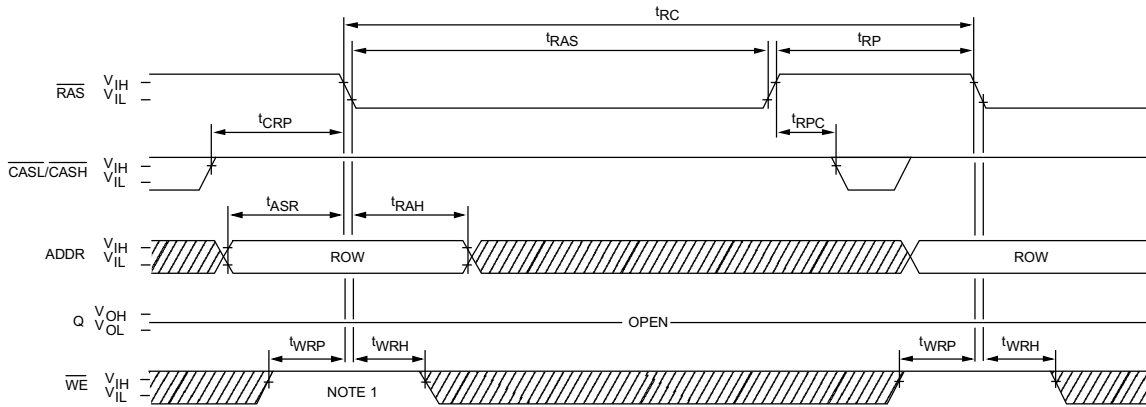
**NOTE:** 1. Although  $\overline{WE}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (READ or WRITE), the system designer should implement  $\overline{WE}$  HIGH for  $tWRP$  and  $tWRH$ . This design implementation will facilitate compatibility with future EDO DRAMs.

**TIMING PARAMETERS**

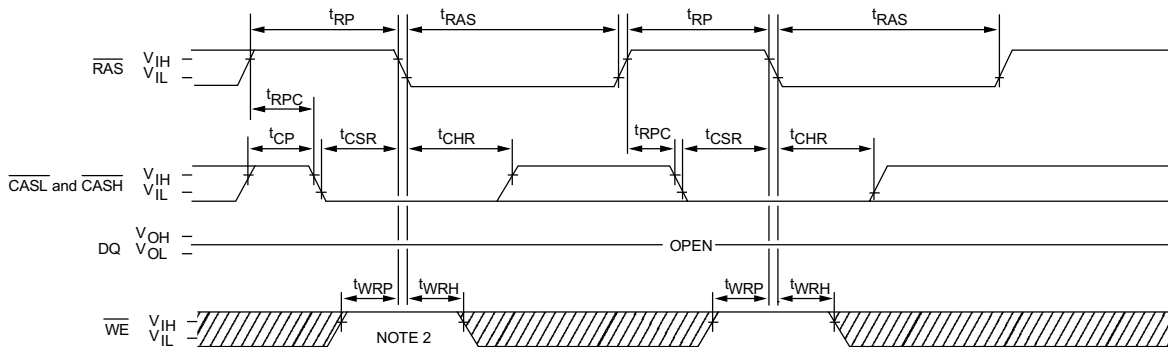
SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{AA}$		30		35	ns
$t_{AR}$	45		50		ns
$t_{ASC}$	0		0		ns
$t_{ASR}$	0		0		ns
$t_{CAC}$		15		20	ns
$t_{CAH}$	10		12		ns
$t_{CAS}$	12	10,000	13	10,000	ns
$t_{CLCH}$	10		10		ns
$t_{CLZ}$	0		0		ns
$t_{CP}$	10		10		ns
$t_{CRP}$	5		5		ns
$t_{CSH}$	50		55		ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{OD}$	0	15	0	15	ns
$t_{OE}$		15		20	ns
$t_{RAC}$		60		70	ns
$t_{RAD}$	12	30	12	35	ns
$t_{RAH}$	10		10		ns
$t_{RCD}$	14	45	14	50	ns
$t_{RCH}$	0		0		ns
$t_{RCS}$	0		0		ns
$t_{WHZ}$	0	13	0	15	ns
$t_{WPZ}$	10		12		ns
$t_{WRH}$	10		10		ns
$t_{WRP}$	10		10		ns

**RAS-ONLY REFRESH CYCLE**



**CBR REFRESH CYCLE**  
(Addresses and  $\overline{OE}$  = DON'T CARE)



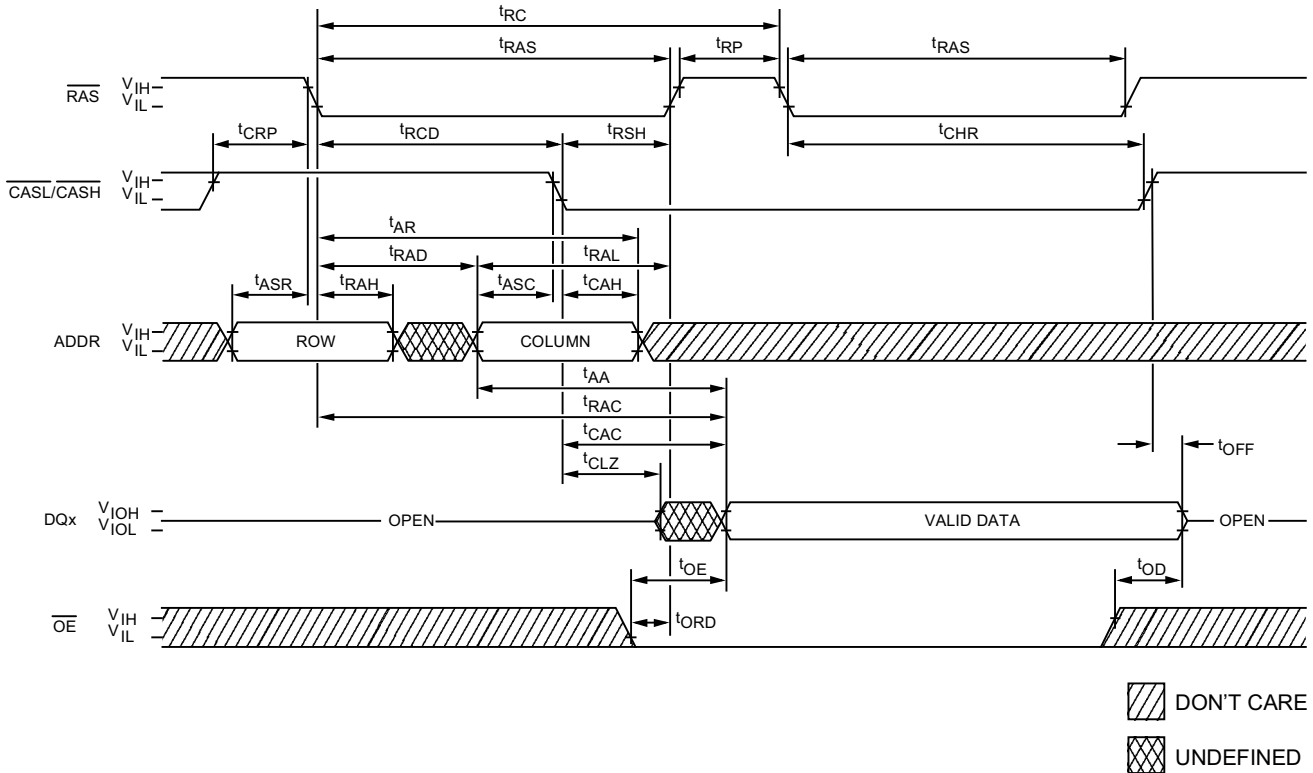
- NOTE:**
1. Although  $\overline{WE}$  is a "don't care" at  $\overline{RAS}$  time during an access cycle (READ or WRITE), the system designer should implement  $\overline{WE}$  HIGH for  $tWRP$  and  $tWRH$ . This design implementation will facilitate compatibility with future EDO DRAMs.
  2.  $tWRP$  and  $tWRH$  are for system design reference only. The  $\overline{WE}$  signal is actually a "don't care" at  $\overline{RAS}$  time during a CBR REFRESH. However,  $\overline{WE}$  should be held HIGH at  $\overline{RAS}$  time during a CBR REFRESH to ensure compatibility with other DRAMs that require  $\overline{WE}$  HIGH at  $\overline{RAS}$  time during a CBR REFRESH.

**TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{ASR}$	0		0		ns
$t_{CHR}$	10		12		ns
$t_{CP}$	10		10		ns
$t_{CRP}$	5		5		ns
$t_{CSR}$	5		5		ns
$t_{RAH}$	10		10		ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
$t_{RAS}$	60	10,000	70	10,000	ns
$t_{RC}$	105		125		ns
$t_{RP}$	40		50		ns
$t_{RPC}$	5		5		ns
$t_{WRH}$	10		10		ns
$t_{WRP}$	10		10		ns

**HIDDEN REFRESH CYCLE** <sup>32</sup>  
( $\overline{WE}$  = HIGH;  $\overline{OE}$  = LOW)

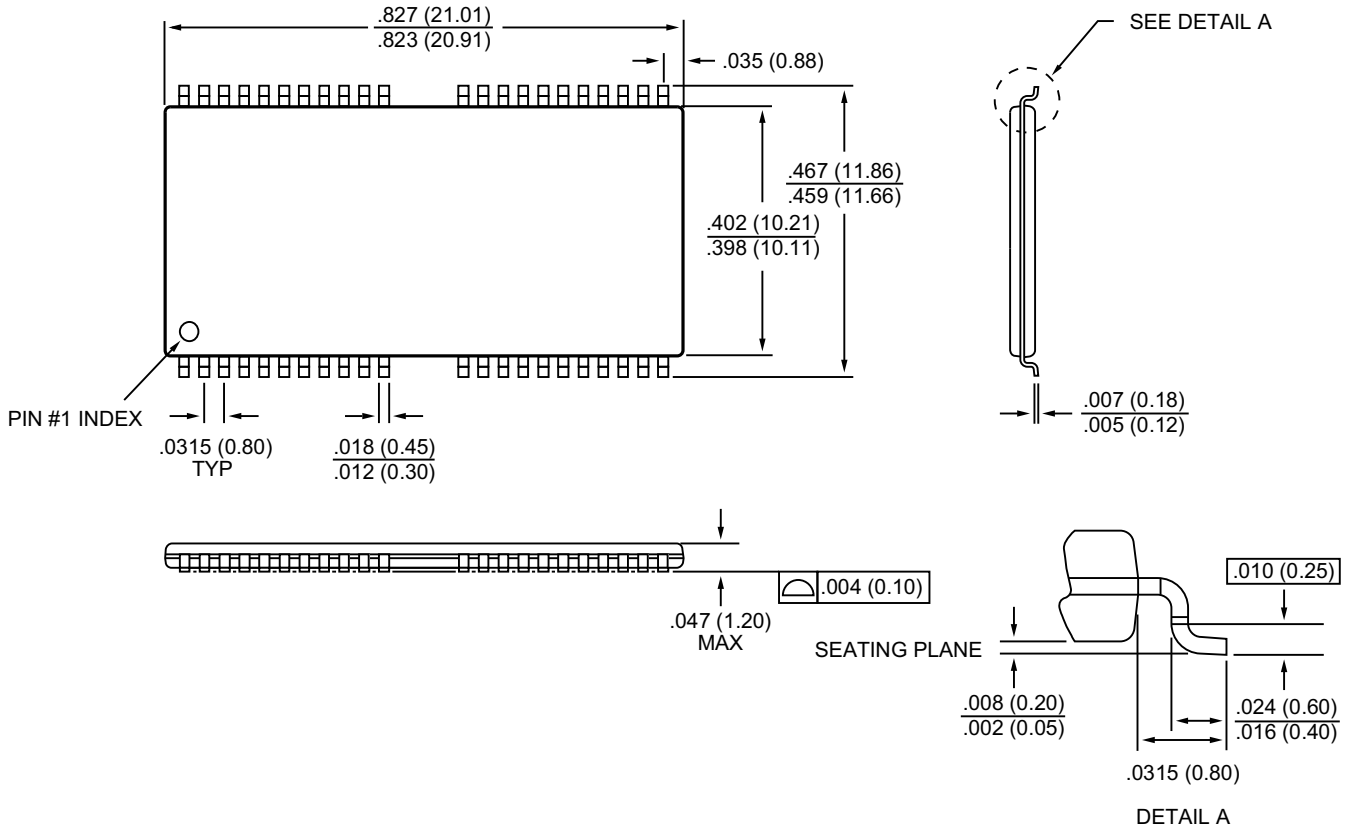


**TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		12		ns
tCHR	10		12		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tOD	0	15	0	15	ns
tOE		15		20	ns

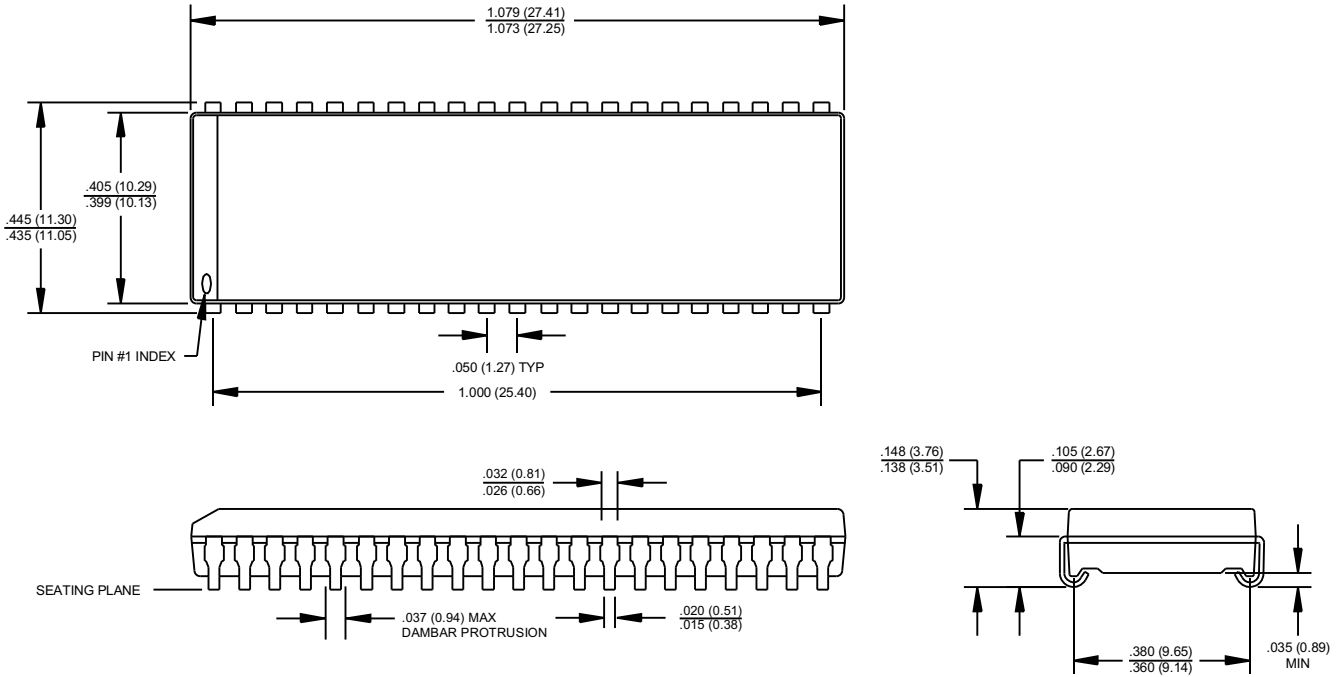
SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tOFF	3	15	3	15	ns
tORD	0		0		ns
tRAC		60		70	ns
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC	105		125		ns
tRCD	14	45	14	50	ns
tRP	40		50		ns
tRSH	13		15		ns

**44/50-PIN PLASTIC TSOP (400 mil)**  
**DB-5**



- NOTE:**
1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.
  2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

**42-PIN PLASTIC SOJ (400 mil)**  
**DA-7**



- NOTE:**
1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.
  2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.