DRAM

64K x 1 DRAM

PAGE MODE

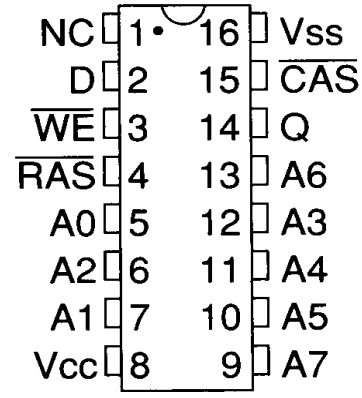
FEATURES

- Industry standard pinout, functions and timing
- Single +5V ±10% power supply
- Low power, 15mW standby; 75mW active, typical
- Common I/O using EARLY-WRITE
- Q held indefinitely by $\overline{CAS}$
- 256-cycle refresh in 4ms
- Fully compatible with MT1259 (256K)
- Optional PAGE MODE access cycle

OPTIONS	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
200ns access	-20
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

16-Pin DIP
(A-1, B-1)



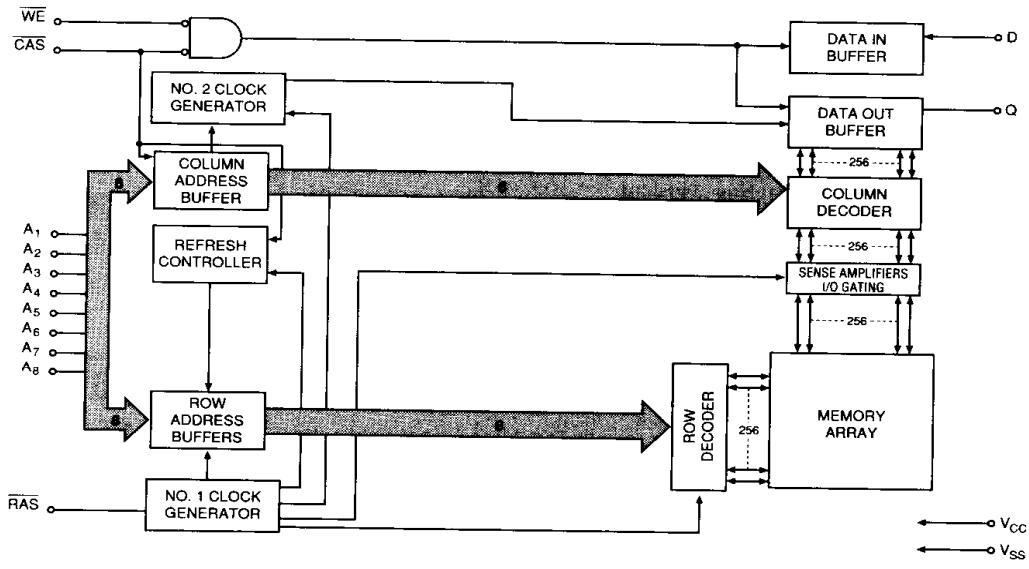
GENERAL DESCRIPTION

The MT4264 is a randomly accessed solid-state memory containing 65,536 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 16 address bits, which are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY or HIDDEN REFRESH) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 4ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	Addresses		
				t_R	t_C	
Standby	H	X	X	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS-ONLY REFRESH	L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 4, 6) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}); I all other pins not under test = 0V	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled; 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}		4	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ Cycling)	I_{CC2}		30	mA	2
$\overline{RAS}$-ONLY REFRESH CURRENT ($\overline{CAS}$ = V_{IH})	I_{CC3}		20	mA	2
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling)	I_{CC4}		30	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7, D	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	18
Output Capacitance: Q	C_O		8	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

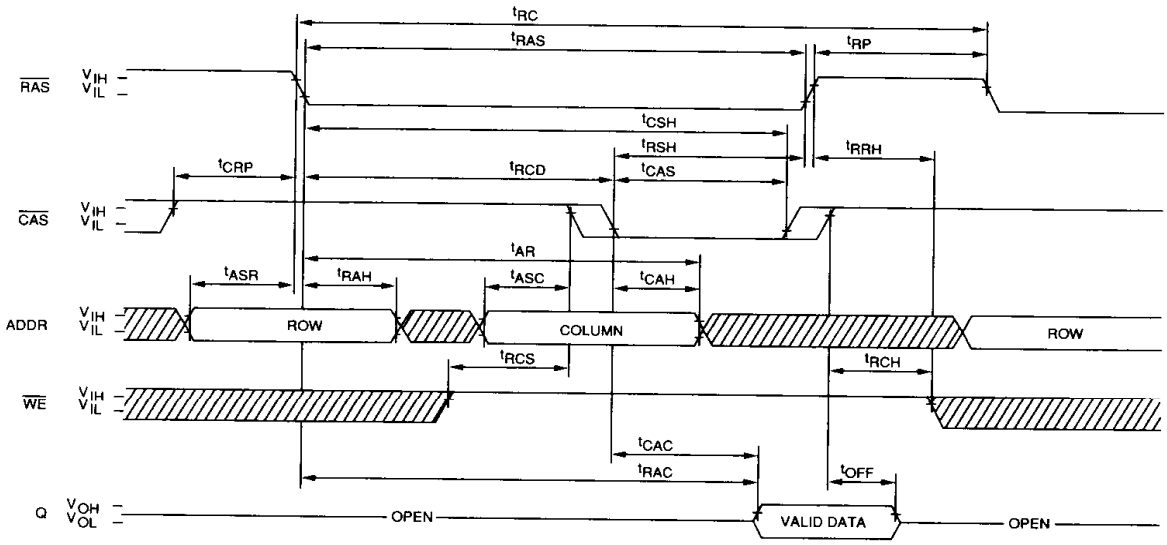
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15		-20			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	195		230		260		330		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	220		255		295		370		ns	
PAGE-MODE cycle time	^tPC	90		100		120		170		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		100		120		150		200	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		50		60		75		120	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		100		ns	
$\overline{RAS}$ precharge time	^tRP	80	20,000	90	20,000	100	20,000	120	20,000	ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	120	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		200		ns	
$\overline{CAS}$ precharge time	^tCPN	25		25		30		35		ns	19
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	30		30		35		40		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	25	50	25	60	25	75	30	80	ns	13
Row address setup time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		20		25		ns	
Column address setup time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	20		20		25		50		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	70		80		100		130		ns	
READ command setup time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	30	0	30	0	35	0	40	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	35		40		45		60		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	85		100		120		140		ns	
WRITE command pulse width	^tWP	35		40		45		50		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		40		45		55		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		40		45		55		ns	
Data-in setup time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	35		40		45		55		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	85		100		120		135		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	40		50		60		100		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	90		110		135		180		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ to $\overline{RAS}$ setup time	^tCRP	10		15		20		20		ns	

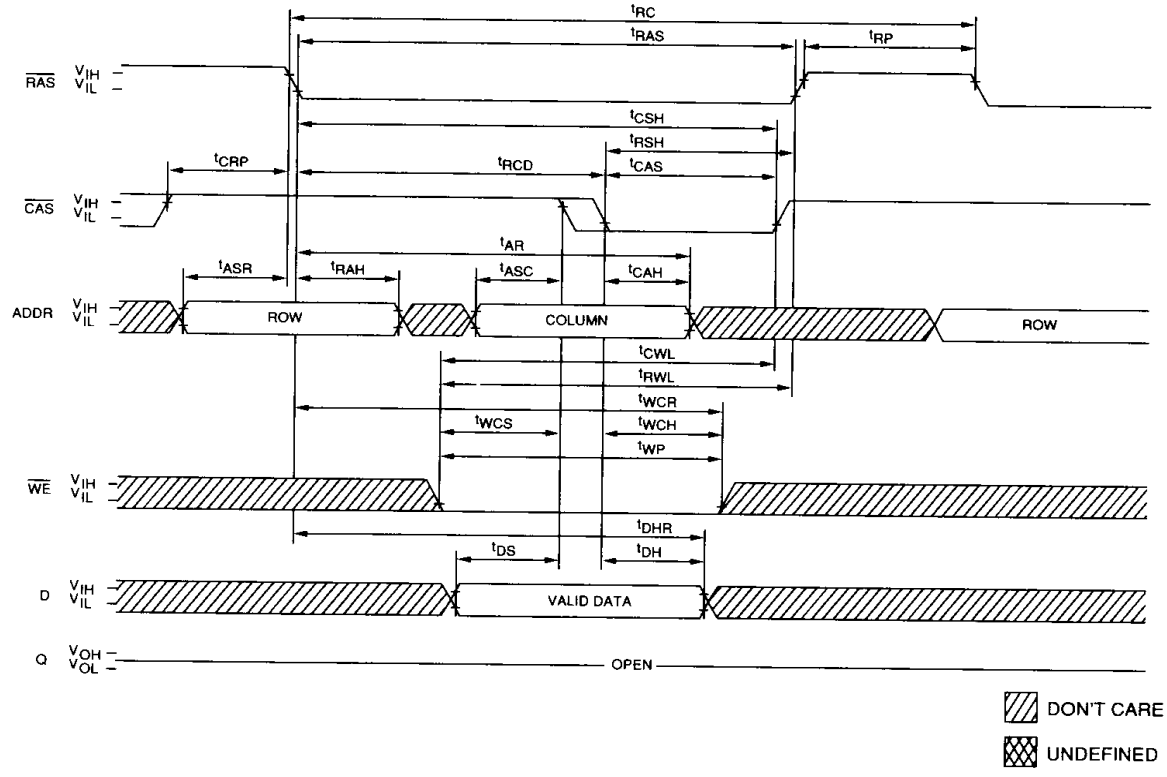
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
16. ^tWCS, ^tRWD and ^tCWD are restrictive operating parameters in late READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq {}^tCWD$ (MIN) and $^tRWD \geq {}^tRWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.

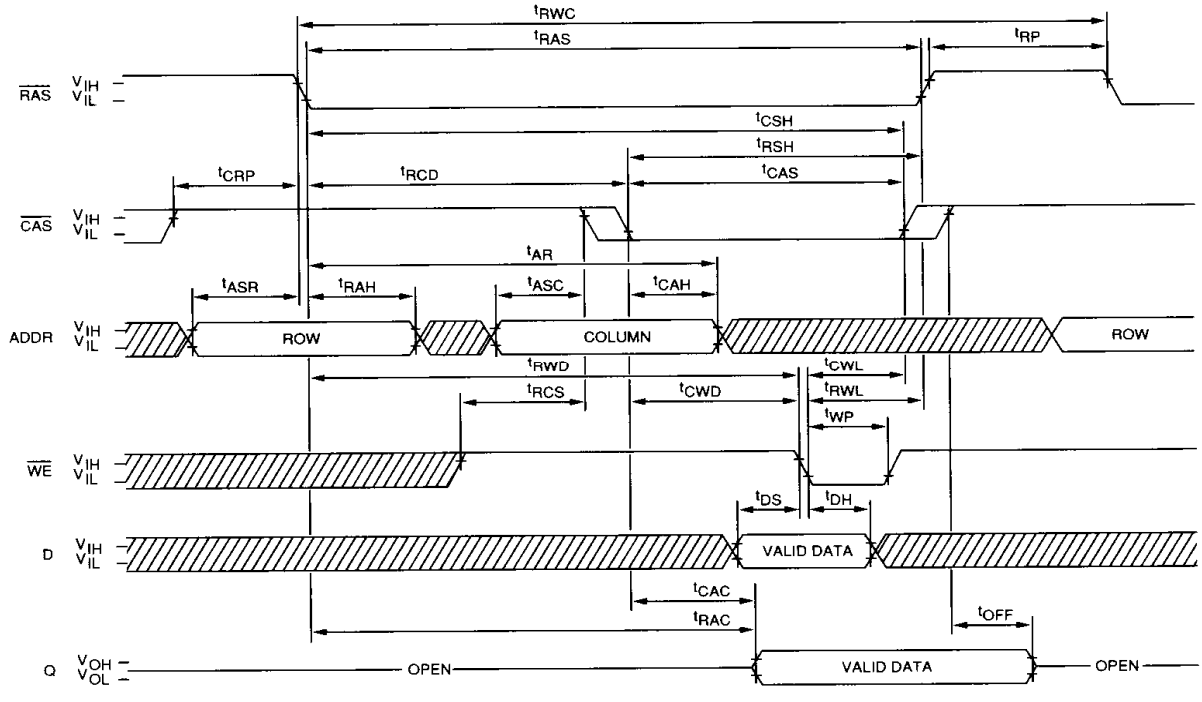
READ CYCLE



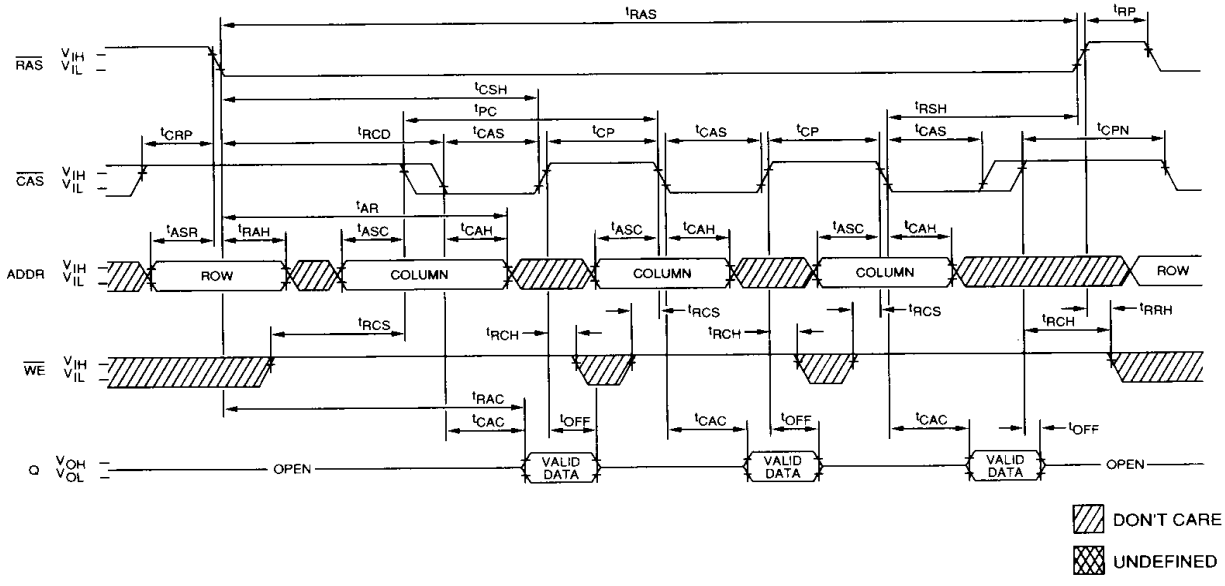
EARLY-WRITE CYCLE



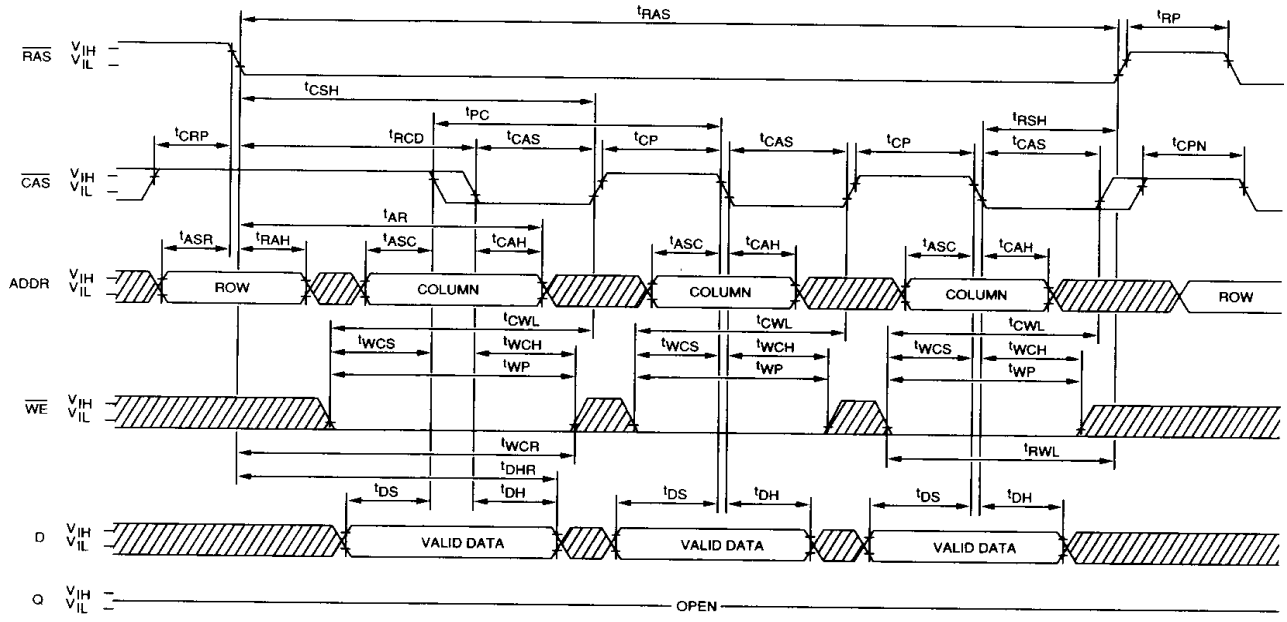
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



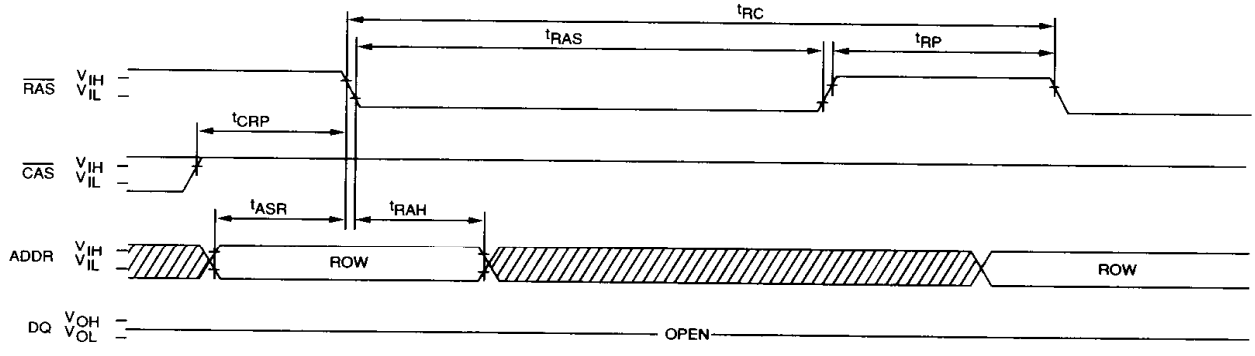
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_7)



DON'T CARE

UNDEFINED