

MSM6810/6811/6812/6813

Single Chip CODEC

GENERAL DESCRIPTION

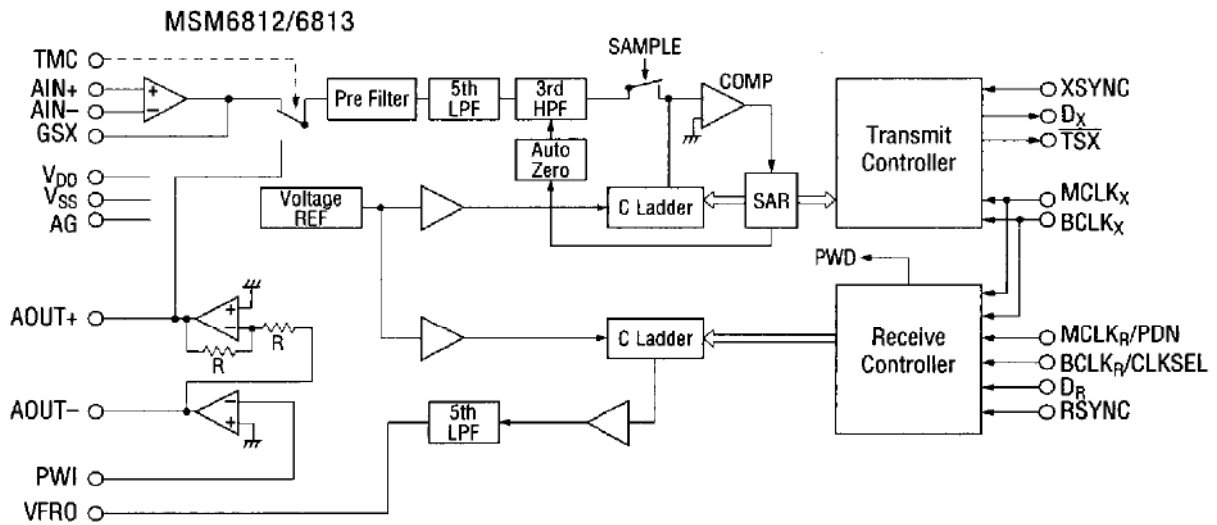
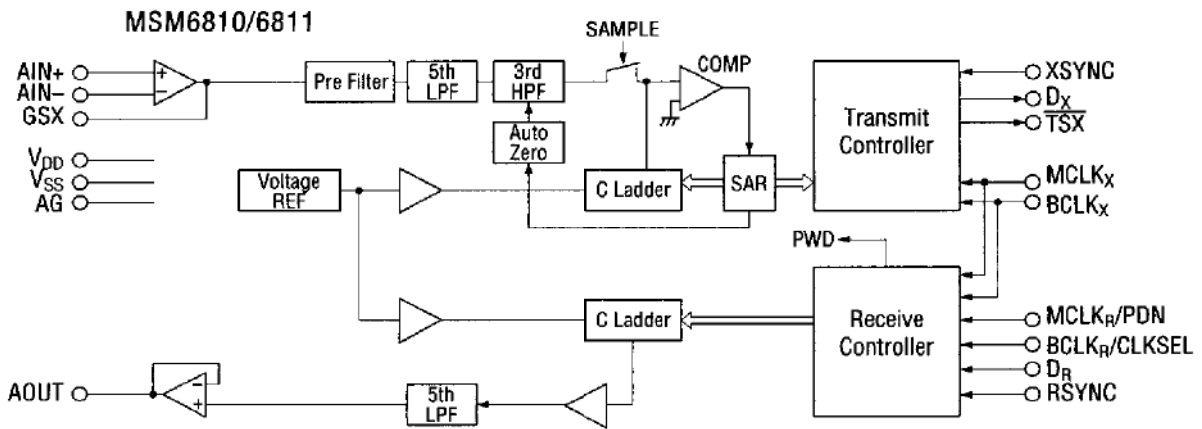
The MSM6810/6811/6812/6813 are a single-channel CODEC CMOS ICs containing filters for A/D and D/A converting of the voice signal ranging from 300 Hz to 3400 Hz.

FEATURES

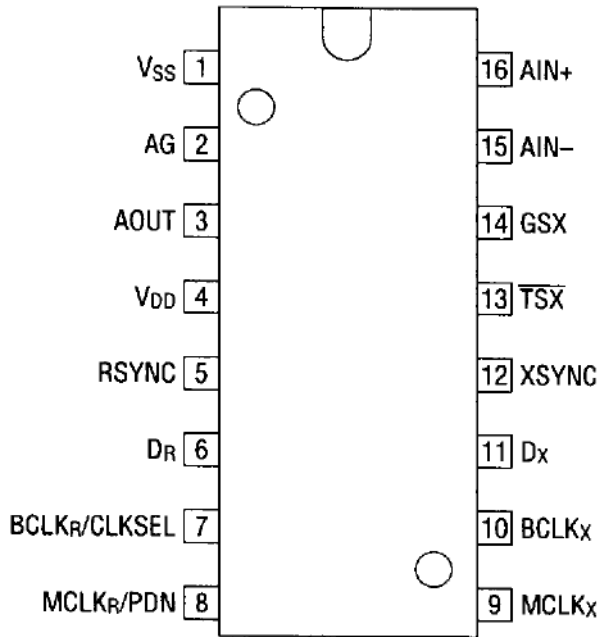
- Compliance with ITU-T companding Law
 - MSM6810/MSM6812 : μ -law
 - MSM6811/MSM6813 : A-law
- Capable of independent operation of transmission and reception
- Transmission clock in the range of 64 kHz to 2048 kHz
- Adjustable Transmit/Receive level
- 300 Ω drive for analog output
 - MSM6810/MSM6811 single end drive
 - MSM6812/MSM6813 Push-pull drive
- Built-in analog loop back function
 - MSM6812/MSM6813
- Built-in reference voltage source
- Low Power Dissipation (60 mW to 70 mW Typ.)
(MSM6810/MSM6811)
- Package options :
 - 16-pin plastic DIP (DIP16-P-300)
 - 16-pin ceramic DIP (DIP16-G-300)
 - 24-pin plastic SOP (SOP24-P-430-VK)
(MSM6812/MSM6813)
- Package options :
 - 20-pin plastic skinny DIP (DIP20-P-300-S1)
 - 24-pin plastic SOP (SOP24-P-430-VK)

Note: The product names are indicated in PIN CONFIGURATION.

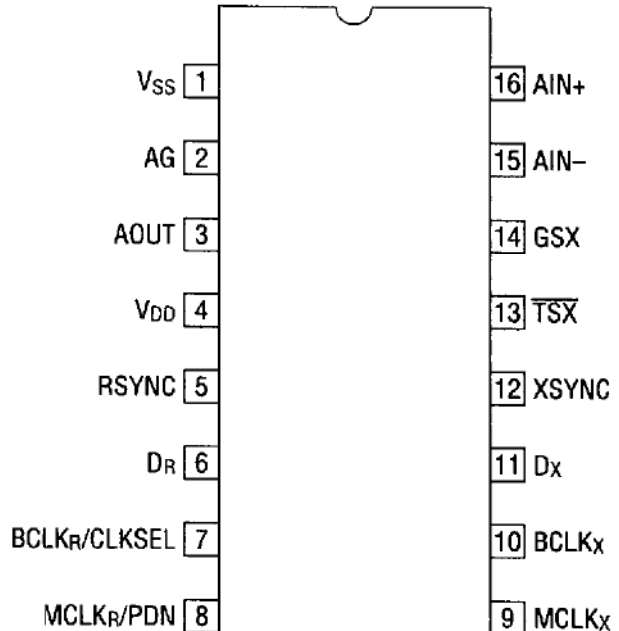
BLOCK DIAGRAM



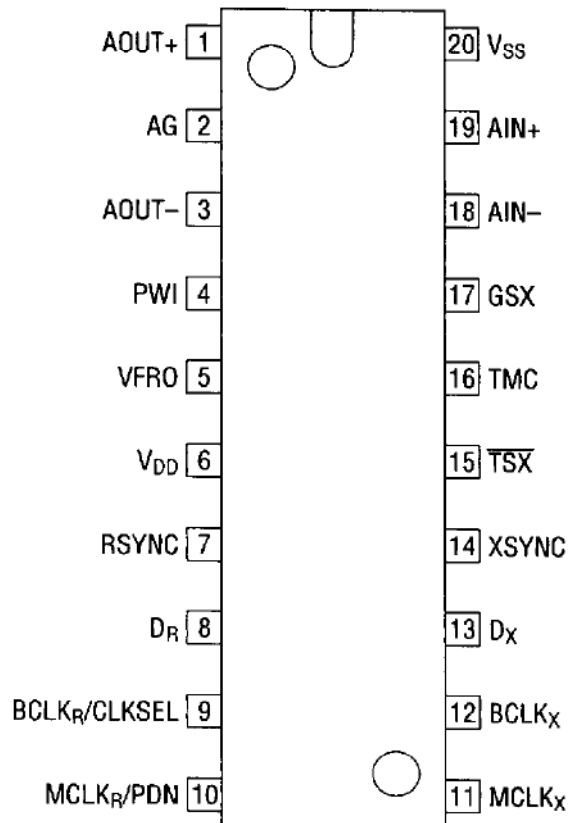
PIN CONFIGURATION (TOP VIEW)



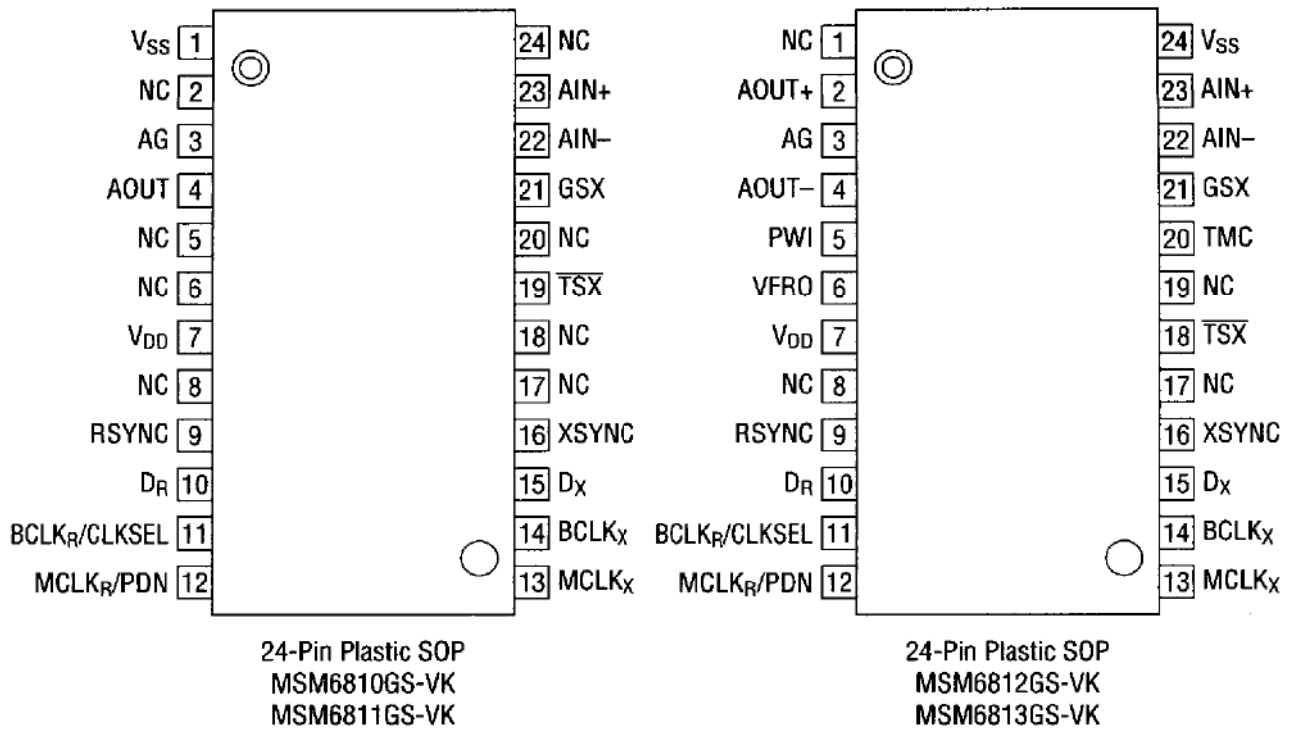
16-Pin Plastic DIP
MSM6810RS
MSM6811RS



16-Pin Ceramic DIP
MSM6810AS
MSM6811AS



20-Pin Plastic Skinny DIP
MSM6812RS
MSM6813RS



NC : No connect pin

PIN AND FUNCTIONAL DESCRIPTIONS

V_{DD}

Positive voltage power supply.
The range of supply voltage is $+5\text{ V} \pm 5\%$.

V_{SS}

Negative voltage power supply.
The range of power supply voltage is $-5\text{ V} \pm 5\%$.

AG

AG is an analog ground.
AG is connected to the analog system ground.

AIN+, AIN-, GSX

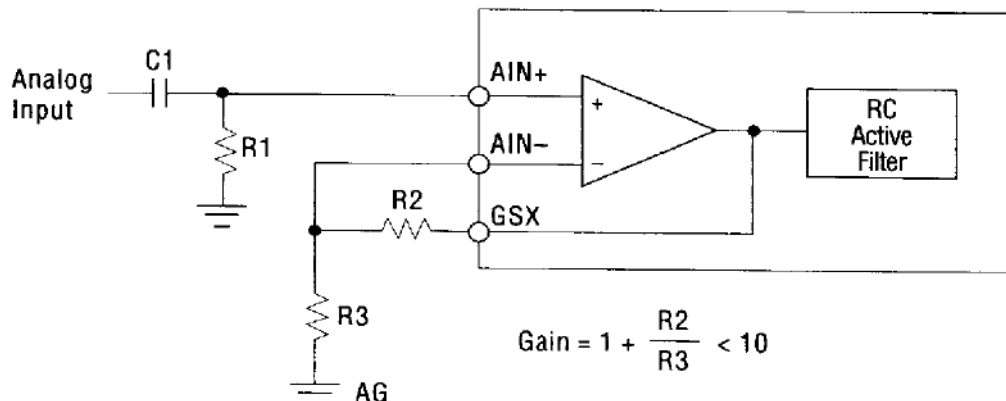
These three pins are used for the transmit level adjustment.

AIN+ is a non-inverting analog input pin which is connected to the non-inverting input of a transmit amplifier.

AIN- is an inverting analog input pin which is connected to the inverting input of the transmit amplifier.

GSX is a transmit amplifier output pin.

Adjustment can be done by following method.



- Notes:
1. $R_2 + R_3 > 10\text{ k}\Omega$
 2. When the DC off-set voltage of analog input is more than 20 mV, C1 and R1 should provide for DC blocking.
In this case, cut-off frequency of HPF, composed by R1 and C1, should be less than 30 Hz.
 3. R1 should be less than 20 k Ω

VFRO

Receive filter output for the MSM6812/6813.

Voltage swing of output signal is 5 V_{P-P} at maximum. It can drive a resistor of 10 k Ω or more. This output is in a high impedance state when powered down.

AOUT

Receive analog signal output for the MSM6810/6811.

The maximum output signal swing is 5 V_{P-P}. These output can drive a 300 Ω resistor or more.

PWI, AOUT+, AOUT-

PWI is connected to the inverting input of the receive driver.

The receive driver output is connected to the AOUT+ pin. Thus, the receive level can be adjusted with the pins VFRO, PWI, and AOUT-. The output of AOUT+ is inverted with respect to the output of AOUT-.

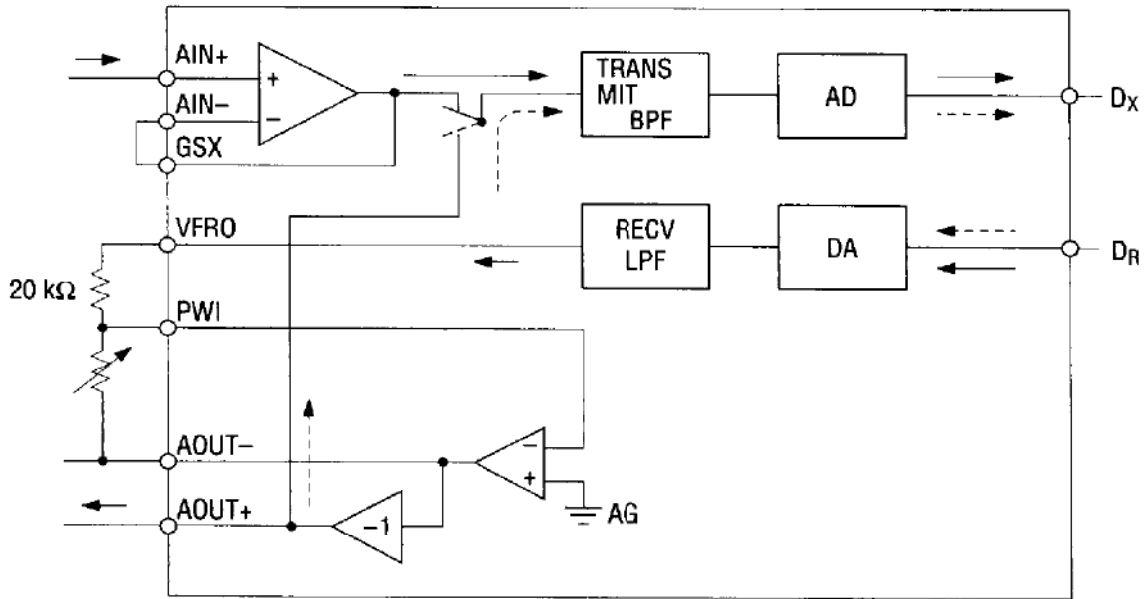
300 Ω	load	6.6 V _{PP}
600 Ω	load	7.0 V _{PP}
> 15 k Ω	load	8.0 V _{PP}

TMC

Control signal input for mode selection.

This pin select the normal operating mode or the analog loop-back mode.

TMC Input	Mode
< 0.6 V	Normal operation
> 2.2 V	Analog loop-back



- ▶ Signal flow in normal operation mode
- - -▶ Signal flow in analog loop-back mode

MCLK_x

Transmit master clock signal input.

This clock is counted down and is used as the clock signal. When synchronous operation, BCLK_R/CLKSEL is used as the selection pin of the master clock frequency.

Table-1

BCLK _R /CLKSEL	Master Clock Frequency	
	MSM6810 MSM6812 (μ)	MSM6811 MSM6813 (A)
64 kHz to 2048 kHz	1536 or 1544 kHz	2048 kHz
0	2048 kHz	1536 or 1544 kHz
1 or open	1536 or 1544 kHz	2048 kHz

MCLK_x/PDN

Receive master clock signal input.

This clock is counted down and is used as the clock signal, MCLK_R/PDN is used as powered down control.

Table-2

MCLK _R /PDN	Operation
1536, 1544, 2048 kHz	Asynchronous operation
0	Synchronous operation
1	Powered down

BCLK_x

The transmit bit clock signal input which shifts out receive PCM data on D_x.

The clock frequency range is from 64 kHz to 2048 kHz. BCLK_x must be synchronous with XSYNC.