8K x 8 High Speed CMOS Static RAM

Preliminary

FEATURES

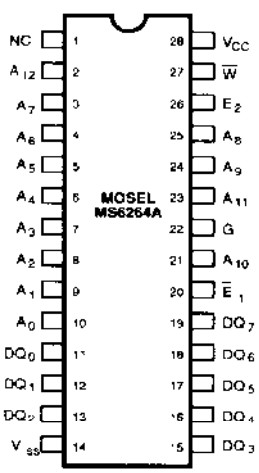
- High-speed – 20/25/30 ns
- Low Power dissipation:
  - 825mW (Max.) Operating
  - 550µW (Max.) Power Down
  - 50µA (Max.) I_{CCDR}
- 5V ± 10% supply
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V
- Pin compatible with 64K bit EPROM

DESCRIPTION

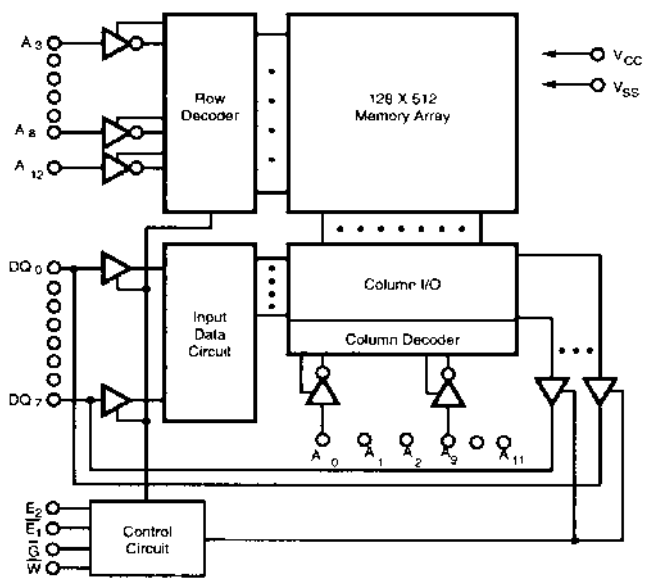
The MOSEL MS6264A is a 65,536-bit static random access memory organized as 8,192 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS6264A is available in the following standard 28-pin packages:

- 600 MIL Plastic DIP
- 300 MIL Plastic DIP
- 300 MIL Small Outline J-Bend (SOJ)
- 300 MIL Small Outline Gullwing (SOG)

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{12} Address Inputs

These 13 address inputs select one of the 8192 x 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input

E_2 Chip Enable 2 Input

$\overline{E}_1$ is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

V_{SS} Ground

TRUTH TABLE

MODE	W	E_1	E_2	G	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-40 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability, and degrade performance characteristics.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MS6264A MIN.	TYP.(1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)			-0.5	-	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)			2.2	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}		-	-	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $\overline{E}_2 = V_{IL}$, or $\overline{G} = V_{IH}$, $V_{I/O}$ = 0V to V_{CC}		-	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA		-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -4mA		2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, $F = F_{max}$(3)		-	-	150	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA		-	-	30	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 \geq V_{CC} - 0.2V$, $E_2 < 0.2V$	L(4)	-	-	100	µA
		$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	S			20	mA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$
4. Low power version only.

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

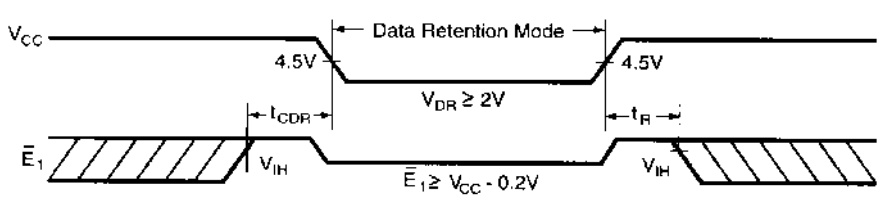
1. This parameter is guaranteed and not tested.

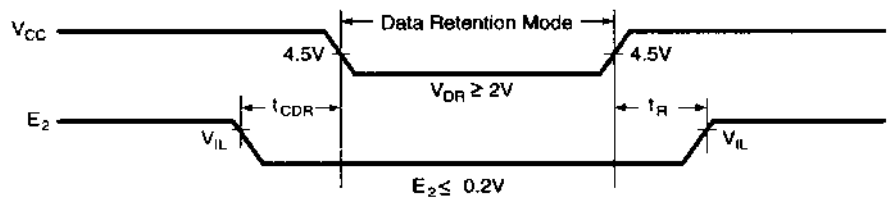
DATA RETENTION CHARACTERISTICS (over the commercial operating range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$E_1 > V_{CC} - 0.2V$, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} < 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$E_1 > V_{CC} - 0.2V$, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	2	50(3)	µA
I_{IL}	Input Leakage Current		-	-	2	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(2)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. For low power version only

LOW V_{CC} DATA RETENTION WAVEFORM ($\overline{E}_1$ Controlled)





AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Timing Reference Level	1.5V

AC TEST LOADS AND WAVEFORMS

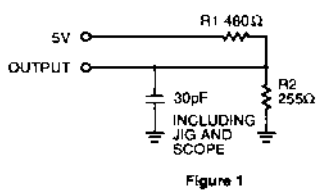


Figure 1

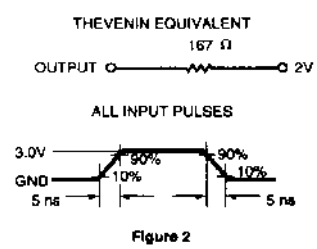
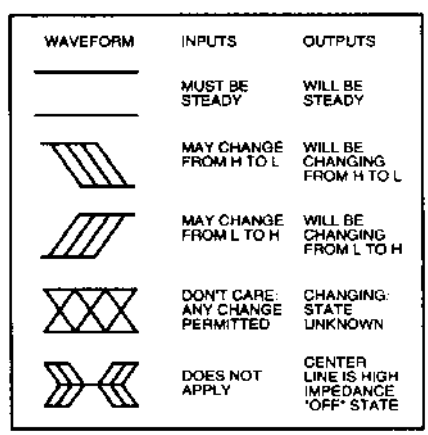


Figure 2

KEY TO SWITCHING WAVEFORMS



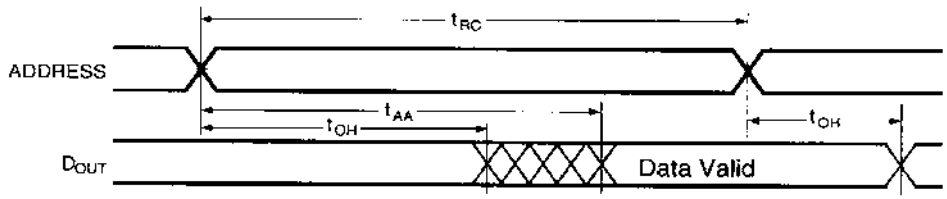
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

READ CYCLE

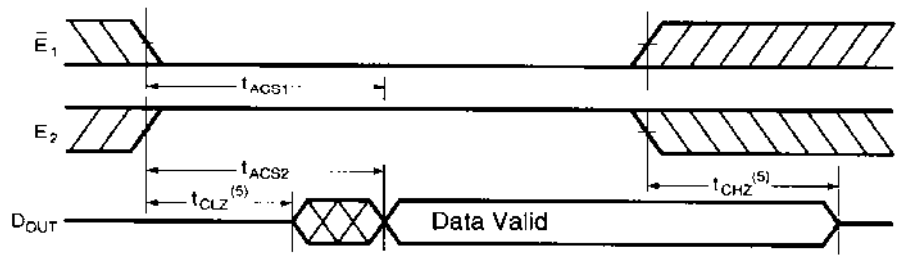
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6264A-20		MS6264A-25		MS6264A-30		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time	20	-	25	-	30	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	20	-	25	-	30	ns
t_{ELQV}	t_{ACS1}	Chip Enable Access Time	-	20	-	25	-	30	ns
t_{ELQV}	t_{ACS2}	Chip Enable Access Time	-	22	-	27	-	32	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-	10	-	15	-	15	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	5	-	5	-	5	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	0	-	0	-	0	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	-	10	-	15	-	15	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	10	-	15	-	15	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	5	-	5	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

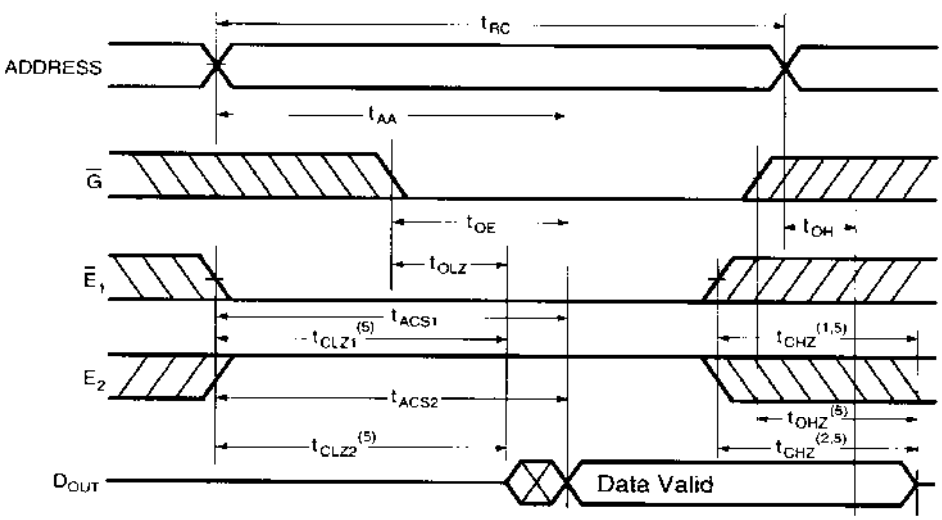
READ CYCLE 1[1, 2, 4]



READ CYCLE 2[1]



READ CYCLE 3[1, 3, 4]



Notes:
1. $\overline{W}$ is high during all read cycles.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and /or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured +500mV from steady state with C_L = 5pF. This parameter is guaranteed and not 100% tested.

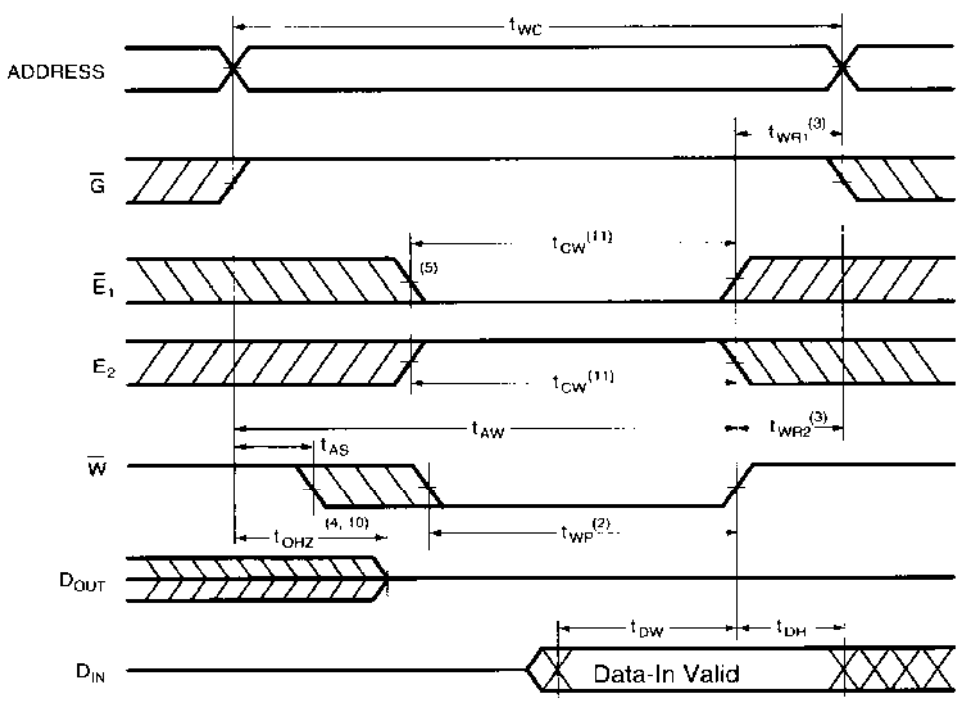
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6264A-20		MS6264A-25		MS6264A-30		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	20	-	25	-	30	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	15	-	20	-	25	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	0	-	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	15	-	20	-	25	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	15	-	20	-	25	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	15	0	20	0	25	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	15	-	20	-	25	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	10	0	15	0	15	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	5	-	5	-	5	-	ns

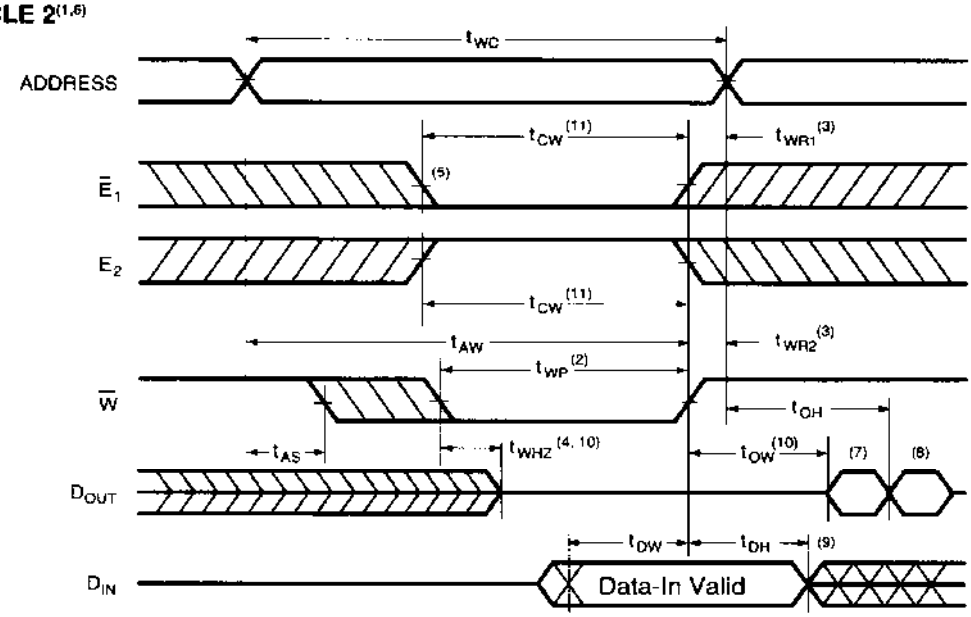
SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[1]



SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 2[1,6]



Notes:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the W low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. G is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outpus must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF. This parameter is guaranteed but not 100% tested.
11. tcw is measured from the later of E_1 going low or E_2 going high to the end of write.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
20	MS6264A-20PC	P28-1	0°C to +70°C
20	MS6264A-20NC	P28-2	0°C to +70°C
20	MS6264A-20RC	R28-1	0°C to +70°C
20	MS6264A-20SC	S28-6	0°C to +70°C
25	MS6264A-25PC	P28-1	0°C to +70°C
25	MS6264A-25NC	P28-2	0°C to +70°C
25	MS6264A-25RC	R28-1	0°C to +70°C
25	MS6264A-25SC	S28-6	0°C to +70°C
30	MS6264A-30PC	P28-1	0°C to +70°C
30	MS6264A-30NC	P28-2	0°C to +70°C
30	MS6264A-30RC	R28-1	0°C to +70°C
30	MS6264A-30SC	S28-6	0°C to +70°C

To order low power device, add "L" after part number and before speed. For example, MS6264AL-20PC.