National Semiconductor

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MM54HC74A/MM74HC74A
Dual D Flip-Flop with Preset and Clear

General Description

The MM54HC74A/MM74HC74A utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

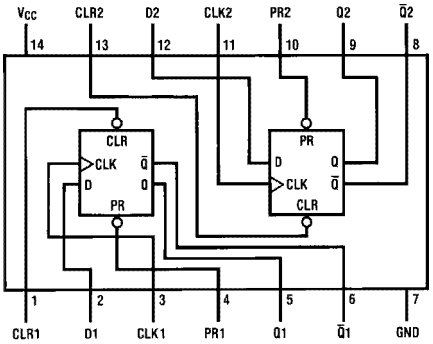
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 40 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



TOP VIEW

TL/F/5106–1

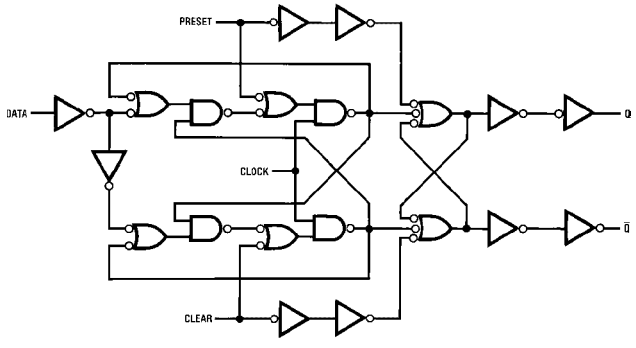
Order Number MM54HC74A or MM74HC74A

Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



TL/F/5106–2

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, $_{OUT}$)		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.3	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

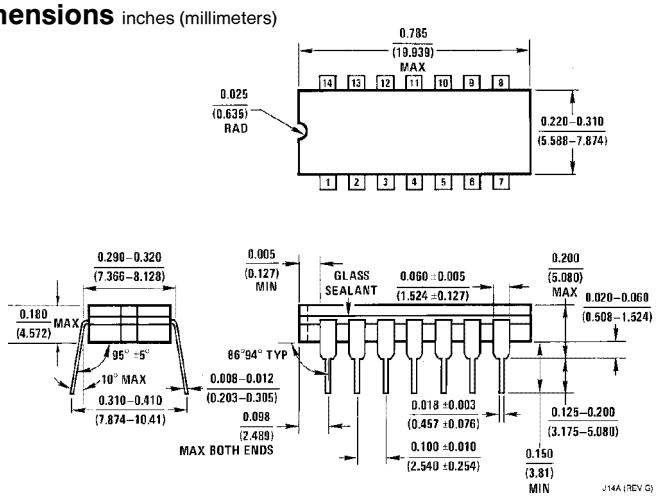
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		72	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		10	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear to Q or $\overline{Q}$		17	40	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock		6	5	ns
t_S	Minimum Setup Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

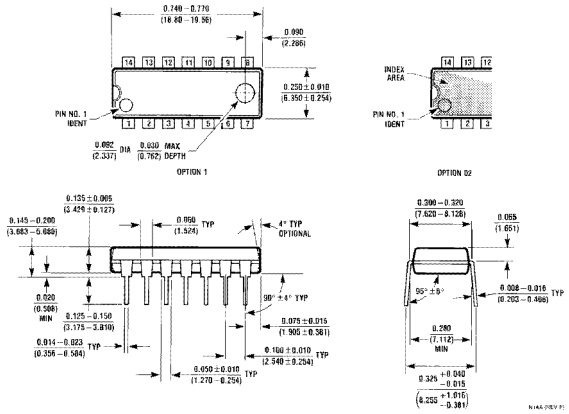
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	22	6	5	4	MHz
			4.5V	72	30	24	20	MHz
			6.0V	94	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	34	110	140	165	ns
			4.5V	12	22	28	33	ns
			6.0V	10	19	24	28	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear To Q or $\overline{Q}$		2.0V	66	150	190	225	ns
			4.5V	20	30	38	45	ns
			6.0V	16	26	33	38	ns
t_{REM}	Minimum Removal Time Preset or Clear To Clock		2.0V	20	50	65	75	ns
			4.5V	6	10	13	15	ns
			6.0V	5	9	11	13	ns
t_S	Minimum Setup Time Data to Clock		2.0V	35	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	17	20	ns
t_H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum, Pulse Width Clock, Preset or Clear		2.0V	30	80	101	119	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters)



Order Number MM54HC74J or MM74HC74J
NS Package J14A



Order Number MM74HC74N
NS Package N14A

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