

## MM54HC688/MM74HC688 8-Bit Magnitude Comparator (Equality Detector)

### General Description

This equality detector utilizes advanced silicon-gate CMOS technology to compare bit for bit two 8-bit words and indicates whether or not they are equal. The  $\overline{P=Q}$  output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

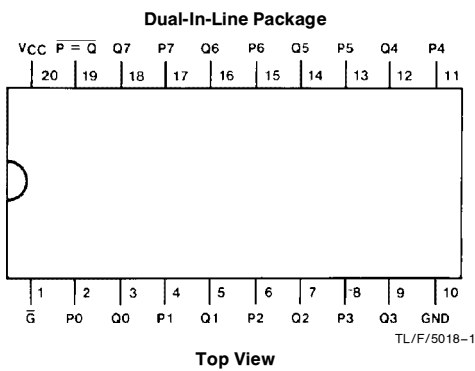
The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin

compatible to the 54LS688/74LS688. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

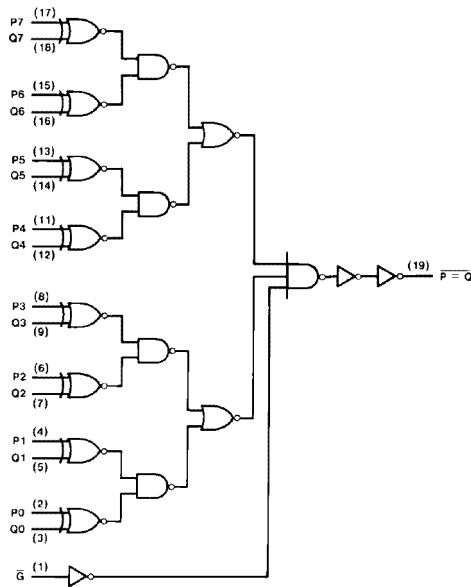
### Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80  $\mu$ A (74 Series)
- Large output current: 4 mA (74 Series)
- Same as 'HC521

### Connection and Logic Diagrams



Order Number MM54HC688 or MM74HC688



### Truth Table

Inputs		$\overline{P=Q}$
Data P,Q	Enable $\overline{G}$	
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

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## Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ ) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. ( $T_L$ ) (Soldering 10 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

## DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			Units	
				Typ	74HC $T_A = -40$ to $85^\circ C$	54HC $T_A = -55$ to $125^\circ C$		
$V_{IH}$	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V	
			4.5V	3.15	3.15	3.15	V	
			6.0V	4.2	4.2	4.2	V	
$V_{IL}$	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V	
			4.5V	1.35	1.35	1.35	V	
			6.0V	1.8	1.8	1.8	V	
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1	V	
			6.0V	0	0.1	0.1	V	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	$\mu A$

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of  $5V \pm 10\%$  the worst case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\* $V_{IL}$  limits are currently tested at 20% of  $V_{CC}$ . The above  $V_{IL}$  specification (30% of  $V_{CC}$ ) will be implemented no later than Q1, CY'89.

## AC Electrical Characteristics

$V_{CC}=5V$ ,  $T_A=25^{\circ}C$ ,  $C_L=15\text{ pF}$ ,  $t_r=t_f=6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, any P or Q to Output		21	30	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Enable to any Output		14	20	ns

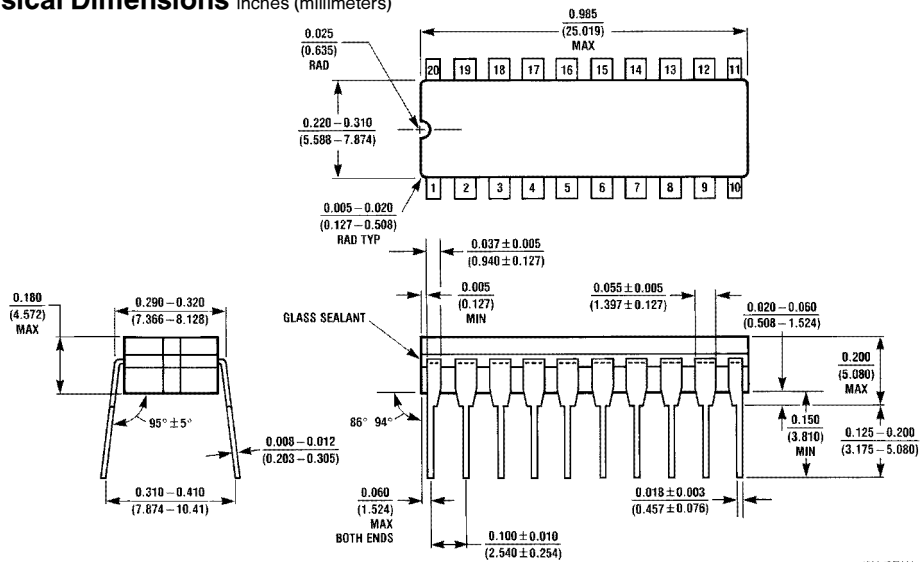
## AC Electrical Characteristics

$V_{CC}=2.0V$  to  $6.0V$ ,  $C_L=50\text{ pF}$ ,  $t_r=t_f=6\text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A=25^{\circ}C$		74HC	54HC	Units
				Typ		$T_A=-40\text{ to }85^{\circ}C$	$T_A=-55\text{ to }125^{\circ}C$	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, P or Q to Output		2.0V	60	175	220	263	ns
			4.5V	22	35	44	53	ns
			6.0V	19	30	38	45	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Enable to Output		2.0V	45	120	150	180	ns
			4.5V	15	24	30	36	ns
			6.0V	13	20	25	30	ns
$t_{THL}$ , $t_{TLH}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)			45				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

Note 5:  $C_{PD}$  determines the no load dynamic power consumption,  $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$ , and the no load dynamic current consumption,  $I_S=C_{PD}V_{CC}f+I_{CC}$ .

## Physical Dimensions inches (millimeters)

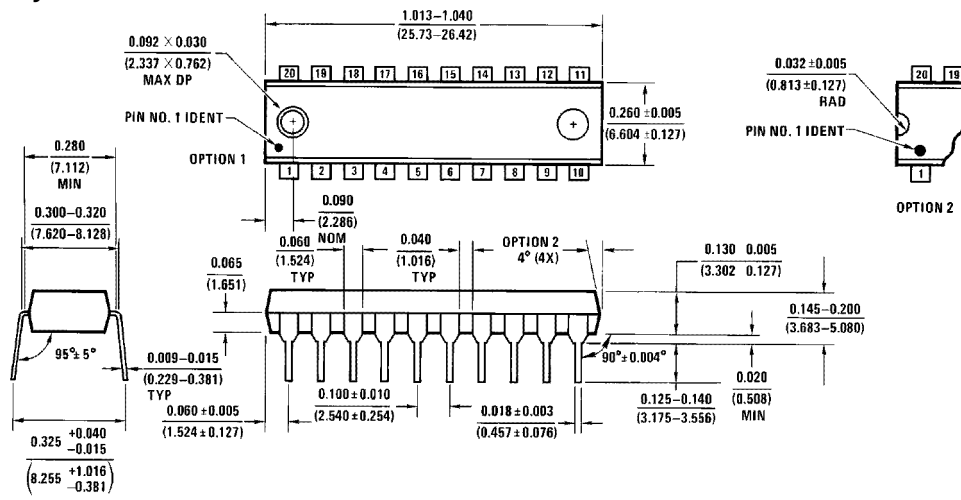


Order Number MM54HC688J or MM74HC688J  
NS Package Number J20A

J20A (REV M)

**MM54HC688/MM74HC688 8-Bit Magnitude Comparator (Equality Detector)**

**Physical Dimensions** inches (millimeters) (Continued)



**Order Number MM74HC688N**  
**NS Package Number N20A**

N20A (REV G)

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