

# MM54HC374/MM74HC374 TRI-STATE® Octal D-Type Flip-Flop

## General Description

These high speed Octal D-Type Flip-Flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

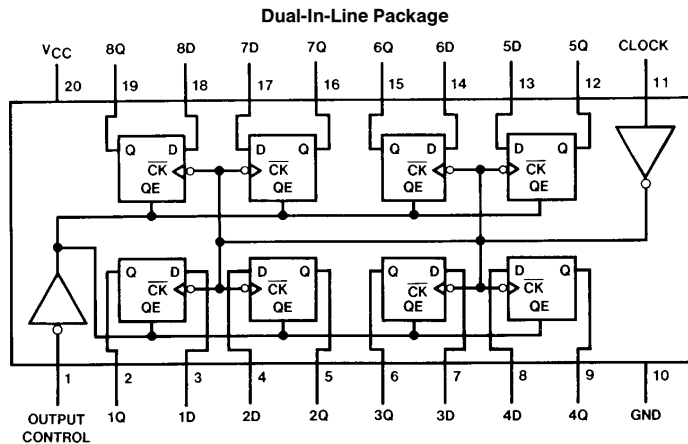
These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

## Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

## Connection Diagram



Top View

TL/F/5336-1

Order Number MM54HC374 or MM74HC374

## Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

H = high Level, L = Low Level  
 X = don't Care  
 ↑ = transition from low-to-high  
 Z = high impedance state  
 Q<sub>0</sub> = the level of the output before steady state input conditions were established

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## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 35$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 70$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ ) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. ( $T_L$ ) (Soldering 10 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

## DC Electrical Characteristics

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$		$T_A = -55$ to $125^\circ C$		Units
				Typ	Guaranteed Limits					
$V_{IH}$	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	1.5	V	
			4.5V		3.15	3.15	3.15	V		
			6.0V		4.2	4.2	4.2	V		
$V_{IL}$	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	0.5	V	
			4.5V		1.35	1.35	1.35	V		
			6.0V		1.8	1.8	1.8	V		
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V		
			4.5V	4.5	4.4	4.4	4.4	V		
			6.0V	6.0	5.9	5.9	5.9	V		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 6.0$ mA $ I_{OUT}  \leq 7.8$ mA	4.5V	4.2	3.98	3.84	3.7	V		
			6.0V	5.7	5.48	5.34	5.2	V		
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V		
			4.5V	0	0.1	0.1	0.1	V		
			6.0V	0	0.1	0.1	0.1	V		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 6.0$ mA $ I_{OUT}  \leq 7.8$ mA	4.5V	0.2	0.26	0.33	0.4	V		
			6.0V	0.2	0.26	0.33	0.4	V		
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$		
$I_{OZ}$	Maximum TRI-STATE Output Leakage Current	$V_{IN} = V_{IH}, OC = V_{IH}$ $V_{OUT} = V_{CC}$ or GND	6.0V		$\pm 0.5$	$\pm 5$	$\pm 10$	$\mu A$		
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	$\mu A$		

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of 5V  $\pm 10\%$  the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\* $V_{IL}$  limits are currently tested at 20% of  $V_{CC}$ . The above  $V_{IL}$  specification (30% of  $V_{CC}$ ) will be implemented no later than Q1, CY'89.

### AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, t_r=t_f=6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency		50	35	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Clock to Q	$C_L = 45\text{ pF}$	20	32	ns
$t_{PZH}, t_{PZL}$	Maximum Output Enable Time	$R_L = k\Omega$ $C_L = 45\text{ pF}$	19	28	ns
$t_{PHZ}, t_{PLZ}$	Maximum Output Disable Time	$R_L = k\Omega$ $C_L = 5\text{ pF}$	17	25	ns
$t_S$	Minimum Setup Time			20	ns
$t_H$	Minimum Hold Time			5	ns
$t_W$	Minimum Pulse Width		9	16	ns

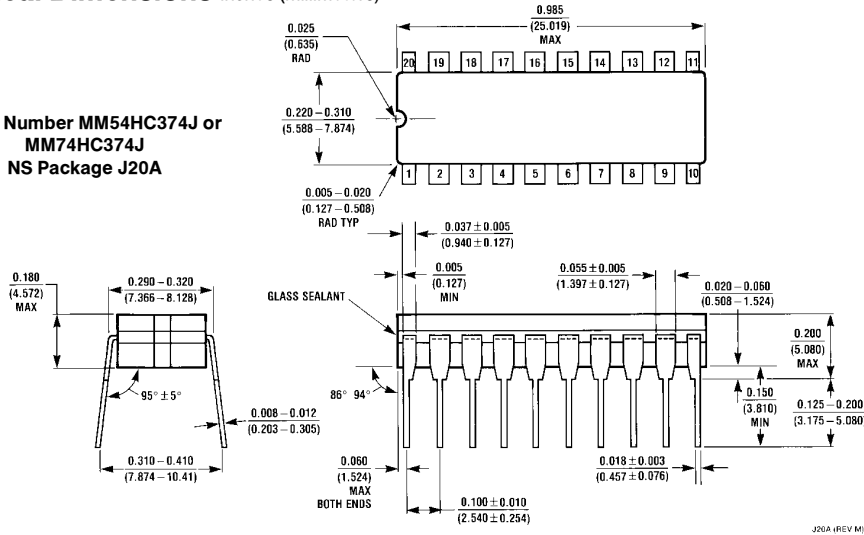
### AC Electrical Characteristics $V_{CC}=2.0-6.0V, C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^{\circ}C$			Units	
				Guaranteed Limits				
				$T_A = -40\text{ to }85^{\circ}C$	$T_A = -55\text{ to }125^{\circ}C$			
$f_{MAX}$	Maximum Operating Frequency	$C_L = 50\text{ pF}$	2.0V 4.5V 6.0V	6 30 35	5 24 28	4 20 23	MHz MHz MHz	
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clock to Q	$C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$	2.0V 2.0V	68 110	180 230	225 288	270 345	ns ns
		$C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$	4.5V 4.5V	22 30	36 46	45 57	48 69	ns ns
		$C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$	6.0V 6.0V	20 28	31 40	39 50	46 60	ns ns
$t_{PZH}, t_{PZL}$	Maximum Output Enable Time	$R_L = 1\text{ k}\Omega$						
		$C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$	2.0V 2.0V	50 80	150 200	189 250	225 300	ns ns
		$C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$	4.5V 4.5V	21 30	30 40	37 50	45 60	ns ns
		$C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$	6.0V 6.0V	19 26	26 35	31 44	39 53	ns ns
$t_{PHZ}, t_{PLZ}$	Maximum Output Disable Time	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$	2.0V 4.5V 6.0V	50 21 19	150 30 26	189 37 31	225 45 39	ns ns ns
$t_S$	Minimum Setup Time		2.0V 4.5V 6.0V	50 9 9	60 13 11	75 15 13	ns ns ns	
$t_H$	Minimum Hold Time		2.0V 4.5V 6.0V	5 5 5	30 5 5	5 5 5	ns ns ns	
$t_W$	Minimum Pulse Width		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 20	ns ns ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time	$C_L = 50\text{ pF}$	2.0V 4.5V 6.0V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
$t_r, t_f$	Maximum Input Rise and Fall Time, Clock		2.0V 4.5V 6.0V	1000 500 400	1000 500 400	1000 500 400	ns ns ns	
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per flip-flop) $OC = V_{CC}$ $OC = GND$		30 50				pF pF
$C_{IN}$	Maximum Input Capacitance			5 10	10	10	10	pF

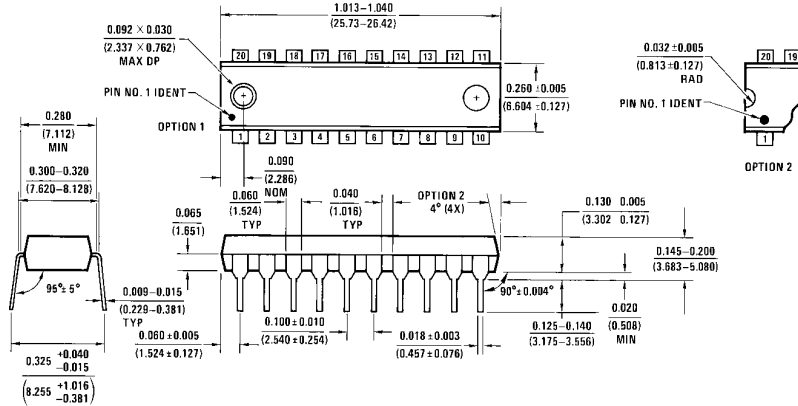
**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters)

Order Number **MM54HC374J** or  
**MM74HC374J**  
NS Package **J20A**



J20A (REV M)



N20A (REV G)

Order Number **MM74HC374N**  
NS Package **N20A**

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**National Semiconductor Corporation**  
1111 West Bardin Road  
Arlington, TX 76017  
Tel: (800) 272-9959  
Fax: (800) 737-7018

**National Semiconductor Europe**  
Fax: (+49) 0-180-530 85 86  
Email: cnjwge@tevm2.nsc.com  
Deutsch Tel: (+49) 0-180-530 85 85  
English Tel: (+49) 0-180-532 78 32  
Français Tel: (+49) 0-180-532 93 58  
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
19th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
Tel: 81-043-299-2309  
Fax: 81-043-299-2408

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