

Advance Information

Integrated Relay/Solenoid Driver

- Optimized to Switch 3 V to 5 V Relays from a 5 V Rail
- Compatible with "TX" and "TQ" Series Telecom Relays Rated up to 300 mW at 3 V to 5 V
- Features Low Input Drive Current
- Internal Zener Clamp Routes Induced Current to Ground Rather Than Back to Supply
- Guaranteed Off State with No Input Connection
- Supports Large Systems with Minimal Off-State Leakage
- ESD Resistant in Accordance with the 2000 V Human Body Model
- Provides a Robust Driver Interface Between Relay Coil and Sensitive Logic Circuits

Applications include:

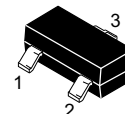
- Telecom Line Cards and Telephony
- Industrial Controls
- Security Systems
- Appliances and White Goods
- Automated Test Equipment
- Automotive Controls

This device is intended to replace an array of three to six discrete components with an integrated SMT part. It is available in a SOT-23 package. It can be used to switch other 3 to 5 Vdc Inductive Loads such as solenoids and small DC motors.

MDC3105LT1

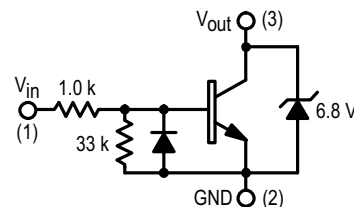
Motorola Preferred Device

RELAY/SOLENOID DRIVER
SILICON MONOLITHIC
CIRCUIT BLOCK



CASE 318-08, STYLE 6
SOT-23 (TO-236AB)

INTERNAL CIRCUIT DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6.0	Vdc
Recommended Operating Supply Voltage	V_{CC}	2.0-5.5	Vdc
Input Voltage	$V_{in(fwd)}$	6.0	Vdc
Reverse Input Voltage	$V_{in(rev)}$	-0.5	Vdc
Output Sink Current — Continuous	I_O	300	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation ⁽¹⁾ Derate above 25°C	P_D	225	mW
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	556	°C/W

1. FR-5 PCB of 1" x 0.75" x 0.062", $T_A = 25^\circ\text{C}$

Thermal Clad is a trademark of the Bergquist Company.

Preferred devices are Motorola recommended choices for future use and best overall value.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MDC3105LT1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Output Zener Breakdown Voltage (@ I _T = 10 mA Pulse)	V _(BRout) V _(-BRout)	6.4 —	6.8 -0.7	7.2 —	V
Output Leakage Current @ 0 Input Voltage (V _{out} = 5.5 Vdc, V _{in} = O.C., T _A = 25°C) (V _{out} = 5.5 Vdc, V _{in} = O.C., T _A = 85°C)	I _{OO}	— —	— —	5.0 30	μA

ON CHARACTERISTICS

Input Bias Current @ V _{in} = 4.0 Vdc (I _O = 250 mA, V _{out} = 0.4 Vdc, T _A = -40°C) (correlated to a measurement @ 25°C)	I _{in}	—	2.5	—	mAdc
Output Saturation Voltage (I _O = 250 mA, V _{in} = 4.0 Vdc, T _A = -40°C) (correlated to a measurement @ 25°C)		—	0.2	0.4	Vdc
Output Sink Current— Continuous (T _A = -40°C, V _{CE} = 0.4 Vdc, V _{in} = 4.0 Vdc) (correlated to a measurement @ 25°C)	I _{C(on)}	250	—	—	mA

TYPICAL APPLICATION-DEPENDENT SWITCHING PERFORMANCE

SWITCHING CHARACTERISTICS

Characteristic	Symbol	V _{CC}	Min	Typ	Max	Units
Propagation Delay Times: High to Low Propagation Delay; Figures 1, 2 (5.0 V 74HC04) Low to High Propagation Delay; Figures 1, 2 (5.0 V 74HC04)	t _{PHL} t _{PLH}	5.5	— —	55 430	— —	ns
High to Low Propagation Delay; Figures 1, 3 (3.0 V 74HC04) Low to High Propagation Delay; Figures 1, 3 (3.0 V 74HC04)	t _{PHL} t _{PLH}	5.5	— —	85 315	— —	
High to Low Propagation Delay; Figures 1, 4 (5.0 V 74LS04) Low to High Propagation Delay; Figures 1, 4 (5.0 V 74LS04)	t _{PHL} t _{PLH}	5.5	— —	55 2385	— —	
Transition Times: Fall Time; Figures 1, 2 (5.0 V 74HC04) Rise Time; Figures 1, 2 (5.0 V 74HC04)	t _f t _r	5.5	— —	45 160	— —	ns
Fall Time; Figures 1, 3 (3.0 V 74HC04) Rise Time; Figures 1, 3 (3.0 V 74HC04)	t _f t _r	5.5	— —	70 195	— —	
Fall Time; Figures 1, 4 (5.0 V 74LS04) Rise Time; Figures 1, 4 (5.0 V 74LS04)	t _f t _r	5.5	— —	45 2400	— —	
Input Slew Rate ⁽¹⁾	ΔV/Δt in	5.5	TBD	—	—	V/ms

1. Minimum input slew rate must be followed to avoid overdissipating the device.

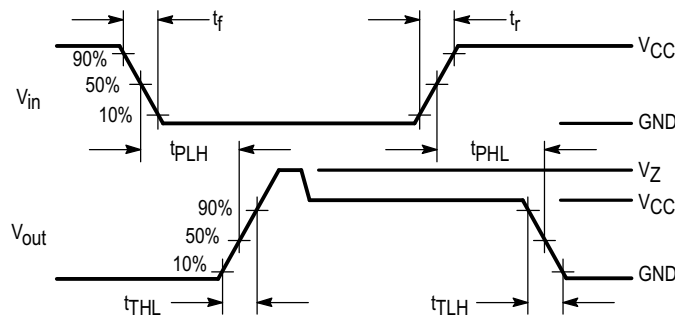


Figure 1. Switching Waveforms

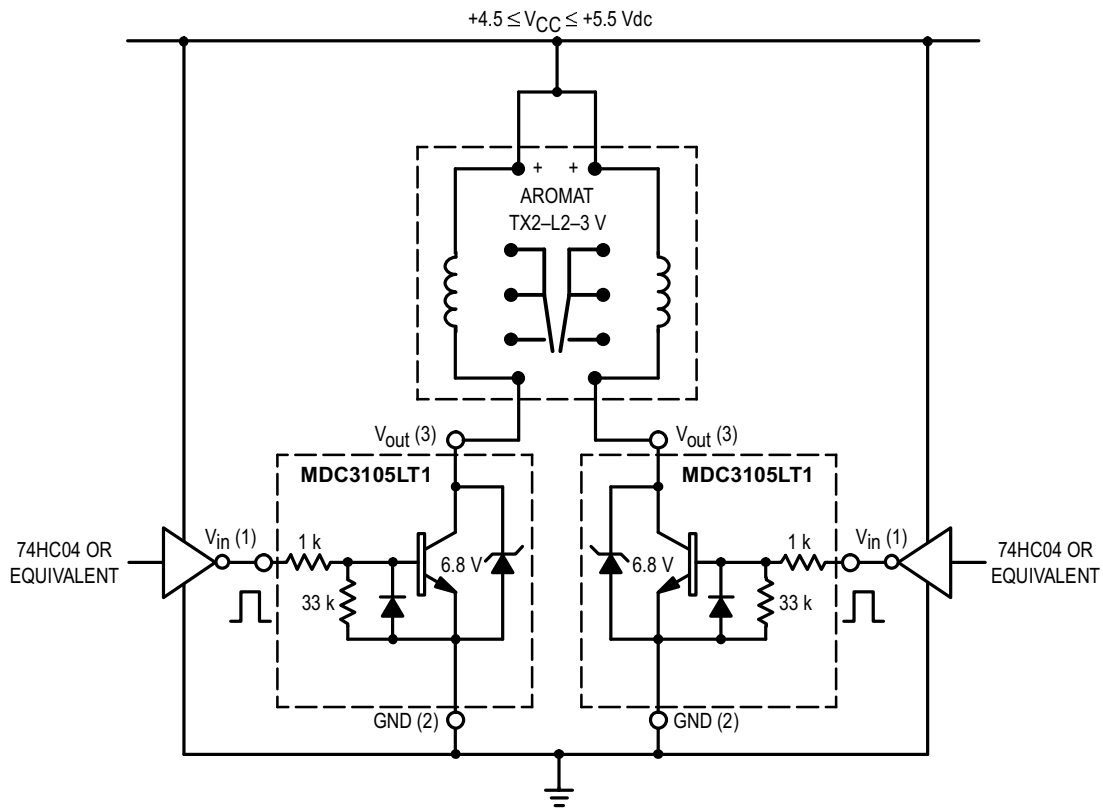


Figure 2. A 3.0-V, 200-mW Dual Coil Latching Relay Application with 5.0 V-HCMOS Interface

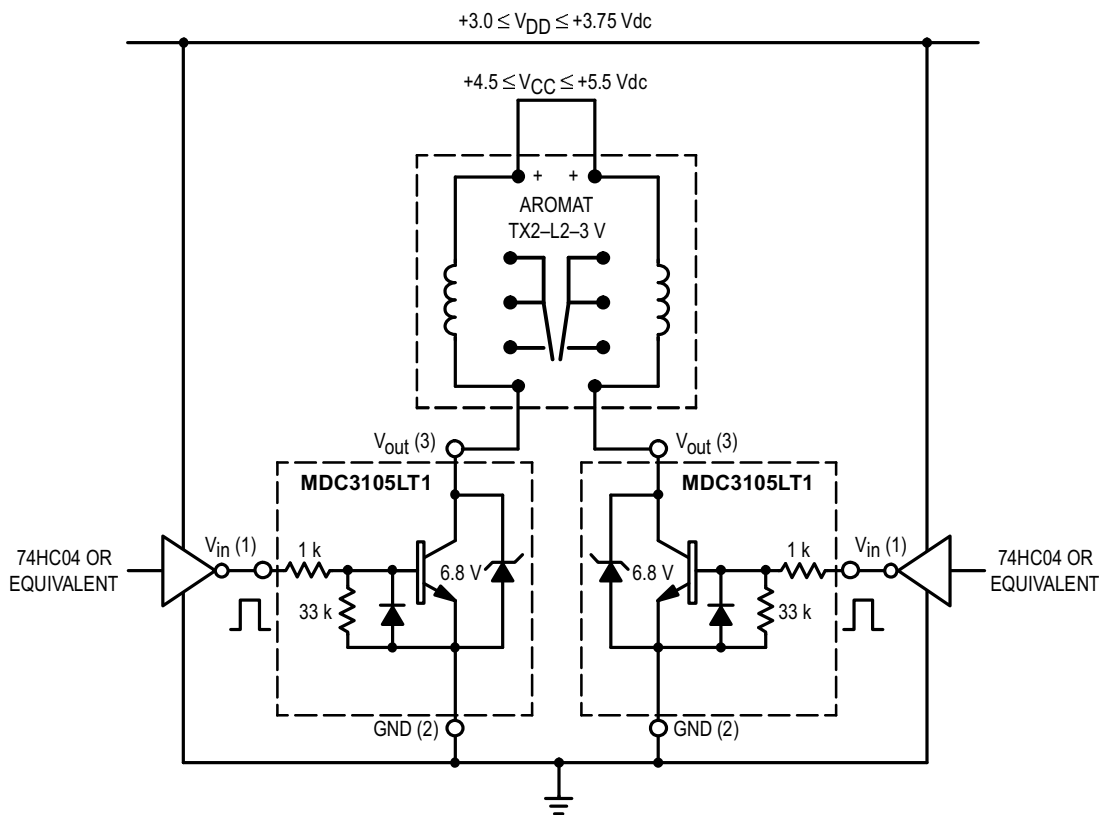


Figure 3. A 3.0-V, 200-mW Dual Coil Latching Relay Application with 3.0 V-HCMOS Interface

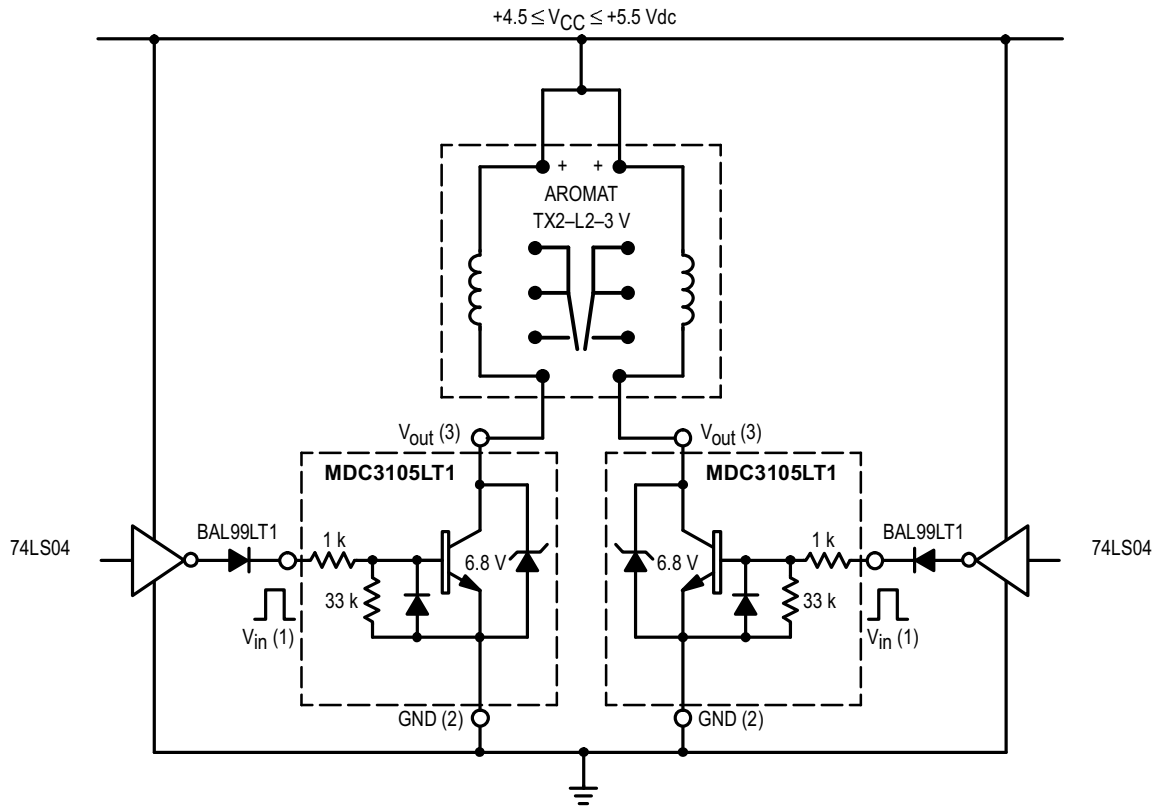


Figure 4. A 3.0-V, 200-mW Dual Coil Latching Relay Application with TTL Interface

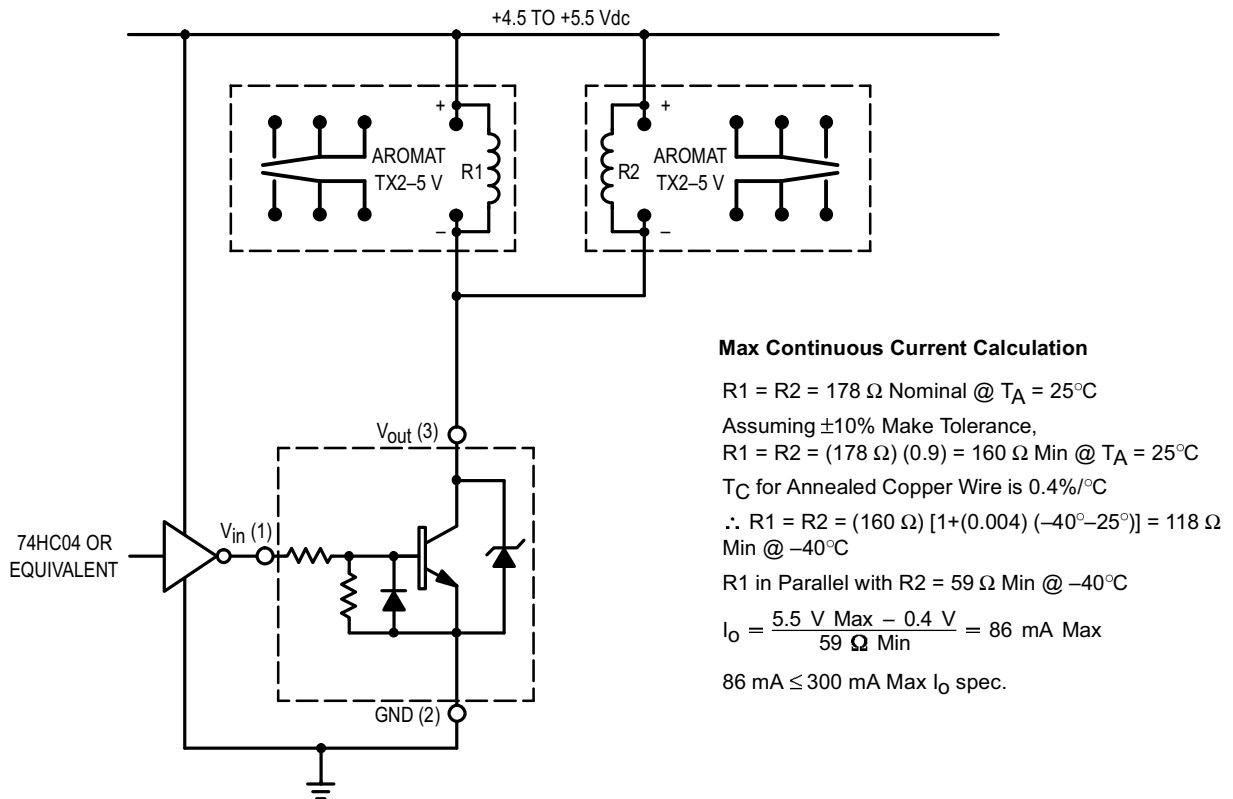


Figure 5. Typical 5.0 V, 140 mW Coil Dual Relay Application

TYPICAL OPERATING WAVEFORMS

(Circuit of Figure 5)

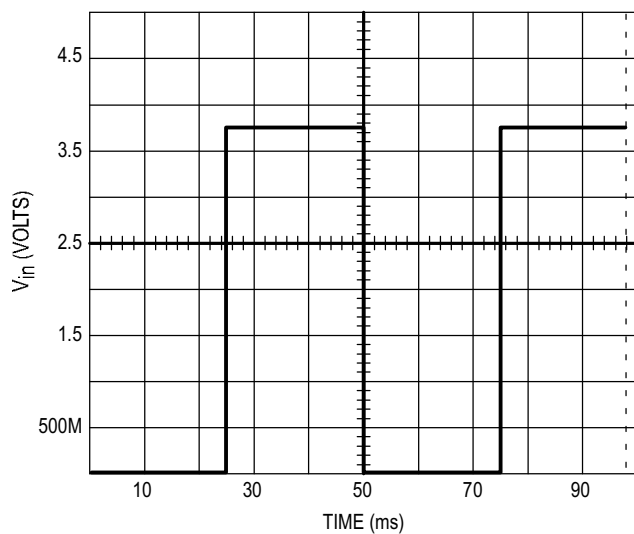


Figure 6. 20 Hz Square Wave Input

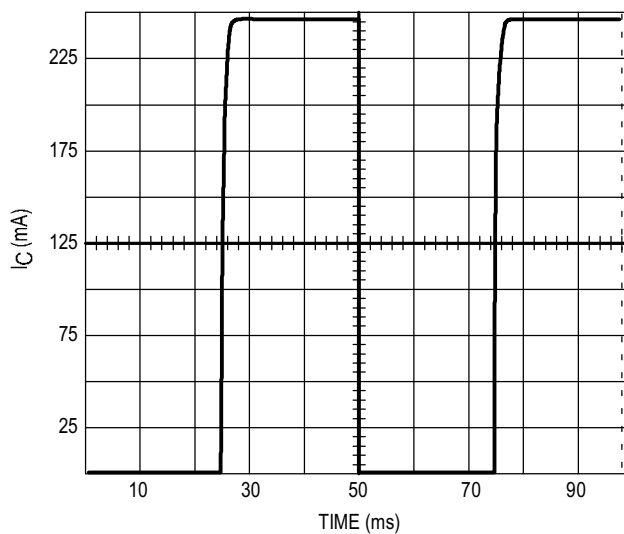


Figure 7. 20 Hz Square Wave Response

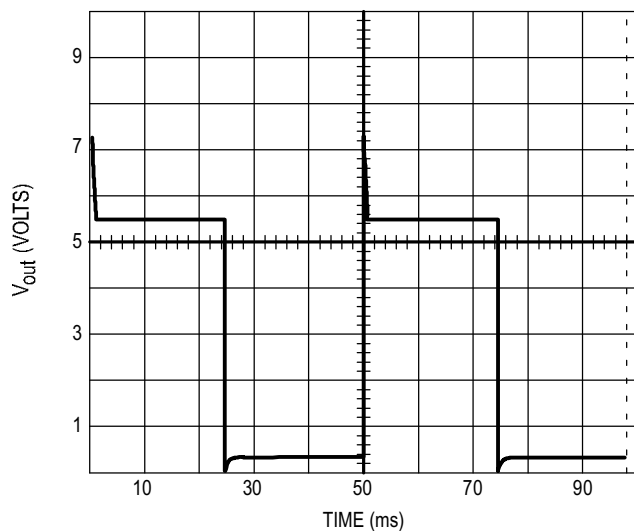


Figure 8. 20 Hz Square Wave Response

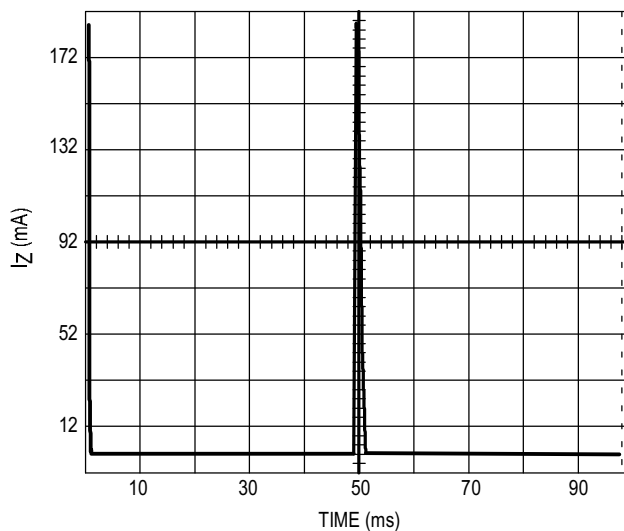


Figure 9. 20 Hz Square Wave Response

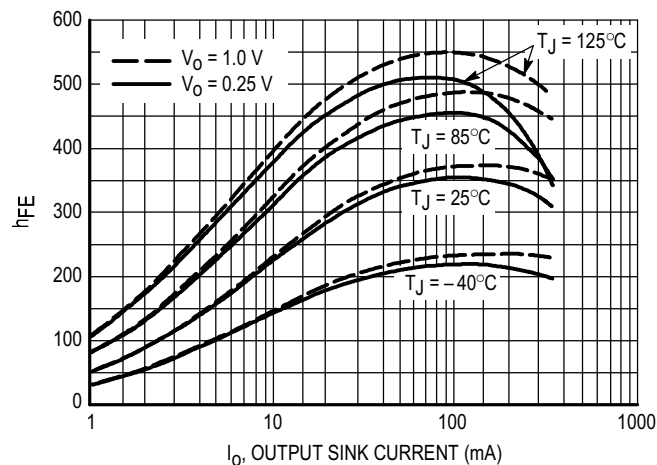


Figure 10. Pulsed Current Gain

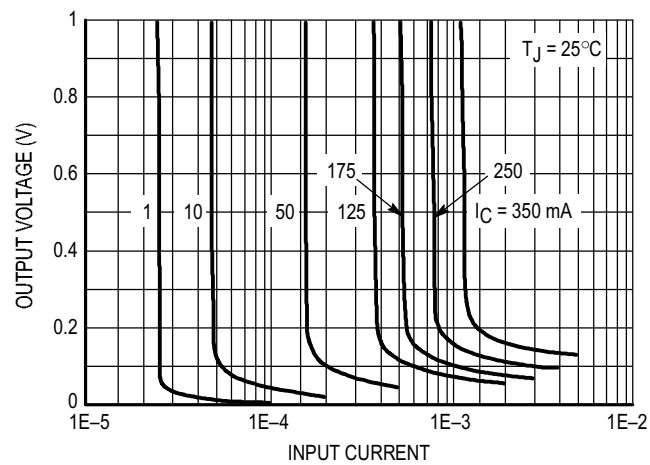


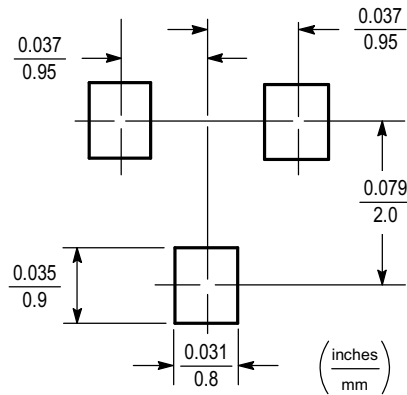
Figure 11. Collector Saturation Region

INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-23

SOT-23 POWER DISSIPATION

The power dissipation of the SOT-23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet for the SOT-23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{556^\circ\text{C/W}} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT-23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

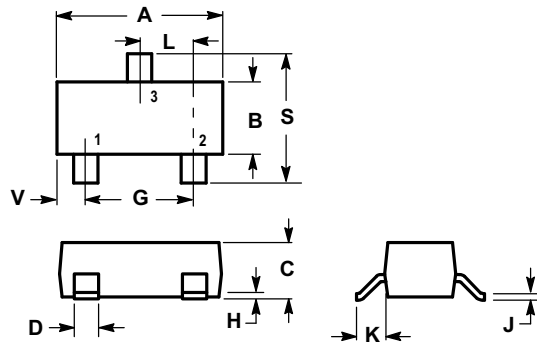
SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

- STYLE 6:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR

CASE 318-08
 ISSUE AE

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