# MCM93422,A
# MCM93L422,A

## TTL

### 256 × 4-BIT RANDOM ACCESS MEMORY

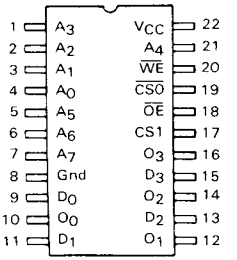
### 1024-BIT RANDOM ACCESS MEMORY

The MCM93422 Series are 1024-bit Read/Write RAMs, organized 256 words by 4 bits, designed for high performance main memory and control storage applications.

They have full decoding on-chip, separate data input and data output lines, an active low-output enable, write enable, and two chip selects, one active high, one active low. These memories are fully compatible with standard TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Outputs
- Noninverting Data Outputs
- Power Dissipation — 0.26 mW/Bit Typical
- Standard 22-Pin, 400 Mil Wide Package
- Power Dissipation Decreases with Increasing Temperature
- Organized 256 Words × 4 Bits
- Two Chip Select Lines for Memory Expansion
- Address Access Time: MCM93422A — 35 ns Max
  MCM93422 — 45 ns Max
  MCM93L422A — 45 ns Max
  MCM93L422 — 60 ns Max

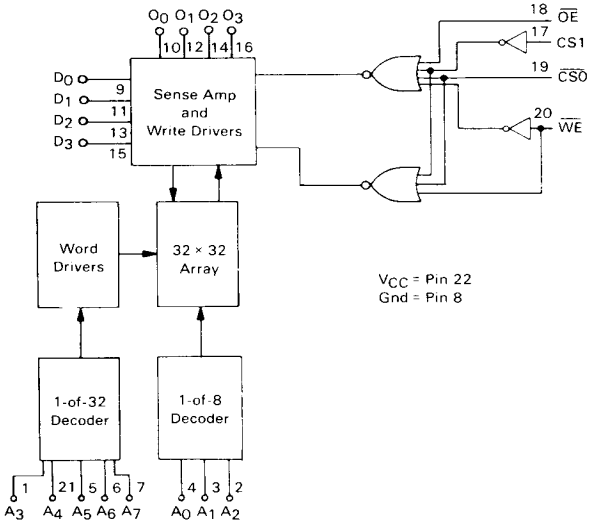
**PIN ASSIGNMENT**




**Pin Description**

| | |
|---|---|
| $\overline{CS0}$, CS1 | Chip Selects |
| $A_0$–$A_7$ | Address Inputs |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $D_0$–$D_3$ | Data Inputs |
| $O_0$–$O_3$ | Data Outputs |

**BLOCK DIAGRAM**




VCC = Pin 22
Gnd = Pin 8

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## FUNCTIONAL DESCRIPTION

The MCM93422 Series are fully decoded 1024-bit random access memories organized 256 words by 4 bits. Word selections are achieved by means of an 8-bit address, $A_0$-$A_7$.

The Chip Select (CS0 and CS1) inputs provide for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable (WE, Pin 20). With WE and CS0 held low and the CS1 held high, the data at $D_n$ is written into the addressed location. To read, WE and CS1 are held high and CS0 is held low. Data in the specified location is presented at the output ($O_0$-$O_2$) and is noninverted.

The three-state outputs provide drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus-organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in a high-impedance state.

### GUARANTEED OPERATING RANGES

| Part Number | Supply Voltage ($V_{CC}$) | | | Ambient Temp. ($T_A$) |
|---|---|---|---|---|
| | Min | Nom | Max | |
| MCM93422DC, PC<br>MCM93L422DC, PC<br>MCM93422ADC, APC<br>MCM93L422ADC, APC | 4.75 V | 5.0 V | 5.25 V | 0°C to +75°C |

### ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Storage Temperature<br>Ceramic Package (D Suffix)<br>Plastic Package (P Suffix) | <br>-65°C to +150°C<br>-55°C to +125°C |
| Operating Junction Temperature, $T_J$<br>Ceramic Package (D Suffix)<br>Plastic Package (P Suffix) | <br>≤165°C<br>≤125°C |
| $V_{CC}$ Pin Potential to Ground Pin | -0.5 V to +7.0 V |
| Input Voltage (dc) | -0.5 V to +5.5 V |
| Voltage Applied to Outputs (Output High) | -0.5 V to +5.5 V |
| Output Current (dc) (Output Low) | +20 mA |
| Input Current (dc) | -12 mA to +5.0 mA |

*Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded

### TRUTH TABLE

| Inputs | | | | | Output | Mode |
|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CS0}$ | CS1 | $\overline{WE}$ | $D_0$-$D_3$ | $O_0$-$O_3$ | |
| X | H | X | X | X | High Z | Not Selected |
| X | X | L | X | X | High Z | Not Selected |
| X | L | H | L | L | High Z | Write "0" |
| X | L | H | L | H | High Z | Write "1" |
| H | X | X | X | X | High Z | Output Disabled |
| L | L | H | H | X | $O_0$-$O_3$ | Read |

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

### DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range)

| Symbol | Characteristic | | Limits Min | Limits Max | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Voltage | | — | 0.45 | Vdc | $V_{CC}$ = Min, $I_{OL}$ = 8.0 mA | |
| $V_{IH}$ | Input High Voltage | | 2.1 | — | Vdc | Guaranteed Input High Voltage for All Inputs | |
| $V_{IL}$ | Input Low Voltage | | — | 0.8 | Vdc | Guaranteed Input Low Voltage for All Inputs | |
| $I_{IL}$ | Input Low Current | | — | -300 | μAdc | $V_{CC}$ = Max, $V_{in}$ = 0.4 V | |
| $I_{IH}$ | Input High Current | | —<br>— | 40<br>1.0 | μAdc<br>mAdc | $V_{CC}$ = Max, $V_{in}$ = 4.5 V<br>$V_{CC}$ = Max, $V_{in}$ = 5.25 V | |
| $I_{off}$ | Output Current (High Z) | | | 50<br>-50 | μAdc | $V_{CC}$ = Max, $V_{out}$ = 2.4 V<br>$V_{CC}$ = Max, $V_{out}$ = 0.5 V | |
| $I_{OS}$ | Output Current Short Circuit to Ground | | — | -70 | mAdc | $V_{CC}$ = Max (Note 1) | |
| $V_{OH}$ | Output High Voltage | | 2.4 | — | Vdc | $V_{CC}$ = Min, $I_{OH}$ = -5.2 mA | |
| $V_{IK}$ | Input Diode Clamp Voltage | | — | -1.5 | Vdc | $V_{CC}$ = Max, $I_{in}$ = -10 mA | |
| $I_{CC}$ | Power Supply Current | MCM93422/ MCM93422A | — | 130 | mAdc | $T_A$ = Max | $V_{CC}$ = Max, All Inputs Grounded |
| | | | — | 155 | mAdc | $T_A$ = Min | |
| | | MCM93L422/ MCM93L422A | — | 75 | mAdc | $T_A$ = Max | |
| | | | — | 80 | mAdc | $T_A$ = Min | |

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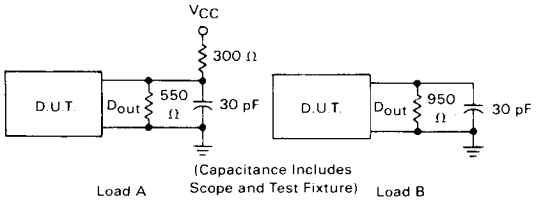
## AC OPERATING CONDITIONS AND CHARACTERISTICS

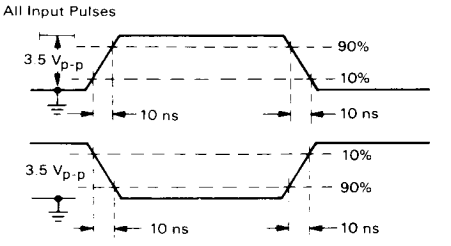
(Full operating voltage and temperature range)

### AC TEST LOAD AND WAVEFORMS

**Loading Conditions**



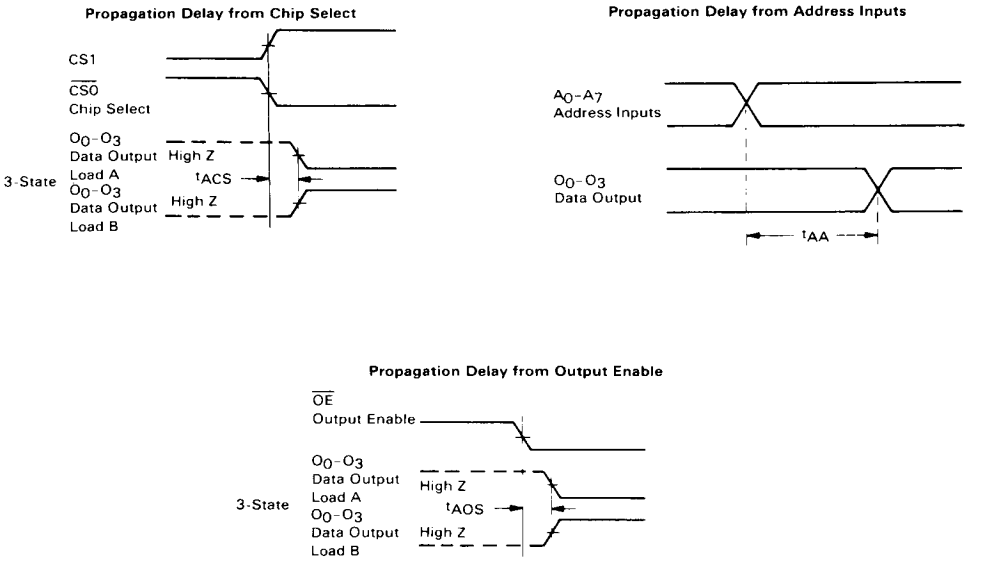

**Input Pulses**



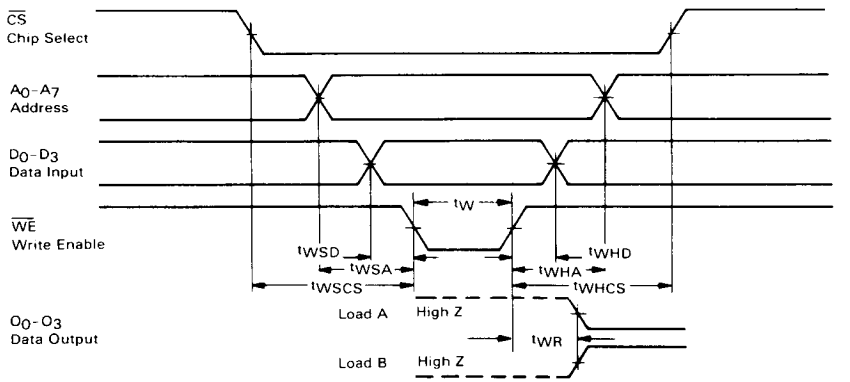

| Symbol | Characteristic (Notes 1, 2, 3, 4, 5) | MCM93422ADC MCM93422APC | | MCM93422DC MCM93422PC | | MCM93L422ADC MCM93L422APC | | MCM93L422DC MCM93L422PC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| READ MODE | DELAY TIMES | | | | | | | | | ns |
| $t_{ACS}$ | Chip Select Time | — | 30 | — | 30 | — | 30 | — | 35 | |
| $t_{ZRCS}$ | Chip Select to High Z | — | 30 | — | 30 | — | 30 | — | 35 | |
| $t_{AOS}$ | Output Enable Time | — | 30 | — | 30 | — | 30 | — | 35 | |
| $T_{ZROS}$ | Output Enable to High Z | — | 30 | — | 30 | — | 30 | — | 35 | |
| $t_{AA}$ | Address Access Time | — | 35 | — | 45 | — | 45 | — | 60 | |
| WRITE MODE | DELAY TIMES | | | | | | | | | ns |
| $t_{ZWS}$ | Write Disable to High Z | — | 35 | — | 35 | — | 35 | — | 40 | |
| $t_{WR}$ | Write Recovery Time | — | 35 | — | 40 | — | 40 | — | 45 | |
| | INPUT TIMING REQUIREMENTS | | | | | | | | | ns |
| $t_W$ | Write Pulse Width (to guarantee write) | 25 | — | 30 | — | 30 | — | 45 | — | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5.0 | — | 5.0 | — | 5.0 | — | 5.0 | — | |
| $t_{WHD}$ | Data Hold Time After Write | 5.0 | — | 5.0 | — | 5.0 | — | 5.0 | — | |
| $t_{WSA}$ | Address Setup Time (at $t_W$ = Min) | 5.0 | — | 10 | — | 10 | — | 10 | — | |
| $t_{WHA}$ | Address Hold Time | 5.0 | — | 5.0 | — | 5.0 | — | 5.0 | — | |
| $t_{WSCS}$ | Chip Select Setup Time | 5.0 | — | 5.0 | — | 5.0 | — | 5.0 | — | |
| $t_{WHCS}$ | Chip Select Hold Time | 5.0 | — | 5.0 | — | 5.0 | — | 5.0 | — | |

NOTES:
1. Output short circuit conditions must not exceed 1.0 second duration.
2. The maximum address access time is guaranteed to be the worst-case bit in the memory.
3. Load A used to measure transitions between logic levels and from High Z state to logic Low state.
   Load B used to measure transitions between High Z state to logic High state.
   Load C used to measure transistions from either logic High or Low state to High Z state.
4. All time measurements are referenced to +1.5 Vdc except transitions into the High Z state where outputs are referenced to a delta of 0.5 Vdc from the logic level using Load C.
5. See test circuit and waveforms.

### READ OPERATION TIMING DIAGRAM
(All Time Measurements Referenced to 1.5 V)




### WRITE CYCLE TIMING




(All above measurements reference to 1.5 V)

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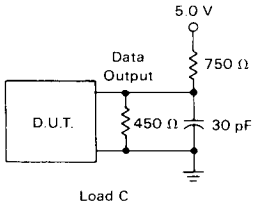
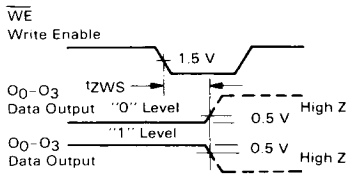
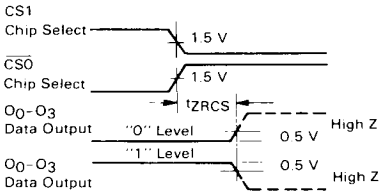
**WRITE ENABLE TO HIGH Z DELAY**

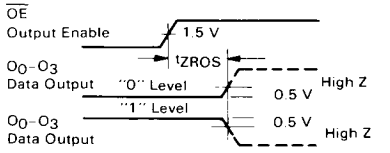



**Propagation Delay from Chip Select to High Z**




**Propagation Delay from Output Enable to High Z**




(All $t_{ZXX}$ parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

| Package | $\theta_{JA}$ (Junction to Ambient) | | $\theta_{JC}$ (Junction to Case) |
|---|---|---|---|
| | Blown* | Still | |
| D Suffix | 50°C/W | 75°C/W | 15°C/W |
| P Suffix | 50°C/W | 60°C/W | 15°C/W |

*500 linear ft. per minute blown air.

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