MOTOROLA

MC54/74F175

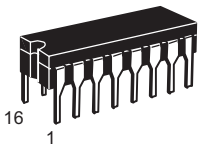
QUAD D FLIP-FLOP

The MC54/74F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where both true and complementary outputs are required and clock and clear inputs are common to all flip-flops. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs when LOW.

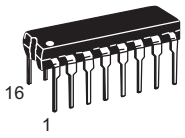
- Four Edge-triggered D-type Inputs
- Buffered Positive Edge-triggered Common Clock
- Buffered Asynchronous Common Reset
- True and Complementary Outputs
- ESD > 4000 Volts

QUAD D FLIP-FLOP

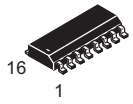
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09

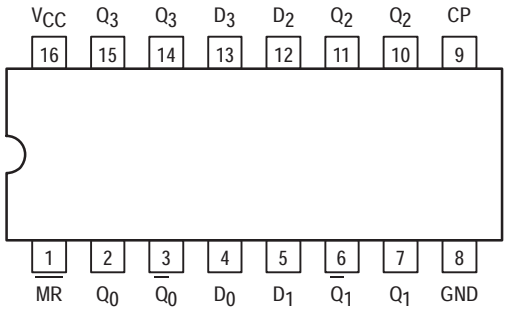


N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

CONNECTION DIAGRAM DIP (TOP VIEW)



FUNCTION TABLE

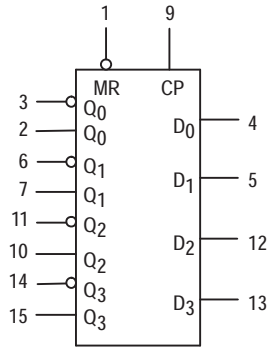
Inputs	Outputs	
@ t_n, $\overline{MR}$ = H	@ t_n + 1	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

t_n = Bit time before clock positive-going transition
t_n + 1 = Bit time after clock positive-going transition
H = HIGH Voltage Level
L = LOW Voltage Level

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

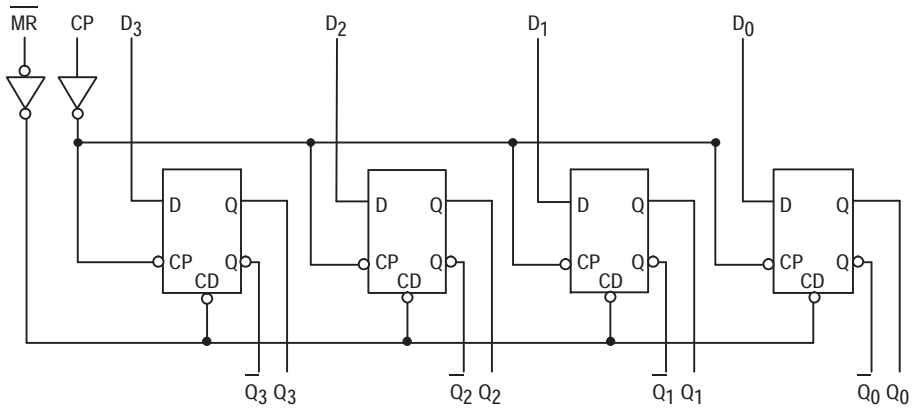
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

MC54/74F175

LOGIC DIAGRAM



NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The F175 consists of four edge-triggered D flop-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs, one setup time before, on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and Q outputs HIGH independent of Clock or Data inputs. The F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	–55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			–1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	I_{IN} = –18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = – 1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = – 1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	µA	V_{IN} = 7.0 V	V_{CC} = MAX
I_{IL}	Input LOW Current				–0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			22.5	34	mA	D_n = $\overline{MR}$ = 4.5 V, CP = ⎍	V_{CC} = MAX

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			54F T_A = –55°C to +125°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF		74F T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF		Unit
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	140		100		100		MHz
t_{PLH}	Propagation Delay	3.5	5.0	6.5	3.5	8.5	3.5	7.5	ns
t_{PHL}	CP to Q_n or $\overline{Q}_n$	4.0	6.5	8.5	4.0	10.5	4.0	9.5	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	9.0	11.5	4.5	15	4.5	13	ns
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	4.0	6.5	8.5	4.0	10	4.0	9.0	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A = –55°C to +125°C, V_{CC} = 5.0 V ± 10%		74F T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 10%		Unit
		Min	Typ	Max	Min	Max	Min	Max	
t_s(H)	Setup Time, HIGH or LOW	3.0			3.0		3.0		
t_s(L)	D_n to CP	3.0			3.0		3.0		ns
t_h(H)	Hold Time, HIGH or LOW	1.0			1.0		1.0		
t_h(L)	D_n to CP	1.0			1.0		1.0		
t_w(H)	CP Pulse Width, HIGH	4.0			4.0		4.0		ns
t_w(L)	or LOW	5.0			5.0		5.0		
t_w(L)	$\overline{MR}$ Pulse Width, LOW	5.0			5.0		5.0		ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0			5.0		5.0		ns

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