MC14555B, MC14556B

Dual Binary to 1-of-4 Decoder/Demultiplexer

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary–to–hexadecimal (1–of–16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

MARKING DIAGRAMS

PDIP–16
P SUFFIX
CASE 648

MC1455xBCP
AWLYYWW

SOIC–16
D SUFFIX
CASE 751B

1455xB
AWLYWW

SOEIAJ–16
F SUFFIX
CASE 966

MC1455xB
ALYW

x	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14555BCP	PDIP–16	2000/Box
MC14555BD	SOIC–16	48/Rail
MC14555BDR2	SOIC–16	2500/Tape & Reel
MC14555BF	SOEIAJ–16	See Note 1.
MC14555BFEL	SOEIAJ–16	See Note 1.
MC14556BCP	PDIP–16	2000/Box
MC14556BD	SOIC–16	48/Rail
MC14556BDR2	SOIC–16	2500/Tape & Reel
MC14556BF	SOEIAJ–16	See Note 1.
MC14556BFEL	SOEIAJ–16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
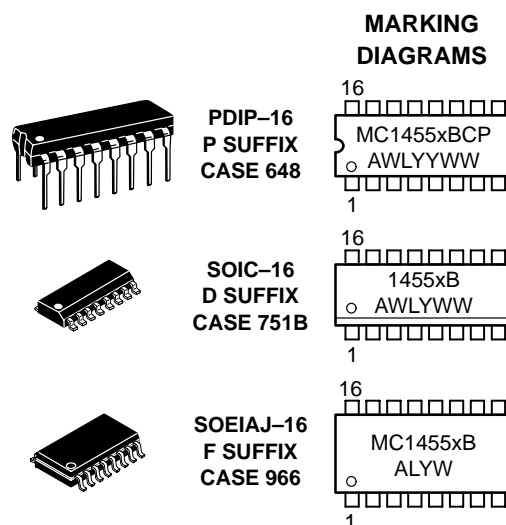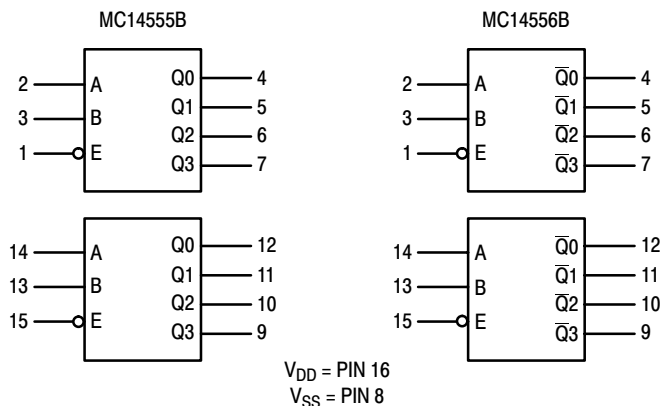   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14555B, MC14556B

PIN ASSIGNMENTS

MC14555B

$\overline{E}_A$	1 ●	16	V_{DD}
A_A	2	15	$\overline{E}_B$
B_A	3	14	A_B
$Q0_A$	4	13	B_B
$Q1_A$	5	12	$Q0_B$
$Q2_A$	6	11	$Q1_B$
$Q3_A$	7	10	$Q2_B$
V_{SS}	8	9	$Q3_B$

MC14556B

$\overline{E}_A$	1 ●	16	V_{DD}
A_A	2	15	$\overline{E}_B$
B_A	3	14	A_B
$\overline{Q0}_A$	4	13	B_B
$\overline{Q1}_A$	5	12	$\overline{Q0}_B$
$\overline{Q2}_A$	6	11	$\overline{Q1}_B$
$\overline{Q3}_A$	7	10	$\overline{Q2}_B$
V_{SS}	8	9	$\overline{Q3}_B$
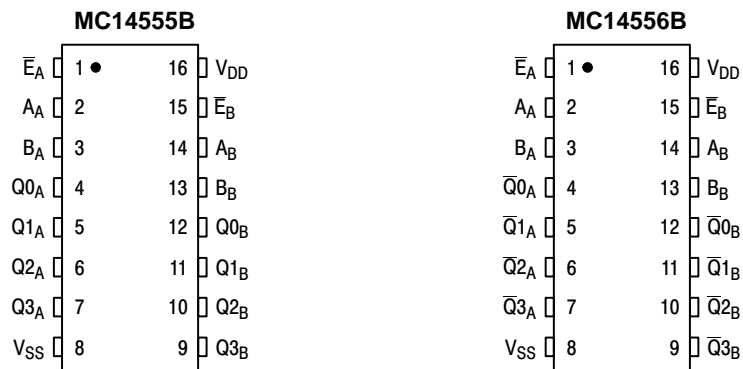
TRUTH TABLE

Inputs			Outputs							
Enable	Select		MC14555B				MC14556B			
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

BLOCK DIAGRAM

MC14555B

2 —	A	Q0	— 4
3 —	B	Q1	— 5
1 —o	E	Q2	— 6
		Q3	— 7

14 —	A	Q0	— 12
13 —	B	Q1	— 11
15 —o	E	Q2	— 10
		Q3	— 9

MC14556B

2 —	A	$\overline{Q0}$	— 4
3 —	B	$\overline{Q1}$	— 5
1 —o	E	$\overline{Q2}$	— 6
		$\overline{Q3}$	— 7

14 —	A	$\overline{Q0}$	— 12
13 —	B	$\overline{Q1}$	— 11
15 —o	E	$\overline{Q2}$	— 10
		$\overline{Q3}$	— 9

V_{DD} = PIN 16
V_{SS} = PIN 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ [4.]	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	− 3.0 − 0.64 − 1.6 − 4.2	— — — —	− 2.4 − 0.51 − 1.3 − 3.4	− 4.2 − 0.88 − 2.25 − 8.8	— — — —	− 1.7 − 0.36 − 0.9 − 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}		—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current [5.] [6.] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15			$I_T = (0.85\ \mu A/kHz)\ f + I_{DD}$ $I_T = (1.70\ \mu A/kHz)\ f + I_{DD}$ $I_T = (2.60\ \mu A/kHz)\ f + I_{DD}$					μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L − 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} − V_{SS})$ in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ [8.]	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay Time — A, B to Output t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 62 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 220 95 70	 440 190 140	ns
Propagation Delay Time — E to Output t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 200 85 65	 400 170 130	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
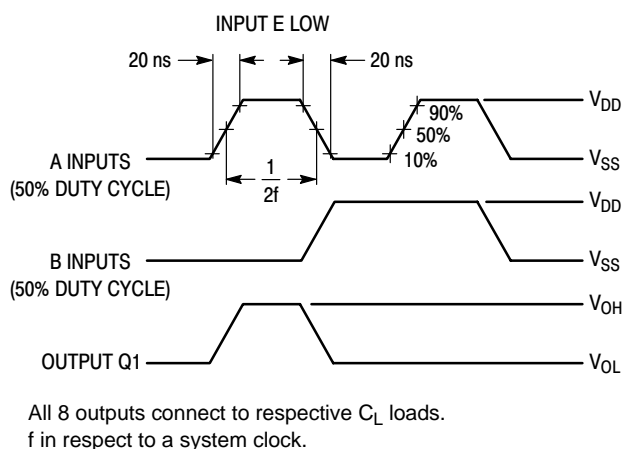
Figure 1. Dynamic Power Dissipation Signal Waveforms
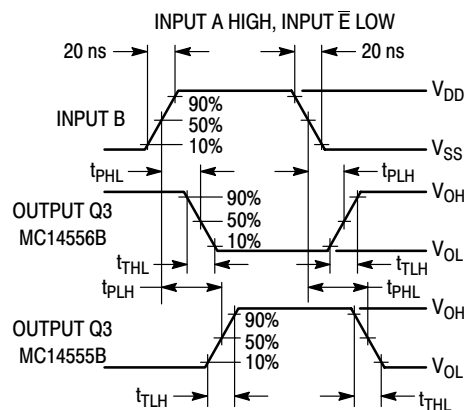
Figure 2. Dynamic Signal Waveforms

LOGIC DIAGRAM
(1/2 of Dual)
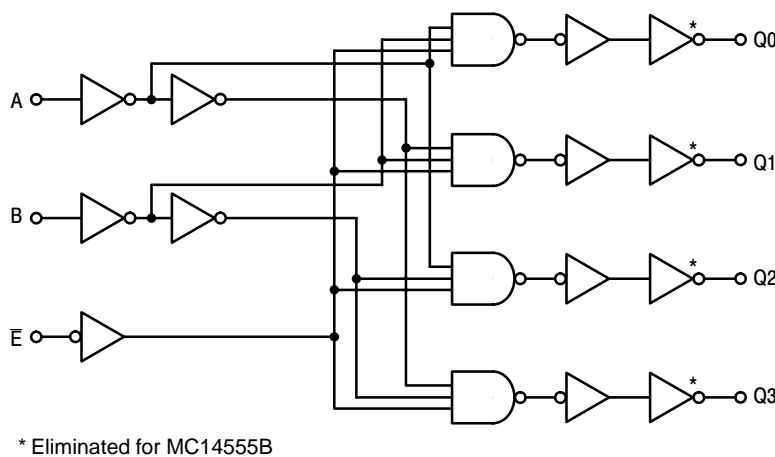
* Eliminated for MC14555B

PACKAGE DIMENSIONS

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R
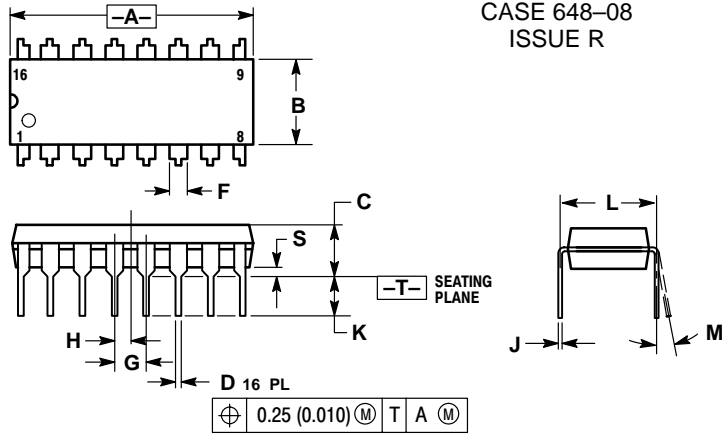
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

SOIC–16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J
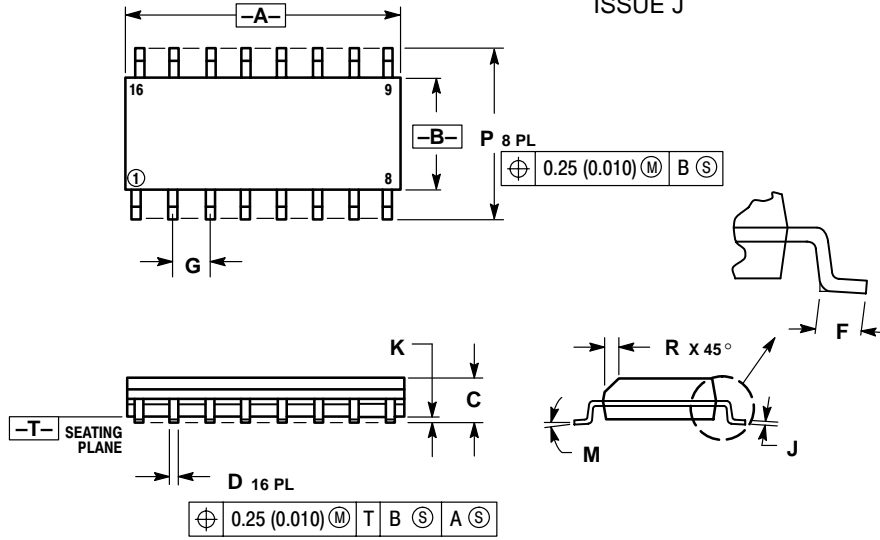
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

SOEIAJ–16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966–01
ISSUE O
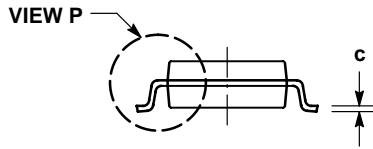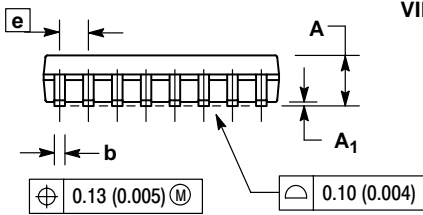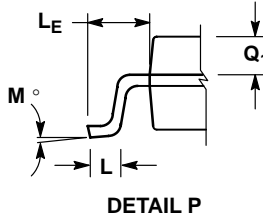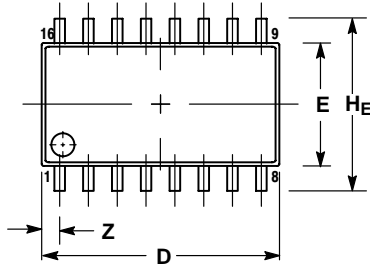
DETAIL P

VIEW P

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

$\bigoplus$ 0.13 (0.005) (M) $\triangle$ 0.10 (0.004)

MC14555B, MC14556B

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
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