

SECTION 6

Neuron CHIP ELECTRICAL AND MECHANICAL SPECIFICATIONS

6.1 INTRODUCTION

The Neuron Chip processor family consists of two device types: MC143150 and MC143120. Within these device types are different versions, each with its own electrical and mechanical specifications. The MC143150B1FU/B1FU1 and MC143120B1/E2DW operate up to 10 MHz over the full industrial temperature range of -40 to $+85^{\circ}\text{C}$, including writes to EEPROM down to -40°C . Memory interface timing is different for all MC143150xx devices. (See Sections 6.2.4 and 6.2.9) Refer to Appendix C in this data book for more information on external memory interfacing.

When deciding at what speed to operate the MC143150, the cost of the external memory will be an important consideration. There is a cost difference between a 200 ns memory (EPROM access time required at 5 MHz) and a 120 ns memory (10 MHz access time) which is rated over the full industrial temperature range, particularly in surface mount packages.

For multiple memory configurations (external EPROM, EEPROM, flash, and/or SRAM), additional cost savings due to slower memory map decode logic, and lower cost of the memory, can be realized at 5 MHz operation. Power consumption will be 30 – 40% lower at 5 MHz than at 10 MHz. Issues such as required data rate and I/O response time must be considered.

Running the Neuron Chip at a higher clock rate decreases the processing time. Proper prioritizing of "when" statements in the application program and use of timer counter objects can help to minimize latency.

Refer to Section D.2 regarding handling precautions and moisture sensitivity of the various Neuron devices.

NOTE: The MC143150FU, MC143150FU1, and MC143150B1FU devices are no longer available, but data regarding these devices are included in this section. **The MC143150B1FU1 is recommended for new designs.**

6.2 ELECTRICAL SPECIFICATIONS

6.2.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range (Referenced to V_{SS})	V_{DD}	- 0.3 to 7.0 V	V
Input Voltage Range (Referenced to V_{SS})	V_{in}	- 0.3 to $V_{DD} + 0.3$	V
Maximum Drain Current	I_{DD}	200	mA
Maximum Source Current	I_{SS}	300	mA
Maximum Power Dissipation	P_D	800	mW
Operating Temperature	T_A	- 40 to + 85	°C
Storage Temperature Range	T_{stg}	- 65 to + 150	°C

6.2.2 Recommended Operating Conditions

(Voltages referenced to V_{SS} , $T_A = - 40$ to + 85°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
TTL Low-Level Input Voltage	V_{IL}	V_{SS}	0.8	V
TTL High-Level Input Voltage	V_{IH}	2.0	V_{DD}	V
CMOS Low-Level Input Voltage	V_{IL}	V_{SS}	0.8	V
CMOS High-Level Input Voltage	V_{IH}	$V_{DD} - 0.8$	V_{DD}	V
Operating Free-Air Temperature	T_A	- 40*	+ 85	°C

*Writes to EEPROM are guaranteed down to - 20°C @ all frequencies for MC143150FU and MC143120DW devices and down to - 40°C @ all frequencies for all other Neuron Chip devices.

6.2.3 Electrical Characteristics ($V_{DD} = 4.5$ to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage IO0 - IO10, D0 - D7, CP0, CP3, CP4, SERVICE CP0, CP1 (Differential) (See Section 6.2.10) Reset (MC143150FU, FU1, MC143120DW) Reset (MC143150B1FU, B1FU1, E2)	V_{IL}	—	—	0.8 Programmable 0.8 0.3 V_{DD}	V
Input High Voltage IO0 - IO10, D0 - D7, CP0, CP3, CP4, service pin CP0, CP1 (Differential) (See Section 6.2.10) Reset (MC143150FU, FU1, MC143120DW) Reset (MC143150B1FU, B1FU1, E2)	V_{IH}	2.0 Programmable	— —	— — $V_{DD} - 0.7$ $V_{DD} - 0.7$	V
Low-Level Output Voltage Standard Outputs ($I_{OL} = 1.4$ mA) (Note 1) High Sink (IO0 - IO3), SERVICE, RESET ($I_{OL} = 20$ mA) High Sink (IO0 - IO3), SERVICE, RESET ($I_{OL} = 10$ mA) Maximum Sink (CP2, CP3) ($I_{OL} = 40$ mA) Maximum Sink (CP2, CP3) ($I_{OL} = 15$ mA)	V_{OL}	— — — — —	— — — — —	0.4 0.8 0.4 1.0 0.4	V
High-Level Output Voltage Standard Outputs ($I_{OH} = -1.4$ mA) (Note 1) High Sink (IO0 - IO3), SERVICE ($I_{OH} = -1.4$ mA) Maximum Source (CP2, CP3) ($I_{OH} = -40$ mA) Maximum Source (CP2, CP3) ($I_{OH} = -15$ mA)	V_{OH}	$V_{DD} - 0.4$ $V_{DD} - 0.4$ $V_{DD} - 1.0$ $V_{DD} - 0.4$	— — — —	— — — —	V
Hysteresis (Excluding CLK1, RESET)	V_{hys}	175	—	—	mV
Input Current (Excluding pullups) (V_{SS} to V_{DD}) (Note 2)	I_{in}	- 10	—	10	μA

Parameter	Symbol	Min	Typ	Max	Unit
MC143150B1FU, B1FU1					
Pullup Source Current ($V_{out} = 0$ V, Output = High-Z) (Note 2)	I_{pu}	60	—	260	μ A
Operating Mode Supply Current (Notes 3, 4)					mA
10 MHz Clock		—	15	25	
5 MHz Clock		—	8	13	
2.5 MHz Clock		—	4.5	7	
1.25 MHz Clock		—	2.4	4.2	
0.625 MHz Clock		—	1.5	2.5	
Sleep Mode Supply Current (Notes 3, 4)		—	15	100	μ A

MC143150FU, FU1					
Pullup Source Current ($V_{out} = 0$ V, Output = High-Z) (Note 2)	I_{pu}	30	—	300	μ A
Operating Mode Supply Current (Notes 3, 4)					mA
10 MHz Clock		—	32	60	
5 MHz Clock		—	22	40	
2.5 MHz Clock		—	16	32	
1.25 MHz Clock		—	13	27	
0.625 MHz Clock		—	12	25	
Sleep Mode Supply Current (Notes 3, 4)		—	0.5	2	mA

MC143120B1DW					
Pullup Source Current ($V_{out} = 0$ V, Output = High-Z) (Note 2)	I_{pu}	60	—	260	μ A
Operating Mode Supply Current (Notes 3, 4, and 5)					mA
10 MHz Clock		—	14	25	
5 MHz Clock		—	7.5	13	
2.5 MHz Clock		—	4.5	7	
1.25 MHz Clock		—	3.2	4.2	
0.625 MHz Clock		—	1.6	2.5	
Sleep Mode Supply Current (Note 3,4)		—	9	100	μ A

MC143120DW					
Pullup Source Current ($V_{out} = 0$ V, Output = High-Z) (Note 2)	I_{pu}	30	—	300	μ A
Operating Mode Supply Current (Notes 3, 5)					mA
10 MHz Clock		—	36	60	
5 MHz Clock		—	22	38	
2.5 MHz Clock		—	16	26	
1.25 MHz Clock		—	10	22	
0.625 MHz Clock		—	8	18	
Sleep Mode Supply Current (Notes 3, 5)		—	0.6	2	mA

MC143120E2DW					
Pullup Source Current ($V_{out} = 0$ V, Output = High-Z) (Note 2)	I_{pu}	60	—	260	μ A
Operating Mode Supply Current (Notes 3, 5)					mA
10 MHz Clock		—	16	N/A	
5 MHz Clock		—	8		
2.5 MHz Clock		—	5.0		
1.25 MHz Clock		—	3.5		
0.625 MHz Clock		—	1.8		
Sleep Mode Supply Current (Notes 3, 5)		—	9	100	μ A

NOTES:

- Standard outputs are A0 – A15, D0 – D7, IO4 – IO10, CP0, CP1, CP4, \bar{E} , and \bar{R}/\bar{W} . (\bar{RESET} is a CMOS open drain input/output. CLK2 must have ≤ 15 pF.
- IO4 – IO7 and $\bar{SERVICE}$ have configurable pullups. \bar{RESET} has a permanent pullup.
- Supply current measurement conditions: all outputs under no-load conditions, all inputs ≤ 0.2 V or $\geq (V_{DD} - 0.2)$ V, configurable pullups off, crystal oscillator clock input, differential receiver disabled. The differential receiver adds approximately 200 μ A typical and 600 μ A maximum when enabled. It is enabled on either of the following conditions:
 - Neuron Chip in Operating mode and Comm Port in Differential mode.
 - Neuron Chip in Sleep mode and Comm Port in Differential mode and Comm Port Wakeup not masked.
- Typical values are at midpoint of voltage range and 25°C only.

VDD Trip Point for Reset

Part Number	Min	Typ	Max	Unit
MC143150B1FU1	2.1	3.3	4.4	V
MC143120B1DW	2.1	3.3	4.4	V
MC143120E2DW	3.8	4.1	4.4	V

6.2.4 External Memory Interface Timing — MC143150B1FU1, VDD ± 10%

(VDD=4.5 to 5.5 V, TA = -40 to +85°C)

Symbol	Parameter	Min	Max	Unit
t _{cyc}	Memory Cycle Time (System Clock Period) (Note 1)	200	3200	ns
PWEH	Pulse Width, \bar{E} High	t _{cyc} /2 - 5	t _{cyc} /2 + 5	ns
PWEL	Pulse Width, \bar{E} Low	t _{cyc} /2 - 5	t _{cyc} /2 + 5	ns
t _{AD}	Delay, \bar{E} High to Address Valid	—	50	ns
t _{AH}	Address Hold Time after \bar{E} High	10	—	ns
t _{RD}	Delay, \bar{E} High to R/ \bar{W} Valid Read	—	45	ns
t _{RH}	R/ \bar{W} Hold Time Read after \bar{E} High	5	—	ns
t _{WR}	Delay, \bar{E} High to R/ \bar{W} Valid Write	—	45	ns
t _{WH}	R/ \bar{W} Hold Time Write after \bar{E} High	5	—	ns
t _{DSR}	Read Data Setup Time to \bar{E} High	20	—	ns
t _{DHR}	Data Hold Time Read after \bar{E} High	0	—	ns
t _{DHW}	Data Hold Time Write after \bar{E} High (Note 4,5)	20	—	ns
t _{DDW}	Delay, \bar{E} Low to Data Valid	—	60	ns
t _{DHZ}	Data Three State Hold Time after \bar{E} Low (Note 3)	0	—	ns
t _{DDZ}	Delay, \bar{E} High to Data Three-State (Note 4)	—	60	ns
t _{acc}	External Memory Access Time (t _{acc} = t _{cyc} - t _{AD} - t _{DSR})	130	—	ns

NOTES:

1. t_{cyc} = 2*1/f, where f is the input clock (CLK1) frequency (10, 5, 2.5, 1.25, or 0.625 MHz). Refer to Clocking System for more details on the CLK1 input clock, including the accuracy requirements (in ppm) and duty cycle requirements.
2. Refer to Figure 6-3, Test Point Levels for E Pulse Width Measurements, for detailed measurement information.
3. The three-state condition is when the device is not actively driving data. Refer to Figure 6-2, Signal Loading for Timing Specifications Unless Otherwise Specified, and Figure 6-5, Test Point Levels for Three-State to Driven Time Measurements, for detailed measurement information.
4. Refer to Figure 6-6, Signal Loading for Driven to Three-State Time Measurements, and Figure 6-7, Test Point Levels for Driven to Three-State Time Measurements, for detailed measurement information.
5. The data hold parameter, t_{DHW}, is measured to the disable levels shown in Figure 6-7, Test Point Levels for Driven to Three-State Time Measurements, rather than to the traditional data invalid levels.

6.2.5 External Memory Interface Timing* — MC143150B1FU1, Over Specified Voltage

($V_{DD}=3.8$ to 5.5 V, $T_A = -40$ to $+85^\circ\text{C}$)

Symbol	Parameter	Min	Max	Unit
t_{cyc}	Memory Cycle Time (System Clock Period) (Note 1)	TBD	TBD	ns
PW_{EH}	Pulse Width, \bar{E} High (Note 2)	TBD	TBD	ns
PW_{EL}	Pulse Width, \bar{E} Low (Note 2)	TBD	TBD	ns
t_{AD}	Delay, \bar{E} High to Address Valid	—	TBD	ns
t_{AH}	Address Hold Time After \bar{E} High	TBD	—	ns
t_{RD}	Delay, \bar{E} High to R/\bar{W} Valid Read	—	TBD	ns
t_{RH}	R/\bar{W} Hold Time Read after \bar{E} High	TBD	—	ns
t_{WR}	Delay, \bar{E} High to R/\bar{W} Valid Write	—	TBD	ns
t_{WH}	R/\bar{W} Hold Time Write after \bar{E} High	TBD	—	ns
t_{DSR}	Read Data Setup Time to \bar{E} High	TBD	—	ns
t_{DHR}	Data Hold Time Read after \bar{E} High	TBD	—	ns
t_{DHW}	Data Hold Time Write after \bar{E} High (Note 4,5)	TBD	—	ns
t_{DDW}	Delay, \bar{E} Low to Data Valid	—	TBD	ns
t_{DHZ}	Data Three State Hold Time after \bar{E} Low (Note 3)	TBD	—	ns
t_{DDZ}	Delay, \bar{E} High to Data Three-State (Note 4)	—	TBD	ns
t_{acc}	External Memory Access Time ($t_{acc} = t_{cyc} - t_{AD} - t_{DSR}$)	TBD	—	ns

NOTES:

- $t_{cyc} = 2 \cdot 1/f$, where f is the input clock (CLK1) frequency (5, 2.5, 1.25, or 0.625 MHz). Refer to Clocking System for more details on the CLK1 input clock, including the accuracy requirements (in ppm) and duty cycle requirements.
- Refer to Figure 6-3, Test Point Levels for E Pulse Width Measurements for detailed measurement information.
- The three-state condition is when the device is not actively driving data. Refer to Figure 6-2, Signal Loading for Timing Specifications Unless Otherwise Specified and Figure 6-5, Test Point Levels for Three-State to Driven Time Measurements for detailed measurement information.
- Refer to Figure 6-6, Signal Loading for Driven to Three-State Time Measurements and Figure 6-7, Test Point Levels for Driven to Three-State Time Measurements for detailed measurement information.
- The data hold parameter, t_{DHW} , is measured to the disable levels shown in Figure 6-7 Test Point Levels for Driven to Three-State Time Measurements, rather than to the traditional data invalid levels.
- LVI Reset occurs between $3.8 < V_{DD} < 4.4$ V.
- This timing is for the range of $3.8 < V_{DD} < 5.5$ V. Table 6.2.4 reflects timing values for $4.5 < V_{DD} < 5.5$ V.

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6.2.6 External Memory Interface Timing* — MC143150B1FU, V_{DD} ± 10%

(V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C)

Symbol	Parameter	Min ³	Min	Max	Unit
t _{cyc}	Memory Cycle Time (System Clock Period) (Note 1)		200	3200	ns
PW _{EH}	Pulse Width, \bar{E} High		t _{cyc} /2 - 5	t _{cyc} /2 + 5	ns
PW _{EL}	Pulse Width, \bar{E} Low		t _{cyc} /2 - 5	t _{cyc} /2 + 5	ns
t _{AD}	Delay, \bar{E} High to Address Valid		—	32	ns
t _{AH}	Address Hold Time	0	10	—	ns
t _{RD}	Delay, \bar{E} High to R/W Valid Read		—	25	ns
t _{RH}	R/W Hold Time Read	0	5	—	ns
t _{DSR}	Read Data Setup Time		34	—	ns
t _{DHR}	Data Hold Time Read		0	—	ns
t _{WR}	Delay, \bar{E} High to R/W Valid Write		—	25	ns
t _{DDW}	Delay, \bar{E} Low to Data Valid		—	60	ns
t _{WH}	R/W Hold Time Write	0	5	—	ns
t _{DHW}	Data Hold Time Write		9	40	ns
t _{acc}	External Memory Access Time (t _{acc} = t _{cyc} - t _{AD} - t _{DSR})		134	—	ns

NOTES:

* All values are preliminary and subject to change.

1. t_{cyc} = 2•1/f, where f is the input clock frequency (10, 5, 2.5, 1.25, or 0.625 MHz).

2. t_{WDD} spec has been eliminated. When R/W goes low, the data bus is not driven until \bar{E} clock goes low.

3. New Parameters. The SC143150B1FU is only being shipped against a Required Order Authorization from the customer.

6.2.7 External Memory Interface Timing — MC143150FU, V_{DD} ± 10%

(V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C)

Symbol	Parameter	Min	Max	Unit
t _{cyc}	Memory Cycle Time (System Clock Period) (Note 1)	200	3200	ns
PW _{EH}	Pulse Width, \bar{E} High	t _{cyc} /2 - 5	t _{cyc} /2 + 5	ns
PW _{EL}	Pulse Width, \bar{E} Low	t _{cyc} /2 - 5	t _{cyc} /2 + 5	ns
t _{AD}	Delay, \bar{E} High to Address Valid	—	55	ns
t _{AH}	Address Hold Time	7	—	ns
t _{RD}	Delay, \bar{E} High to R/W Valid Read	—	25	ns
t _{RH}	R/W Hold Time Read	5	—	ns
t _{DSR}	Read Data Setup Time	55	—	ns
t _{DHR}	Data Hold Time Read	0	—	ns
t _{WR}	Delay, \bar{E} High to R/W Valid Write	—	25	ns
t _{WDD}	Delay, R/W Low to Data Drivers On (Note 2)	10	—	ns
t _{DDW}	Delay, \bar{E} Low to Data Valid	—	60	ns
t _{WH}	R/W Hold Time Write	5	—	ns

NOTES:

1. t_{cyc} = 2•1/f, where f is the input clock frequency.

2. See Figure 6-1. The Neuron Chip drives the previously read data until after the falling edge of \bar{E} . Therefore, an external memory and the Neuron Chip may both be driving the data lines to the same levels during this time without contention.

6.2.8 External Memory Interface Timing — MC143150FU, $V_{DD} \pm 5\%$

($V_{DD} = 4.75$ to 5.25 V, $T_A = -40$ to $+85^\circ\text{C}$)

Symbol	Parameter	Min	Max	Unit
t_{cyc}	Memory Cycle Time (System Clock Period) (Note 1)	200	3200	ns
PW_{EH}	Pulse Width, \bar{E} High	$t_{cyc}/2 - 5$	$t_{cyc}/2 + 5$	ns
PW_{EL}	Pulse Width, \bar{E} Low	$t_{cyc}/2 - 5$	$t_{cyc}/2 + 5$	ns
t_{AD}	Delay, \bar{E} High to Address Valid	—	45	ns
t_{AH}	Address Hold Time	8	—	ns
t_{RD}	Delay, \bar{E} High to R/W Valid Read	—	25	ns
t_{RH}	R/W Hold Time Read	5	—	ns
t_{DSR}	Read Data Setup Time	50	—	ns
t_{DHR}	Data Hold Time Read	0	—	ns
t_{WR}	Delay, \bar{E} High to R/W Valid Write	—	25	ns
t_{WDD}	Delay, R/W Low to Data Drivers On (Note 2)	10	—	ns
t_{DDW}	Delay, \bar{E} Low to Data Valid	—	60	ns
t_{WH}	R/W Hold Time Write	5	—	ns

NOTES:

- $t_{cyc} = 2 \cdot 1/f$, where f is the input clock frequency.
- See Figure 6-1. The Neuron Chip drives the previously read data until after the falling edge of \bar{E} . Therefore, an external memory and the Neuron Chip may both be driving the data lines to the same levels during this time without contention.

6.2.9 External Memory Interface Timing — MC143150FU1, $V_{DD} \pm 10\%$

($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to $+85^\circ\text{C}$)

Symbol	Parameter	Min	Max	Unit
t_{cyc}	Memory Cycle Time (System Clock Period) (Note 1)	400	3200	ns
PW_{EH}	Pulse Width, \bar{E} High	$t_{cyc}/2 - 5$	$t_{cyc}/2 + 5$	ns
PW_{EL}	Pulse Width, \bar{E} Low	$t_{cyc}/2 - 5$	$t_{cyc}/2 + 5$	ns
t_{AD}	Delay, \bar{E} High to Address Valid	—	80	ns
t_{AH}	Address Hold Time	7	—	ns
t_{RD}	Delay, \bar{E} High to R/W Valid Read	—	50	ns
t_{RH}	R/W Hold Time Read	5	—	ns
t_{DSR}	Read Data Setup Time	80	—	ns
t_{DHR}	Data Hold Time Read	0	—	ns
t_{WR}	Delay, \bar{E} High to R/W Valid Write	—	50	ns
t_{WDD}	Delay, R/W Low to Data Drivers On (Note 2)	10	—	ns
t_{DDW}	Delay, \bar{E} Low to Data Valid	—	100	ns
t_{WH}	R/W Hold Time Write	5	—	ns

NOTES:

- $t_{cyc} = 2 \cdot 1/f$, where f is the input clock frequency.
- See Figure 6-1. The Neuron Chip drives the previously read data until after the falling edge of \bar{E} . Therefore, an external memory and the Neuron Chip may both be driving the data lines to the same levels during this time without contention.

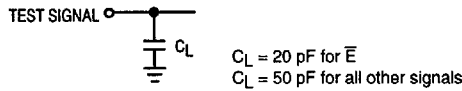


Figure 6-2. Signal Loading for Timing Specifications Unless Otherwise Specified

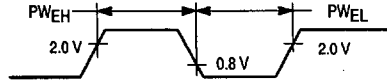
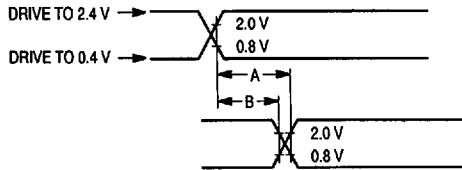


Figure 6-3. Test Point Levels for \bar{E} Pulse Width Measurements



- A — Signal valid to signal valid specification (maximum or minimum)
- B — Signal valid to signal invalid specification (maximum or minimum)

Figure 6-4. Drive Levels and Test Point Levels for Timing Specifications Unless Otherwise Specified

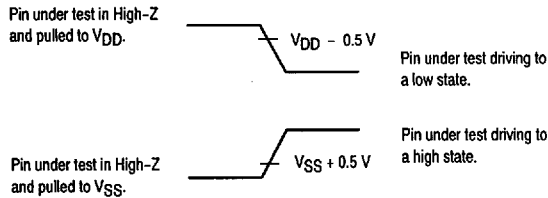


Figure 6-5. Test Point Levels for Three-State To Driven Time Measurements

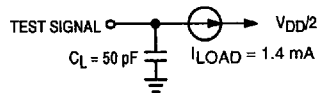


Figure 6-6. Signal Loading for Driven to Three-State Time Measurements

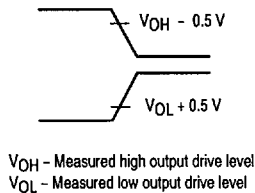


Figure 6-7. Test Point Levels for Driven To Three-State Time Measurements

6.2.10 Communications Port Programmable Hysteresis Values

(Expressed as differential peak to peak voltages in terms of V_{DD})

Hysteresis*	V_{hys} Min	V_{hys} Typ	V_{hys} Max
0	0.019 V_{DD}	0.027 V_{DD}	0.035 V_{DD}
1	0.040 V_{DD}	0.054 V_{DD}	0.068 V_{DD}
2	0.061 V_{DD}	0.081 V_{DD}	0.101 V_{DD}
3	0.081 V_{DD}	0.108 V_{DD}	0.135 V_{DD}
4	0.101 V_{DD}	0.135 V_{DD}	0.169 V_{DD}
5	0.121 V_{DD}	0.162 V_{DD}	0.203 V_{DD}
6	0.142 V_{DD}	0.189 V_{DD}	0.236 V_{DD}
7	0.162 V_{DD}	0.216 V_{DD}	0.270 V_{DD}

*Hysteresis values are under the conditions that the input signal swing is 200 mV greater than the programmed value.

6.2.11 Communications Port Programmable Glitch Filter Values*

[Receiver (end-to-end) filter values expressed as transient pulse suppression times]

Filter (F)	Min	Typ	Max	Unit
0	10	75	140	ns
1	120	410	700	ns
2	240	800	1350	ns
3	480	1500	2600	ns

*Must be disabled if data rate is 1.25 Mbps.

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6.2.12 Receiver* (End-to-End) Absolute Asymmetry

(Worst case across hysteresis)

Filter (F)	Max ($ t_{PLH} - t_{PHL} $)	Unit
0	35	ns
1	150	ns
2	250	ns
3	400	ns

*Receiver input, $V_D = V_{CP0} - V_{CP1}$, at least 200 mV greater than hysteresis levels. See Figure 6-4.

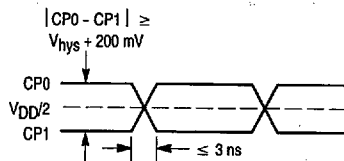


Figure 6-8. Receiver Input Waveform

6.2.13 Differential Receiver (End-to-End) Absolute Symmetry

Filter (F)	Hysteresis (H)	Max ($ t_{pLH} - t_{pHL} $)	Unit
0	0	24	ns

NOTES:

- CP0 and CP1 inputs each 0.60 V p-p, 1.25 MHz sine wave 180° out of phase with each other as shown in Figure 6-9.
 $V_{DD} = 5.00\text{ V} \pm 5\%$
- t_{pLH} : Time from input switching states from low to high to output switching states
 t_{pHL} : Time from input switching states from high to low to output switching states

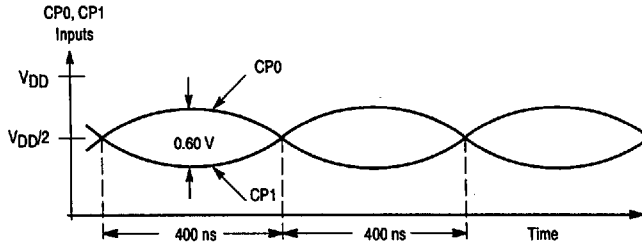


Figure 6-9. Communications Port Signal Input for Table 6.2.13

6.2.14 Differential Transceiver Electrical Characteristics

Characteristic	Min	Max
Receiver Common Mode Voltage Range to maintain hysteresis as specified in Table 4-4*	1.2 V	$V_{DD} - 2.2\text{ V}$
Receiver Common Mode Range to operate with unspecified hysteresis	0.9 V	$V_{DD} - 1.75\text{ V}$
Input Offset Voltage	$-0.05 V_{hys} - 35\text{ mV}$	$0.05 V_{hys} + 35\text{ mV}$
Propagation Delay ($F = 0, V_{ID} = V_{hys}/2 + 200\text{ mV}$)	—	230 ns
Input Resistance	5 MΩ	—
Wake-Up Time	—	10 μs

* Common mode voltage is defined as the average value of the waveform at each input at the time switching occurs.

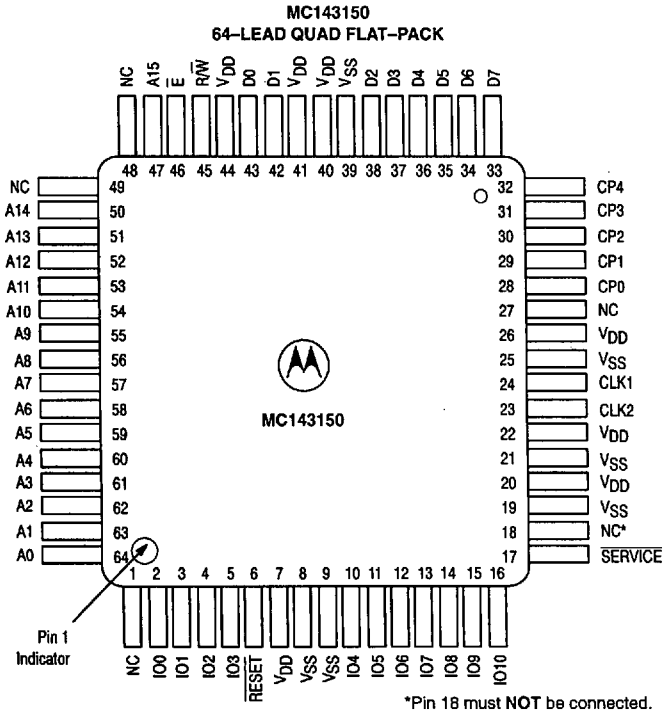
6.3 MECHANICAL SPECIFICATIONS

6.3.1 Pin Descriptions

Pin Name	I/O	Pin Function	MC143150 Pin Number	MC143120 Pin Number
CLK1	Input	Oscillator connection or external clock input.	24	15
CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1. One Load.	23	14
RESET	I/O (Built-In Pullup)	Reset pin (active low).	6	1
SERVICE	I/O (Built-In Configurable Pullup)	Service pin. Indicator output during operation.	17	8
IO0 – IO3	I/O	Large current–sink capacity (20 mA). General I/O port.	2, 3, 4, 5	7, 6, 5, 4
IO4 – IO7	I/O (Built-In Configurable Pullup)	General I/O port. One of IO4 to IO7 can be specified as No. 1 timer/counter input with IO0 as output. IO4 can be used as the No. 2 timer/counter input with IO1 as output.	10, 11, 12, 13	3, 30, 29, 28
IO8 – IO10	I/O	General I/O port. Can be used for serial communication with other devices.	14, 15, 16	27, 26, 24
D0 – D7	I/O	Memory data bus.	43, 42, 38, 37, 36, 35, 34, 33	N/A
R/W	Output	Read/write control output port for external memory.	45	N/A
E	Output	Control output port for external memory.	46	N/A
A15 – A0	Output	Address output port.	47, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64	N/A
VDD	Input	Power input (5 V nom). All VDD pins must be connected together externally.	7, 20, 22, 26, 40, 41, 44	2, 11, 12, 18, 25, 32
VSS	Input	Power input (0 V, GND). All VSS pins must be connected together externally.	8, 9, 19, 21, 25, 39	9, 10, 13, 16, 23, 31
CP0 – CP4	Communication Network Interface	Bidirectional port that supports communications protocols by specifying mode.	28, 29, 30, 31, 32	19, 20, 17, 21, 22
NC	N/A	No internal connection. Leave open. CAUTION: Pin 18 of the MC143150 MUST NOT have any external connection.	1, 18, 27, 48, 49	N/A

6

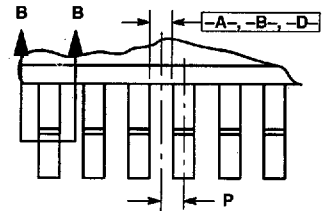
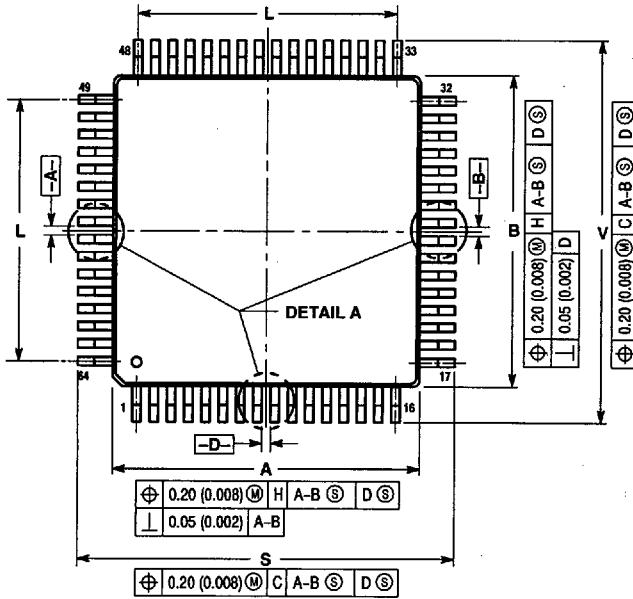
6.3.2 MC143150 Pin Assignments



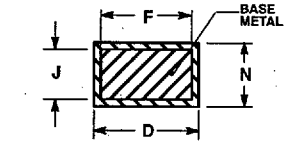
The larger dimple at the bottom left of the marking indicates pin 1.

6.3.3 MC143150 Package Dimensions

MC143150FU1/B1FU/B1FU1
 PLASTIC
 64-LEAD QUAD FLAT-PACK
 CASE 840C-04

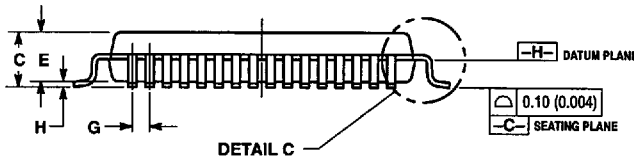


DETAIL A

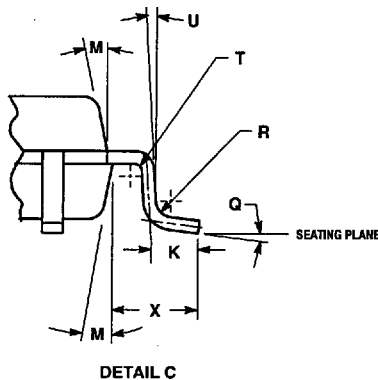


SECTION B-B

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
 4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
 5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
 6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
 7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.53 (0.021). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
 8. DIMENSION K IS TO BE MEASURED FROM THE THEORETICAL INTERSECTION OF LEAD FOOT AND LEG CENTERLINES.



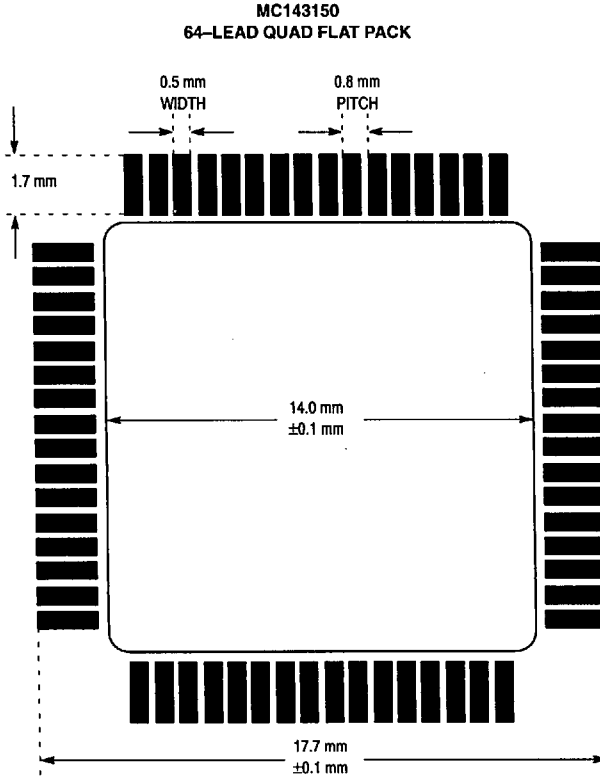
DETAIL C



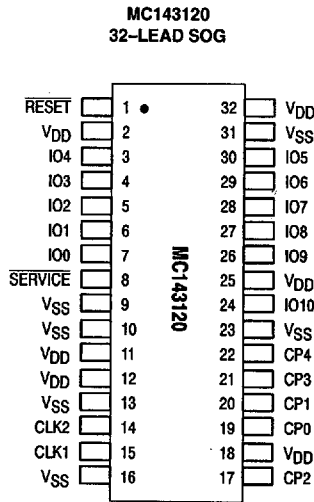
DETAIL C

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	13.90	14.10	0.547	0.555
C	2.07	2.46	0.081	0.097
D	0.30	0.45	0.012	0.018
E	2.00	2.40	0.079	0.094
F	0.30	---	0.012	---
G	0.80 BSC	---	0.031 BSC	---
H	0.067	0.250	0.003	0.010
J	0.190	0.230	0.005	0.090
K	0.50	0.66	0.020	0.026
L	12.00 REF	---	0.472 REF	---
M	5°	10°	---	---
N	0.130	0.170	0.005	0.007
P	0.40 BSC	---	0.016 BSC	---
Q	2°	8°	---	---
R	0.13	0.30	0.005	0.012
S	16.20	16.60	0.638	0.654
T	0.20 REF	---	0.008 REF	---
U	0°	---	---	---
V	16.20	16.60	0.638	0.654
X	1.10	1.30	0.043	0.051

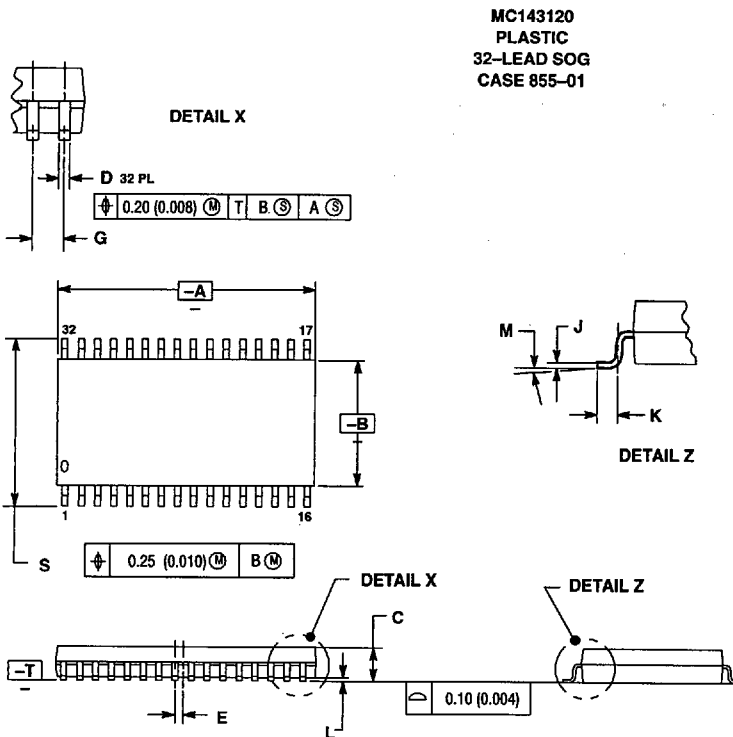
6.3.4 MC143150 Pad Layout



6.3.5 MC143120 Pin Assignment



6.3.6 MC143120 Package Dimensions

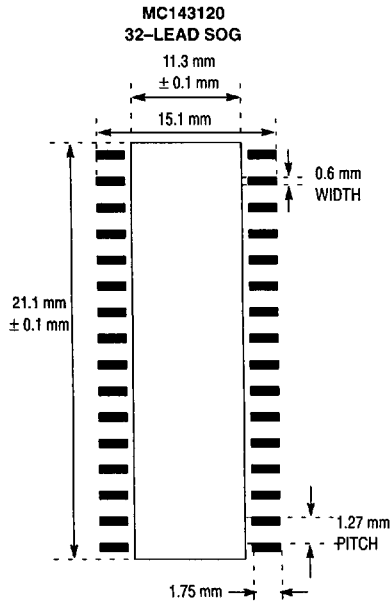


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.40	20.70	0.803	0.815
B	11.10	11.30	0.437	0.445
C	2.75	3.04	0.108	0.120
D	0.35	0.50	0.014	0.020
E	0.64 BSC		0.025 BSC	
G	1.27 BSC		0.050 BSC	
J	0.14	0.32	0.006	0.012
K	0.60	1.00	0.024	0.039
L	0.10	0.35	0.004	0.014
M	0°	8°	0°	8°
S	13.80	14.40	0.543	0.567

6.3.7 MC143120 Pad Layout



6.3.8 Sockets for Neuron Chips

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that these are the only suppliers.

Integrated Circuit	Manufacturer	Part Number
MC143120	Yamaichi	IC51-0322-667-2
MC143150	Enplas	FPQ-64-0.8-10A
MC143150	Enplas	FPQ-64-0.8-02*

* This is a tighter-fitting socket than the one above, and is used on Motorola's M143120EVK Test Board.