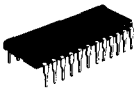
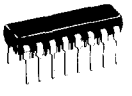
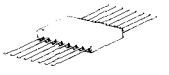
MC10,100/10,200 Series (-30 to +85°C)
MC10,500/10,600 Series (-55 to +125°C)

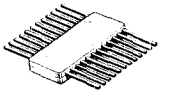
MECL 10,000 has an excellent speed-power product, has relatively slow rise and fall times, and transmission-line drive capability. The combination of versatile logic functions and the 2.0 ns propagation delay make MECL 10,000 a versatile family for data handling and processing systems.

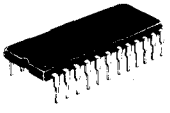
Circuit design with MECL 10,000 is unusually convenient. The differential amplifier input and emitter-follower output permit high fanout, the wired-OR option, and complementary outputs. MECL III is directly compatible with MECL 10,000, and can be used to extend the speed capability of the MECL 10,000 series.

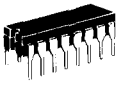

L SUFFIX
CERAMIC PACKAGE
CASE 623

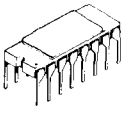

P SUFFIX
PLASTIC PACKAGE
CASE 648


F SUFFIX
CERAMIC PACKAGE
CASE 650


F SUFFIX
CERAMIC PACKAGE
CASE 652


P SUFFIX
PLASTIC PACKAGE
CASE 649


L SUFFIX
CERAMIC PACKAGE
CASE 620


AL SUFFIX
CERAMIC PACKAGE
CASE 690

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C)

Function	Type① -30 to +85°C	Type① -55 to +125°C	Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
Quad 2-Input NOR Gate With Strobe	MC10100	–	2.0	100	620
Quad OR/NOR Gate	MC10101	MC10501	2.0	100	620,648,650
Quad 2-Input NOR Gate	MC10102	MC10502	2.0	100	620,648,650
Quad 2-Input OR Gate	MC10103	–	2.0	100	620
Quad 2-Input AND Gate	MC10104	MC10504	2.7	140	620,648,650
Triple 2-3-2-Input OR/NOR Gate	MC10105	MC10505	2.0	90	620,648,650
Triple 4-3-3-Input NOR Gate	MC10106	MC10506	2.0	90	620,648,650
Triple 2-Input Exclusive OR/Exclusive NOR	MC10107	MC10507	2.5	110	620,648,650
Dual 4-5-Input OR/NOR Gate	MC10109	MC10509	2.0	60	620,648,650
Dual 3-Input 3-Output OR Gate	MC10110	–	2.4	160	620,648
Dual 3-Input 3-Output NOR Gate	MC10111	–	2.4	160	620,648
Quad Exclusive OR Gate	MC10113	–	2.5	175	620
Triple Line Receiver	MC10114	MC10514	2.4	145	620,648,650
Quad Line Receiver	MC10115	MC10515	2.0	110	620,648,650
Triple Line Receiver	MC10116	MC10516	2.0	85	620,648,650
Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate	MC10117	MC10517	2.3	100	620,648,650
Dual 2-Wide 3-Input OR-AND Gate	MC10118	MC10518	2.3	100	620,648,650
4-Wide 4-3-3-3-Input OR-AND Gate	MC10119	MC10519	2.3	100	620,648,650
4-Wide OR-AND/OR-AND-INVERT Gate	MC10121	MC10521	2.3	100	620,648,650
Triple 4-3-3-Input Bus Driver	MC10123	–	3.0	310	620
Quad MTTL to MECL Translator	MC10124	MC10524	3.5	380	620,648,650
Quad MECL to MTTL Translator	MC10125	MC10525	4.5	380	620,648,650
Dual MECL to MOS Translator	MC10127	–	–	–	620
Bus Driver	MC10128	–	12.0	700	620
Quad Bus Receiver	MC10129	–	10.0	750	620
Dual Latch	MC10130	MC10530	2.5	155	620,648,650
Dual Type D Master-Slave Flip-Flop	MC10131	MC10531	f = 160 MHz	235	620,648,650
Dual Multiplexer With Latch and Common Reset	MC10132	–	3.0	225	620,648
Quad Latch	MC10133	MC10533	4.0	310	620,648,650
Multiplexer with Latch	MC10134	–	3.0	225	620,648
Dual J-K Master-Slave Flip-Flop	MC10135	MC10535	f = 140 MHz	280	620,648,650
Universal Hexadecimal Counter	MC10136	MC10536	f = 150 MHz	625	620,650

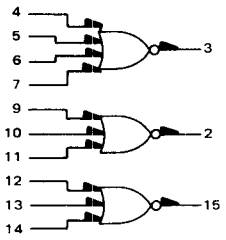
① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*External Load Power not included.

2

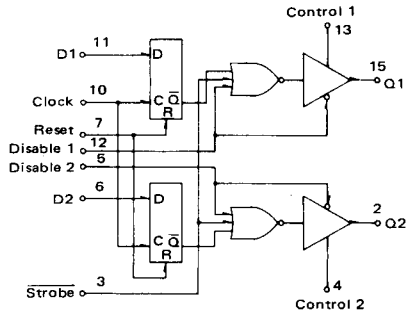
DRIVER

MC10123
Triple 4-3-3 Input Bus Driver



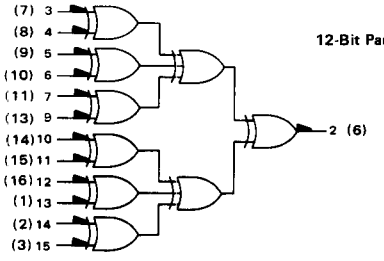
P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

MC10128
Bus Driver



P_D = 700 mW typ/pkg (No Load)
t_{pd} = 12 ns typ

PARITY CHECKER



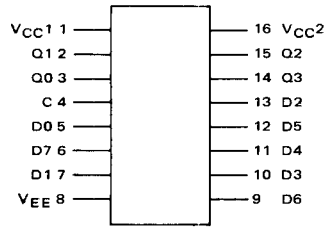
MC10160
MC10560
12-Bit Parity Generator-Checker

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

P_D = 320 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ

ENCODER

MC10165
8-Input
Priority Encoder



TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	L
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	H
L	L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	H	L
L	L	L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H
L	L	L	L	H	ϕ	ϕ	ϕ	H	H	L	L
L	L	L	L	L	H	ϕ	ϕ	H	H	L	H
L	L	L	L	L	L	H	ϕ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

ϕ = Don't Care

P_D = 545 mW typ/pkg
t_{pd} = 7.0 ns typ (Data to Output)

MC10128

Advance Information

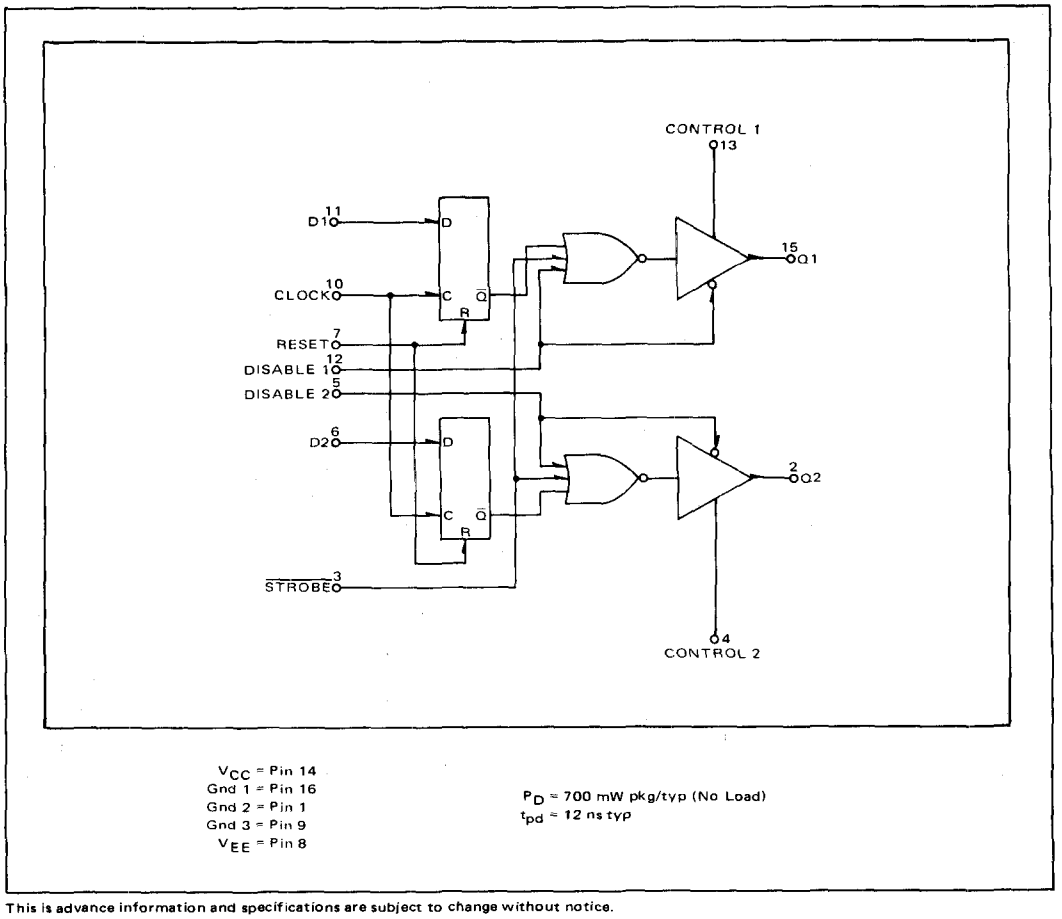
The MC10128 is designed to provide outputs which are compatible with IBM-type bus levels; or, if desired, it will drive TTL type loads and/or provide TTL three-state outputs. The inputs accept MECL 10,000 levels. The MC10128 output levels can be accepted by the MC10129 Bus Receiver.

The operating mode IBM or TTL is selected by tying the external control pins to ground or leaving them open. Leaving a control pin open selects the TTL mode, and tying a control pin to ground selects the IBM mode.

The TTL mode will drive a 25-ohm load, terminated to +1.5 Vdc or a 50-ohm load, terminated to ground. The device has totem-pole type outputs, but it also has a disable input for three-state logic operation when the circuit is used in the TTL mode. When in the high state the disable input causes the output to exhibit a high impedance state when it would normally be a positive logic "1" state. When the strobe is in the high state it inhibits the output data to the low state.

Latches are provided on each data input for temporary storage. When the clock input is in the low logic state, information present at the data inputs D1 and D2 will be fed directly to the latch output. When the clock goes high, the input data is latched. The outputs are gated to allow full bus driving and strobing capability.

The MC10128 is useful in interfacing and bus applications in central processors, mini-computers, and peripheral equipment.



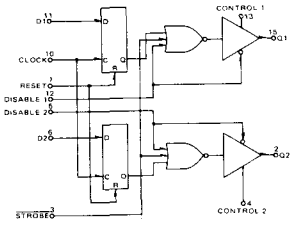
V_{CC} = Pin 14
Gnd 1 = Pin 16
Gnd 2 = Pin 1
Gnd 3 = Pin 9
V_{EE} = Pin 8

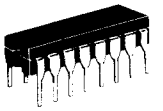
P_D = 700 mW pkg/typ (No Load)
t_{pd} = 12 ns typ

This is advance information and specifications are subject to change without notice.
See General Information section for packaging, and maximum ratings.

ELECTRICAL CHARACTERISTICS – MTTL MODE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.



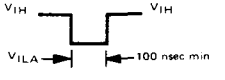


L SUFFIX
CERAMIC PACKAGE
CASE 620

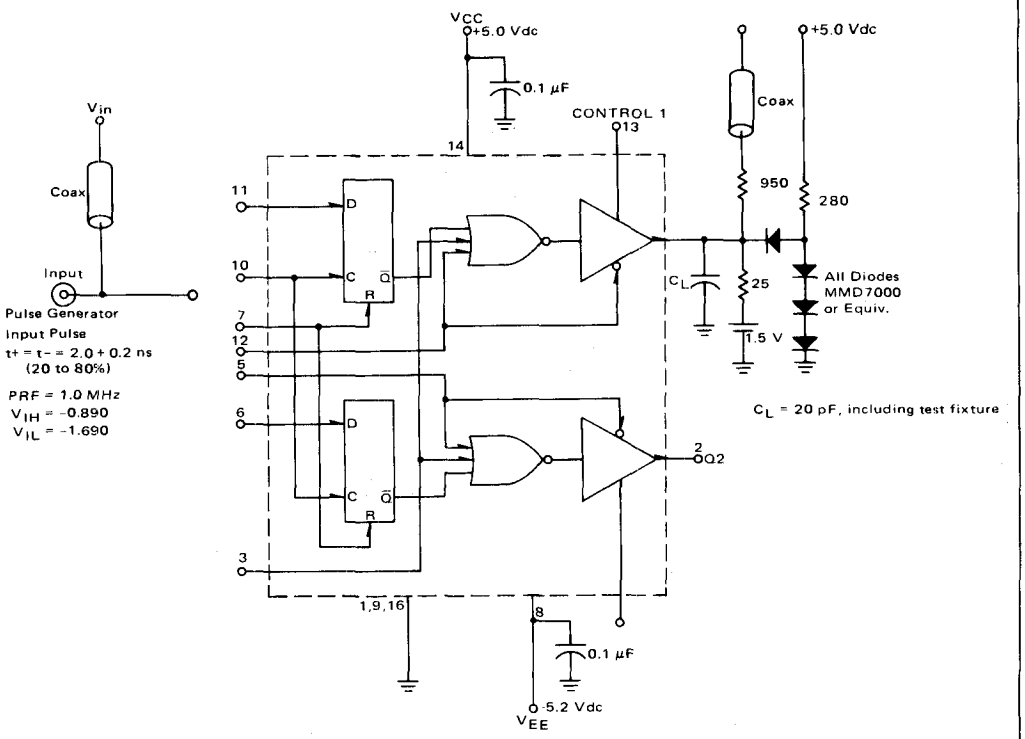
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	mAdc I_{OH1}	μAdc I_{OH2}	mAdc I_{OL}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+5.00	-50	-100	+56
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+5.00	-50	-100	+56
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+5.00	-50	-100	+56

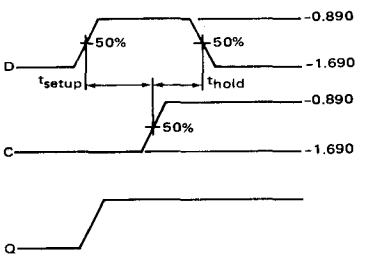
Characteristic	Symbol	Pin Under Test	MC10128L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}	Gnd
Negative Power Supply Drain Current	I_E	8	–	–	–	97	–	–	mAdc	6,11	–	–	–	8	14	–	–	–	1, 9,16
Positive Power Supply Drain Current	I_{CC}	14	–	–	–	73	–	–	mAdc	6,11	–	–	–	8	14	–	–	–	1, 9,16
Input Leakage Current	I_{inH}	3	–	–	–	620	–	–	μAdc	3	–	–	–	8	14	–	–	–	1, 9,16
		7	–	–	–	350	–	–		7	–	–	–			–	–	–	
		10	–	–	–	265	–	–		10	–	–	–			–	–	–	
		11	–	–	–	265	–	–		11	–	–	–			–	–	–	
		12	–	–	–	500	–	–		12	–	–	–			–	–	–	
	I_{inL}	All	–	–	0.5	–	–	–	μAdc	–		–	–	8	14	–	–	–	1, 9,16
Logic "1" Output Voltage	V_{OH}	15	–	–	2.5	–	–	–	Vdc	11	–	–	–	8	14	2,15	–	–	1, 9,16
		15	–	–	2.7	–	–	–	Vdc	11	–	–	–	8	14	–	2,15	–	1, 9,16
Logic "0" Output Voltage	V_{OL}	15	–	–	–	0.5	–	–	Vdc	3	–	–	–	8	14	–	–	2,15	1, 9,16
		2	–	–	–	0.5	–	–	Vdc	3	–	–	–	8	14	–	–	2,15	1, 9,16
Logic "1" Threshold Voltage	V_{OHA}	15	–	–	2.5	–	–	–	Vdc	11	7	–	10 ③	8	14	2,15	–	–	1, 9,16
		2	–	–	2.5	–	–	–	Vdc	6	7	–	10 ③	8	14	2,15	–	–	1, 9,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	–	–	0.5	–	–	Vdc	11	7,10	3	–	8	14	–	–	2,15	1, 9,16
		2	–	–	–	0.5	–	–	Vdc	6	7,10	3	–	8	14	–	–	2,15	1, 9,16
Output Short Circuit Current	I_{SC}	15	–	–	–	260	–	–	mAdc	11	–	–	–	8	14	–	–	–	1,2, 9,15,16
		2	–	–	–	260	–	–	mAdc	6	–	–	–	8	14	–	–	–	1,2, 9,15,16
Switching Times † Propagation Delay										-0.890 V	-1.690 V	Pulse In	Pulse Out						
Data Input	t_{11+15+}	,5	–	–	3.5	18	–	–	ns	–	10	11	15	8	14	–	–	–	1, 9 ,16
	t_{11-15-}	15	–	–		18	–	–		–	10	11				–	–	–	
Clock Input	t_{10-15+}	15 ①	–	–		20	–	–		–	–	10,11				–	–	–	
	t_{10-15-}	15 ②	–	–			–	–		–	–	10,11				–	–	–	
Reset Input	t_{7+15-}	15 ②	–	–			–	–		11	–	7,10				–	–	–	
	t_{7+2-}	2 ②	–	–			–	–		6	–	7,10	2			–	–	–	
STROBE Input	t_{3+15-}	15	–	–	2.5	18	–	–		11	10	3	15			–	–	–	
	t_{3-15+}	15	–	–			–	–		–			15			–	–	–	
	t_{3+2-}	2	–	–			–	–		6			2			–	–	–	
	t_{3-2+}	2	–	–			–	–		–			2			–	–	–	
Setup Time	t_{setupH}	15	–	–	–	–	–	–		–	–	10,11	15			–	–	–	
	t_{setupL}	15	–	–	–	–	–	–		–						–	–	–	
Hold Time	t_{holdH}	15	–	–	–	–	–	–		–	–					–	–	–	
	t_{holdL}	15	–	–	–	–	–	–		–	–					–	–	–	
Rise Time (20% to 80%)	t_{15+}	15	–	–	1.0	8.0	–	–		–	10	11				–	–	–	
Fall Time (20% to 80%)	t_{15-}	15	–	–	1.0	8.0	–	–		–	10	11				–	–	–	

* Apply V_{ILmin} individually to pin under test.
① Output latched to logic Low state prior to test.
② Output latched to logic High state prior to test.
† See waveforms
③ A pulse is applied to pin 10.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – MTTL MODE



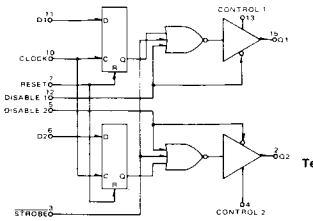


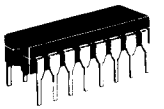
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

ELECTRICAL CHARACTERISTICS — IBM MODE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.





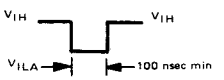
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	mAdc I_{OH1}	μAdc I_{OH2}	μAdc I_{OL}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+6.00	-59.3	-30	-240
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+6.00	-59.3	-30	-240
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+6.00	-59.3	-30	-240

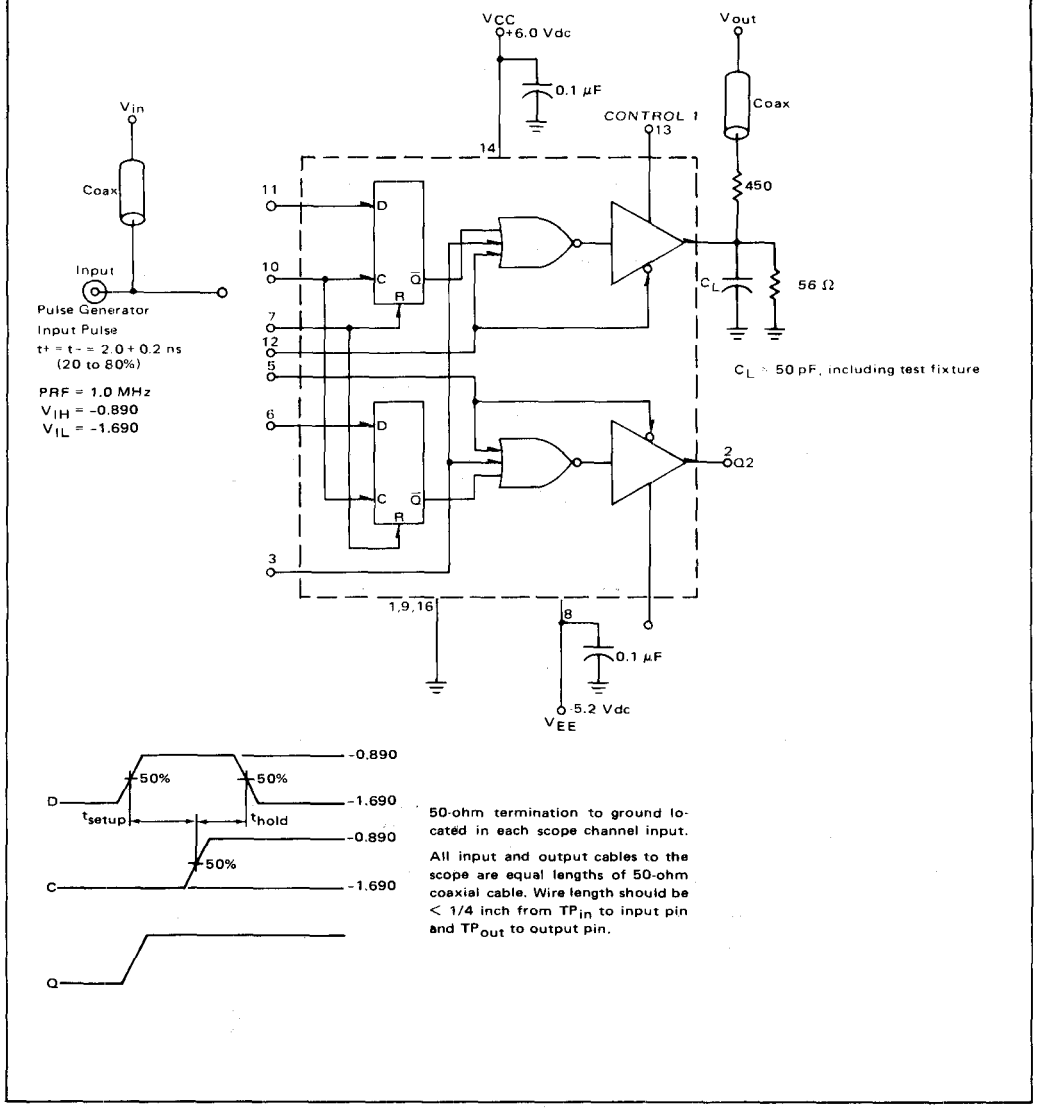
Characteristic	Symbol	Pin Under Test	MC10128L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}	Gnd
Negative Power Supply Drain Current	I_E	8	–	–	–	97	–	–	mAdc	6,11	–	–	–	8	14	–	–	–	1,4,9,13,16
Positive Power Supply Drain Current	I_{CC}	14	–	–	–	73	–	–	mAdc	6,11	–	–	–	8	14	–	–	–	1,4,9,13,16
Input Leakage Current	I_{inH}	3	–	–	–	620	–	–	μAdc	3	–	–	–	8	14	–	–	–	1,4,9,13,16
		7	–	–	–	350	–	–		7	–	–	–			–	–	–	
		10	–	–	–	265	–	–		10	–	–	–			–	–	–	
		11	–	–	–	265	–	–		11	–	–	–			–	–	–	
		12	–	–	–	500	–	–		12	–	–	–			–	–	–	
	I_{inL}	All	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	14	–	–	–	1,4,9,13,16
Logic "1" Output Voltage	V_{OH}	15	–	–	3.11	–	–	–	Vdc	11	–	–	–	8	14	2,15	–	–	1,4,9,13,16
		15	–	–	–	5.85	–	–	Vdc	11	–	–	–	8	14	–	2,15	–	1,4,9,13,16
Logic "0" Output Voltage	V_{OL}	15	–	–	-0.5	0.15	–	–	Vdc	3	–	–	–	8	14	–	–	2,15	1,4,9,13,16
		2	–	–	-0.5	0.15	–	–	Vdc	3	–	–	–	8	14	–	–	2,15	1,4,9,13,16
Logic "1" Threshold Voltage	V_{OHA}	15	–	–		2.9	–	–	Vdc	11	7	–	10 ③	8	14	2,15	–	–	1,4,9,13,16
		2	–	–		2.9	–	–	Vdc	6	7	–	10 ③	8	14	2,15	–	–	1,4,9,13,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	–	-0.5	0.25	–	–	Vdc	11	7,10	3	–	8	14	–	–	2,15	1,4,9,13,16
		2	–	–	-0.5	0.25	–	–	Vdc	6	7,10	3	–	8	14	–	–	2,15	1,4,9,13,16
Output Short Circuit Current	I_{SC}	15	–	–	–	320	–	–	mAdc	11	–	–	–	8	14	–	–	–	1,2,4,9,13,15,16
		2	–	–	–	320	–	–	mAdc	6	–	–	–	8	14	–	–	–	1,2,4,9,13,15,16
Switching Times † Propagation Delay										-0.890 V	-1.690 V	Pulse In	Pulse Out						
Data Input	t_{11+15+}	15	–	–	3.5	23	–	–	ns	–	10	11	15	8	14	–	–	–	1,4,9,13,16
	t_{11-15-}	15	–	–			–	–		–	10	11				–	–	–	
Clock Input	t_{10-15+}	15 ①	–	–			–	–			–	10,11				–	–	–	
	t_{10-15-}	15 ②	–	–			–	–		–	–	10,11				–	–	–	
Reset Input	t_{7+15-}	15 ②	–	–			–	–		11	–	7,10				–	–	–	
	t_{7+2-}	2 ②	–	–			–	–		6	–	7,10	2			–	–	–	
$\overline{\text{STROBE}}$ Input	t_{3+15-}	15	–	–	2.5		–	–		11	10	3	15			–	–	–	
	t_{3-15+}	15	–	–			–	–		–			15			–	–	–	
	t_{3+2-}	2	–	–			–	–		6			2			–	–	–	
	t_{3-2+}	2	–	–			–	–		–			2			–	–	–	
Setup Time	t_{setupH}	15	–	–	–	–	–	–		–	–	10,11	15			–	–	–	
	t_{setupL}	15	–	–	–	–	–	–		–	–					–	–	–	
Hold Time	t_{holdH}	15	–	–	–	–	–	–		–	–					–	–	–	
	t_{holdL}	15	–	–	–	–	–	–		–	–					–	–	–	
Rise Time (20% to 80%)	t_{15+}	15	–	–	1.0	8.0	–	–		–	10	11				–	–	–	
Fall Time (20% to 80%)	t_{15-}	15	–	–	1.0	8.0	–	–		–	10	11				–	–	–	

* Apply V_{ILmin} individually to pin under test.
① Output latched to logic Low state prior to test.
② Output latched to logic High state prior to test.
† See waveforms

③ A pulse is applied to pin 10.



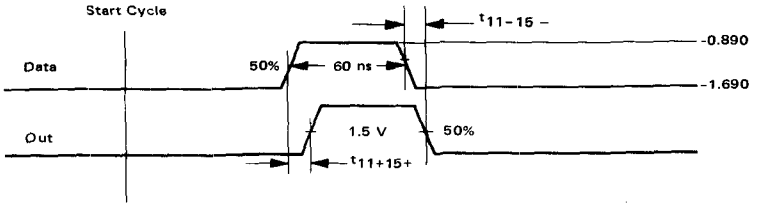
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – IBM MODE



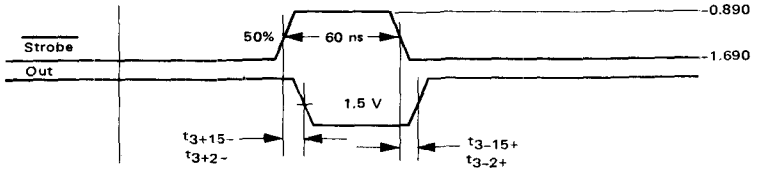
3

VOLTAGE WAVEFORMS

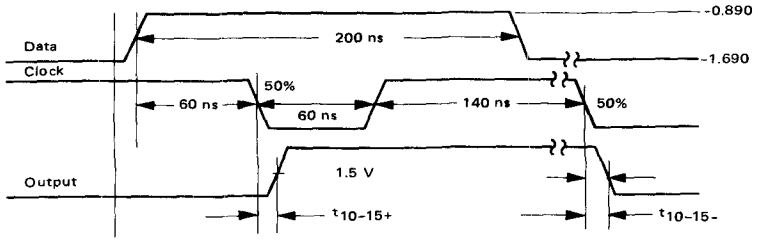
DATA INPUT



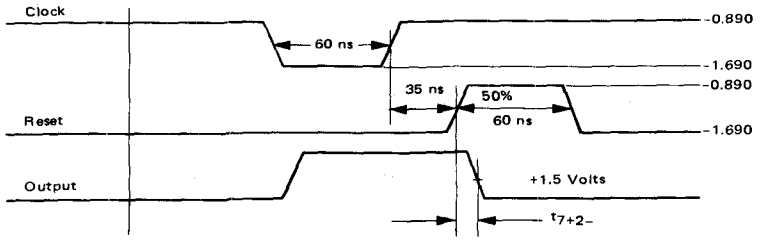
STROBE INPUT



CLOCK INPUT



RESET INPUT



TTL – MODE
V_{OL} = 0.5 Volts Max
V_{OH} = 2.5 Volts Min

IBM – MODE
V_{OL} = 0.25 Volts Max
V_{OH} = 5.85 Volts Min