M74HC373P
M74HC373DWP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC373 is a semiconductor integrated circuit consisting of eight D-type latches with 3-state outputs, common latch-enable input and output-enable input.

FEATURES

- High-fanout 3-state output: (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 13ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC373 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373.

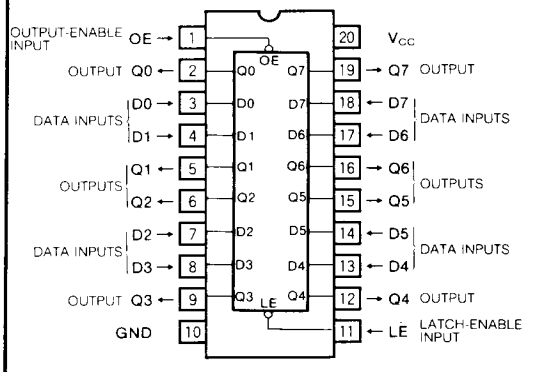
The M74HC373 consists of eight D-type latches with latch-enable input LE and output-enable input $\overline{OE}$ common to all circuits.

When LE is high, the signals of data input D will go through the latch and be output to Q. When the state of D changes, the state of Q will also change. When LE changes from high-level to low-level, the data existing immediatery prior to the change at D will be stored in the latch.

Even if other inputs are changed when LE is low, the contents stored in the latch will not be affected.

When $\overline{OE}$ is high, all outputs Q will become high-impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2V

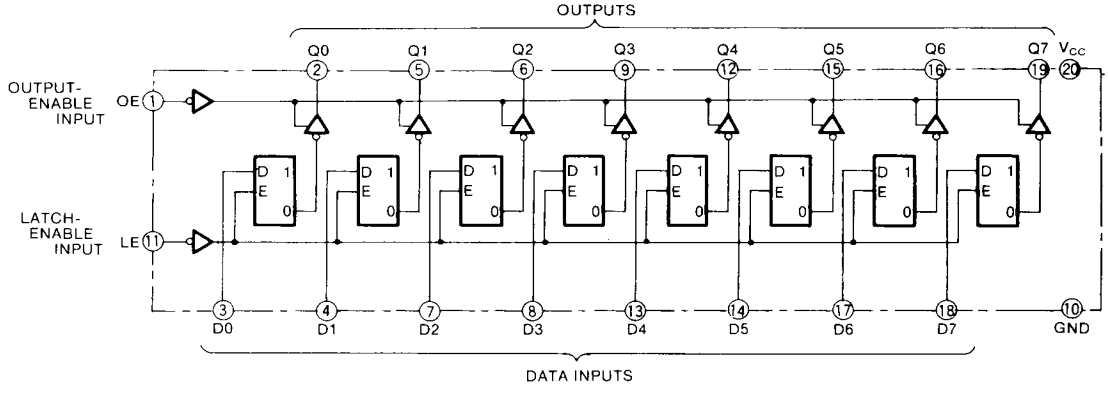
A version of the M74HC373 with the same pin connections and an inverted output, the M74HC533, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1 : Q^0 : Output state Q before LE changed
Z : High impedance
X : Irrelevant

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC373DWP, T_a = −40∼+80℃ and 80∼85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	Limits 25℃ Min	Typ	Max	−40∼+85℃ Min	Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V I_O = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V I_O = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 6.0mA	4.5			0.26		0.33	
			I_{OL} = 7.8mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O=V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O=GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				25	ns
t_{PHL}					25	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)				30	ns
t_{PHL}					30	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

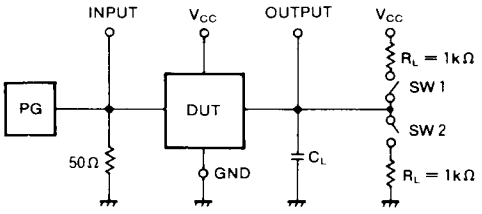
Symbol	Parameter	Test conditions	V_{CC}(V)	Limits 25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHL}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PLH}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PHL}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{LE}$ − Q)	C_L = 50pF (Note 4)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	
			4.5			35		44	
			6.0			30		37	
t_{PLH}		C_L = 150pF (Note 4)	2.0			225		284	
			4.5			45		57	
			6.0			38		48	
t_{PHL}			2.0			225		284	
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Output disabled capacitance	$\overline{OE}$ = V_{CC}				15		15	
C_{PD}	Power dissipation capacitance (Note 3)				57				

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Latch enable pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D setup time with respect to $\overline{LE}$		2.0	75			90		ns
			4.5	15			18		
			6.0	13			16		
t_h	D hold time with respect to $\overline{LE}$		2.0	50			60		ns
			4.5	10			12		
			6.0	9			11		

Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open ,
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM