

# MITSUBISHI LSIs M5M5256CP,FP,KP,VP,RV-85LL,-85XL, -10LL,-10XL

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

## DESCRIPTION

This M5M5256CP,FP,KP,VP,RV is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

Especially the M5M5256CVP,RV are packaged in a 28-pin thin small outline package. Two types of devices are available, M5M5256CVP (normal lead bend type package) and M5M5256CRV (reverse lead bend type package). Using both type of devices, it becomes very easy to design a printed circuit board.

## FEATURES

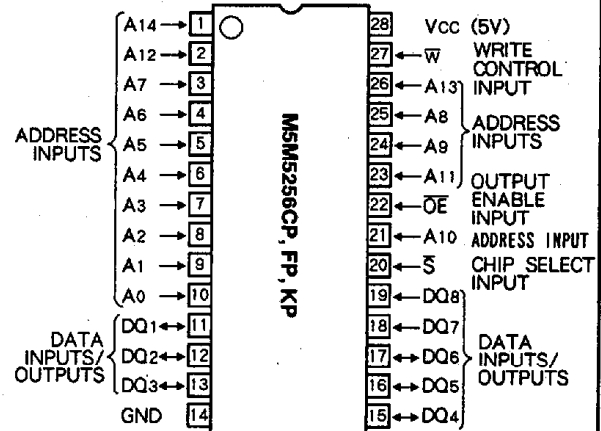
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256CP, FP, KP, VP, RV-85LL M5M5256CP, FP, KP, VP, RV-10LL	85ns 100ns	50mA (V <sub>CC</sub> =5.5V)	20 μA (V <sub>CC</sub> = 5.5V)
M5M5256CP, FP, KP, VP, RV-85XL M5M5256CP, FP, KP, VP, RV-10XL	85ns 100ns		5 μA (V <sub>CC</sub> = 5.5V) 0.05 μA (V <sub>CC</sub> = 3V, typ)

- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible: All inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expansion by  $\bar{S}$
- $\bar{OE}$  prevents data contention in the I/O bus
- Common data I/O
- Low stand-by current..... 0.05 μA (typ)
- Package
  - M5M5256CP..... 28 pin 600 mil DIP
  - M5M5256CKP..... 28 pin 300 mil DIP
  - M5M5256CFP..... 28 pin 450 mil SOP
  - M5M5256CVP,RV..... 28pin 8 × 13.4mm<sup>2</sup> TSOP

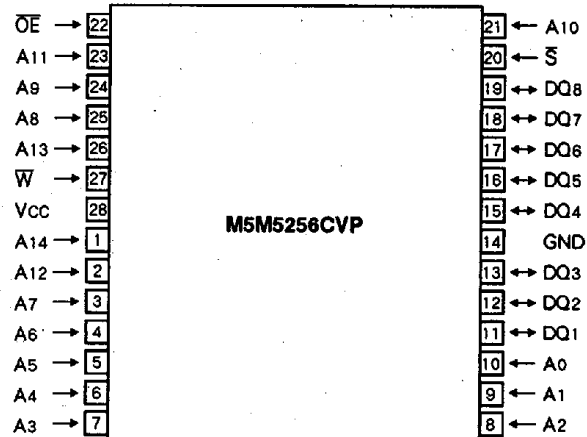
## APPLICATION

Small capacity memory units

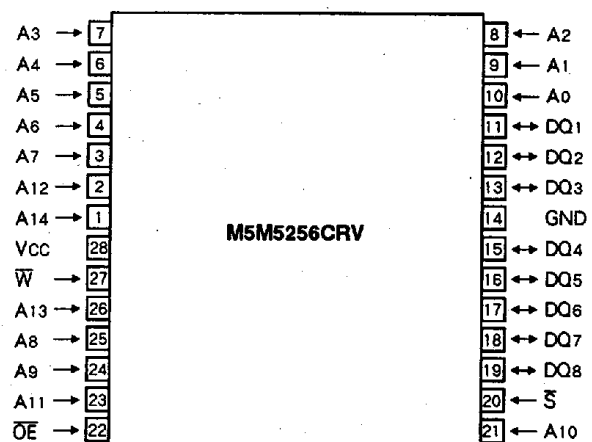
## PIN CONFIGURATION (TOP VIEW)



28P4 (P)  
Outline 28P2W-C (FP)  
28P4Y (KP)



Outline 28P2C-A



Outline 28P2C-B

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# M5M5256CP,FP,KP,VP,RV-85LL,-85XL,-10LL,-10XL

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

## FUNCTION

The operation mode of the M5M5256CP,FP,KP,VP,RV is determined by a combination of the device control inputs  $\bar{S}$ ,  $\bar{W}$  and  $\bar{OE}$ . Each mode is summarized in the function table.

A write cycle is executed whenever the low level  $\bar{W}$  overlaps with the low level  $\bar{S}$ . The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of  $\bar{W}$ ,  $\bar{S}$ , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable  $\bar{OE}$  directly controls the output stage. Setting the  $\bar{OE}$  at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

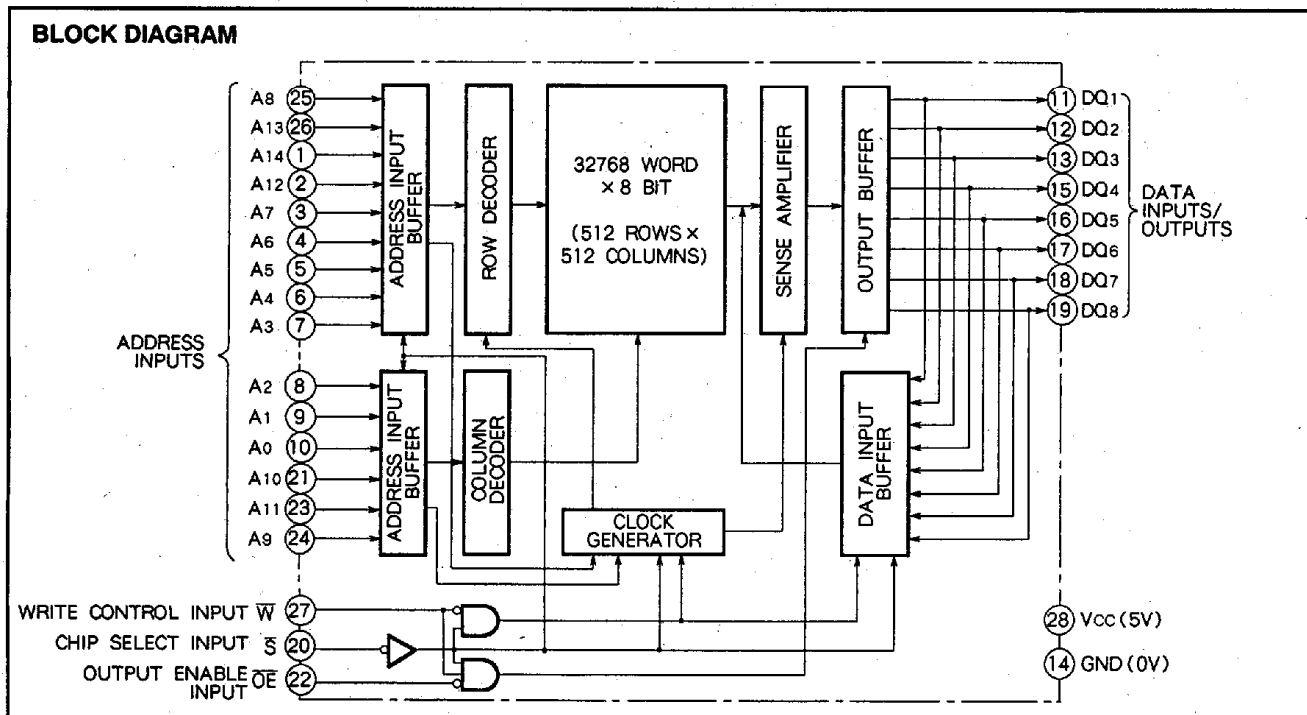
A read cycle is executed by setting  $\bar{W}$  at a high level and  $\bar{OE}$  at a low level while  $\bar{S}$  are in an active state.

When setting  $\bar{S}$  at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by  $\bar{S}$ . The power supply current is reduced as low as the stand-by current which is specified as  $I_{CC3}$  or  $I_{CC4}$ , and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

## FUNCTION TABLE

$\bar{S}$	$\bar{W}$	$\bar{OE}$	Mode	DQ	$I_{CC}$
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	$D_{in}$	Active
L	H	L	Read	$D_{out}$	Active
L	H	H		High-impedance	Active

## BLOCK DIAGRAM



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## M5M5256CP,FP, KP, VP, RV-85LL, -85XL, -10LL, -10XL

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## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage	With respect to GND	-0.3~7	V
V <sub>I</sub>	Input voltage		-0.3*~V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output voltage		0~V <sub>CC</sub>	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	700	mW
T <sub>opr</sub>	Operating temperature		0~70	°C
T <sub>stg</sub>	Storage temperature		-65~150	°C

\* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>CC</sub> = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage		2.2		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage		-0.3*		0.8	V
V <sub>OH1</sub>	High-level output voltage 1	I <sub>OH</sub> = -1mA	2.4			V
V <sub>OH2</sub>	High-level output voltage 2	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> -0.5			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2mA			0.4	V
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = 0~V <sub>CC</sub>			±1	μA
I <sub>O</sub>	Output leakage current	$\bar{S} = V_{IH}$ or $\overline{OE} = V_{IH}$ , V <sub>I/O</sub> = 0~V <sub>CC</sub>			±1	μA
I <sub>CC1</sub>	Active supply current (AC, MOS level)	$\bar{S} \leq 0.2V$ Other inputs ≤ 0.2V or ≥ V <sub>CC</sub> - 0.2V Output open	Min.cycle	30	45	mA
			1MHz	4	8	
I <sub>CC2</sub>	Active supply current (AC, TTL level)	$\bar{S} = V_{IL}$ Other inputs = V <sub>IL</sub> or V <sub>IH</sub> Output open	Min.cycle	35	50	mA
			1MHz	5	10	
I <sub>CC3</sub>	Stand-by supply current	$\bar{S} \geq V_{CC} - 0.2V$ Other inputs = 0~V <sub>CC</sub>	-LL		20	μA
			-XL	0.1	5	
I <sub>CC4</sub>	Stand-by supply current	$\bar{S} = V_{IH}$ , Other inputs = 0~V <sub>CC</sub>			3	mA

\* -3.0V in case of AC (Pulse width 30ns)

CAPACITANCE (T<sub>a</sub> = 0~70°C, V<sub>CC</sub> = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>I</sub>	Input capacitance (T <sub>a</sub> = 25°C)	V <sub>I</sub> = GND, V <sub>I</sub> = 25mVrms, f = 1MHz			6	pF
C <sub>O</sub>	Output capacitance (T <sub>a</sub> = 25°C)	V <sub>O</sub> = GND, V <sub>O</sub> = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into IC is indicated as positive.(no mark)

2. Typical value is V<sub>CC</sub> = 5V, T<sub>a</sub> = 25°C.3. C<sub>I</sub>, C<sub>O</sub> are periodically sampled and are not 100% tested.

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### AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, unless otherwise noted)

#### (1) MEASUREMENT CONDITIONS

Input pulse level.....V<sub>IH</sub> = 2.4V, V<sub>IL</sub> = 0.6V

Input rise and fall time .....5ns

Reference level.....V<sub>OH</sub> = V<sub>OL</sub> = 1.5V

Transition is measured ± 500mV from steady state voltage.(for t<sub>en</sub>, t<sub>dis</sub>)

Output loads.....Fig.1. C<sub>L</sub> = 100pF

C<sub>L</sub> = 5pF (for t<sub>en</sub>, t<sub>dis</sub>)

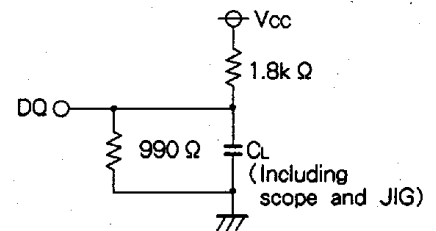


Fig.1 Output load

#### (2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M5256C-85LL M5M5256C-85XL			M5M5256C-10LL M5M5256C-10XL			
		Min	Typ	Max	Min	Typ	Max	
t <sub>CR</sub>	Read cycle time	85			100			ns
t <sub>a(A)</sub>	Address access time			85			100	ns
t <sub>a(S)</sub>	Chip select access time			85			100	ns
t <sub>a(OE)</sub>	Output enable access time			45			50	ns
t <sub>dis(S)</sub>	Output disable time after $\bar{S}$ high			30			35	ns
t <sub>dis(OE)</sub>	Output disable time after $\bar{OE}$ high			30			35	ns
t <sub>en(S)</sub>	Output enable time after $\bar{S}$ low	10			10			ns
t <sub>en(OE)</sub>	Output enable time after $\bar{OE}$ low	10			10			ns
t <sub>v(A)</sub>	Data valid time after address	20			20			ns

#### (3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5256C-85LL M5M5256C-85XL			M5M5256C-10LL M5M5256C-10XL			
		Min	Typ	Max	Min	Typ	Max	
t <sub>cw</sub>	Write cycle time	85			100			ns
t <sub>w(W)</sub>	Write pulse width	60			70			ns
t <sub>su(A)</sub>	Address set up time	0			0			ns
t <sub>su(A-WH)</sub>	Address set up time with respect to $\bar{W}$ high	70			80			ns
t <sub>su(S)</sub>	Chip select set up time	70			80			ns
t <sub>su(D)</sub>	Data set up time	30			35			ns
t <sub>h(D)</sub>	Data hold time	0			0			ns
t <sub>rec(W)</sub>	Write recovery time	0			0			ns
t <sub>dis(W)</sub>	Output disable time after $\bar{W}$ low			30			35	ns
t <sub>dis(OE)</sub>	Output disable time after $\bar{OE}$ high			30			35	ns
t <sub>en(W)</sub>	Output enable time after $\bar{W}$ high	10			10			ns
t <sub>en(OE)</sub>	Output enable time after $\bar{OE}$ low	10			10			ns

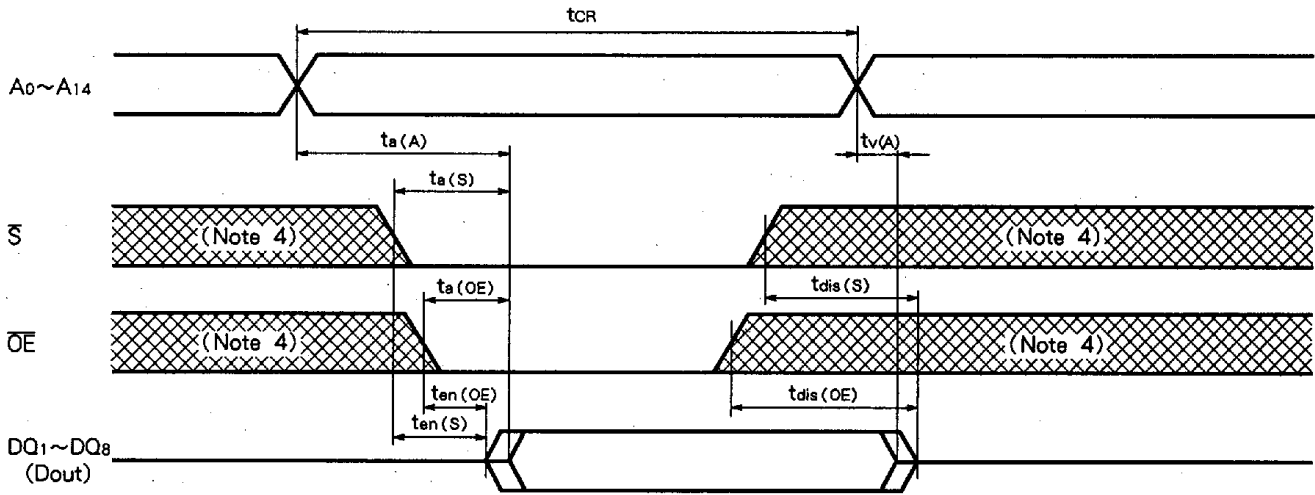
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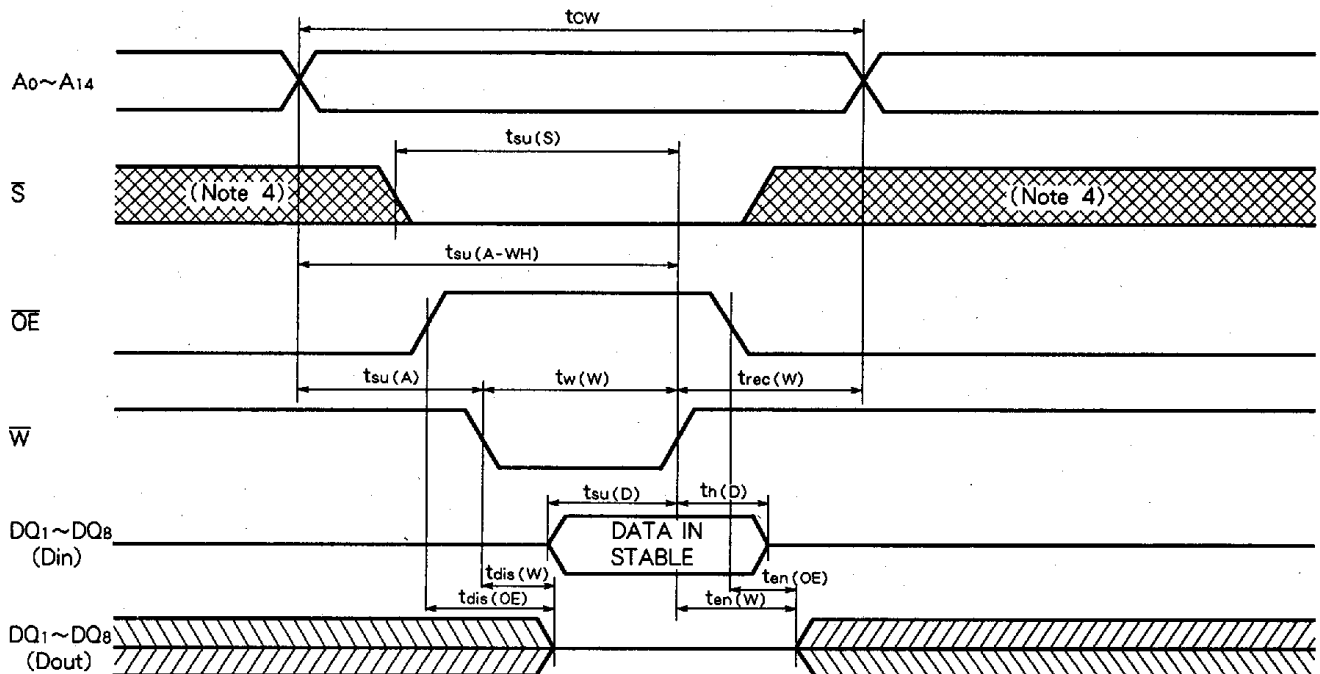
(4) TIMING DIAGRAMS

Read cycle



$\bar{W}$  = "H" level

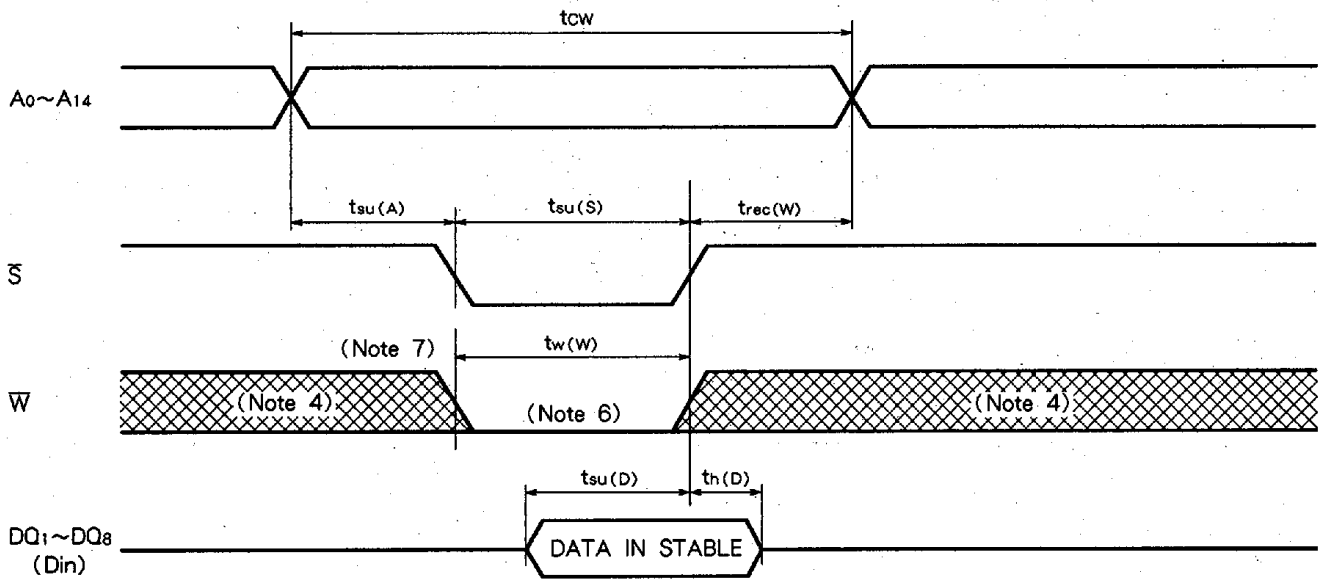
Write cycle ( $\bar{W}$  control mode)



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Write cycle ( $\bar{S}$  control mode)



Note 4. Hatching indicates the state is don't care.

5. Writing is executed in overlap of  $\bar{S}$  and  $\bar{W}$  low.

6. If  $\bar{W}$  goes low simultaneously with or prior to  $\bar{S}$ , the output remains in the high-impedance state.

7. Don't apply inverted phase signal externally when  $DQ$  pin is in output mode.

8.  $t_{en}$ ,  $t_{dis}$  are periodically sampled and are not 100% tested.

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**POWER DOWN CHARACTERISTICS**

**(1) ELECTRICAL CHARACTERISTICS** ( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_I(\bar{S})$	Chip select input $\bar{S}$	$2.2V \leq V_{CC(PD)}$	2.2			V
		$2V \leq V_{CC(PD)} \leq 2.2V$		$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3V$ Other inputs = 3V	-LL		10*	$\mu A$
			-XL		0.05	2**

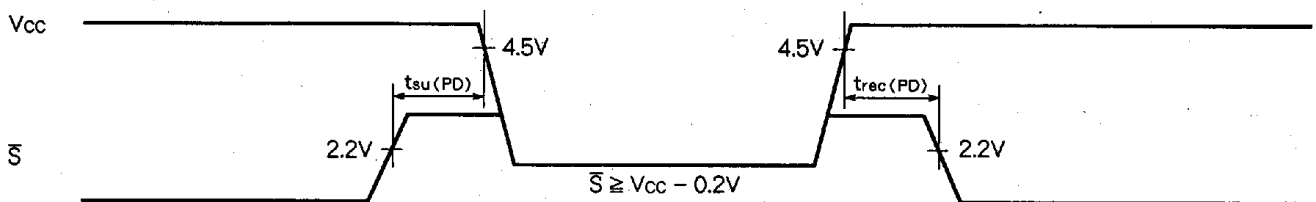
\*  $T_a = 25^\circ\text{C}$ ,  $I_{CC(PD)} = 1 \mu A$   
 \*\*  $T_a = 25^\circ\text{C}$ ,  $I_{CC(PD)} = 0.2 \mu A$

**(2) TIMING REQUIREMENTS** ( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		tCR			ns

**(3) POWER DOWN CHARACTERISTICS**

$\bar{S}$  control mode



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