M5M5255BP, BFP, BKP-70,-85,-10,-12,-70L, -85L,-10L,-12L,-70LL,-85LL,-10LL,-12LL

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M5255BP, BFP, BKP is a 262144-bit CMOS static RAM organized as 32768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM.

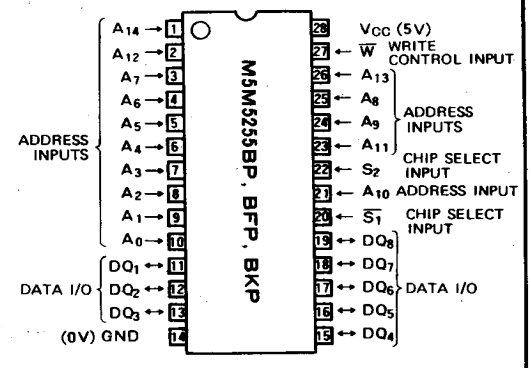
The M5M5255BP, BFP, BKP provides two chip select input ($\overline{S_1}$, S_2). It is ideal for battery back up application.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5255BP, BFP, BKP-70 M5M5255BP, BFP, BKP-85 M5M5255BP, BFP, BKP-10 M5M5255BP, BFP, BKP-12	70ns 85ns 100ns 120ns	70mA	2 mA
M5M5255BP, BFP, BKP-70L M5M5255BP, BFP, BKP-85L M5M5255BP, BFP, BKP-10L M5M5255BP, BFP, BKP-12L	70ns 85ns 100ns 120ns		100μA (V_{CC}=5.5V) 50μA (V_{CC}=3.0V)
M5M5255BP, BFP, BKP-70LL M5M5255BP, BFP, BKP-85LL M5M5255BP, BFP, BKP-10LL M5M5255BP, BFP, BKP-12LL	70ns 85ns 100ns 120ns		20μA (V_{CC}=5.5V) 10μA (V_{CC}=3.0V)

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S_1}$, S_2
- Common Data I/O
- Package
  - M5M5255BP . . . . . 28 Pin 600 mil DIP
  - M5M5255BKP . . . . . 28 Pin 300 mil DIP
  - M5M5255BFP . 28 Pin Small Outline Package (SOP)

PIN CONFIGURATION (TOP VIEW)

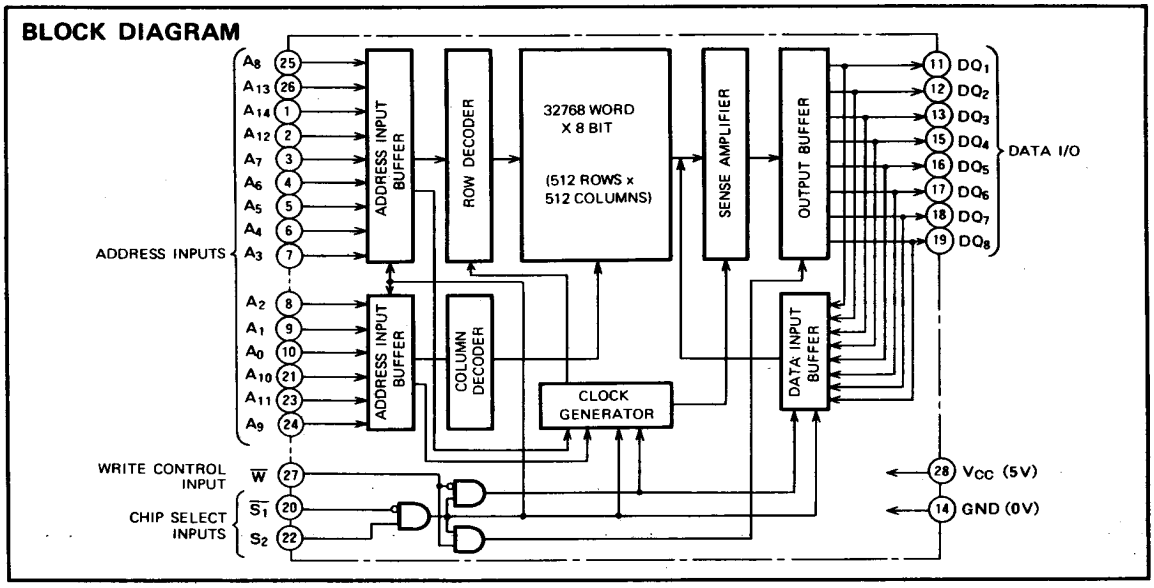


Outline 28P4 (BP)
28P2W-C (BFP)
28P4Y (BKP)

APPLICATION

Small Capacity Memory Units.

BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M5255BP, BFP, BKP is determined by a combination of the device control inputs $\overline{S_1}$, S_2, and $\overline{W}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained.

A read cycle is excuted by setting $\overline{W}$ at a high level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L, S_2 = H)

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S_1}$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	Mode	DQ	I_{CC}
H	X	X	Non selection	High-impedance	Standby
X	L	X	Non selection	High-impedance	Standby
L	H	L	Write	D_{IN}	Active
L	H	H	Read	D_{OUT}	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3 ~ 7	V
V_I	Input voltage		−0.3 ~ V_{CC}+0.3	V
V_O	Output voltage		0 ~ V_{CC}	V
T_{opr}	Operating temperature	Ta = 25°C	0 ~ 70	°C
T_{stg}	Storage temperature		−65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			−0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = −1mA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2 mA				0.4	V
I_I	Input current	V_I = 0 ~ V_{CC}				±1	μA
I_{OZH}	High level output current in off-state	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL}				1	μA
I_{OZL}	Low level output current in off-state	$V_{I/O}$ = 0 − V_{CC}				−1	μA
I_{CC1}	Active supply current (AC. MOS level)	$\overline{S_1}$ < 0.2, S_2 > V_{CC} − 0.2 Output open Other inputs < 0.2 or > V_{CC} − 0.2 Min. cycle			30	65	mA
I_{CC2}	Active supply current (AC. TTL level)	$\overline{S_1}$ = V_{IL} or S_2 = V_{IH} Output open Other inputs = V_{IL} or V_{IH} Min. cycle			35	70	mA
I_{CC3}	Stand by supply current	$S_2 \geqq$ 0.2V, Other inputs = 0 ~ V_{CC}	BP, BFP, BKP			2	mA
			BP, BFP, BKP-L			100	μA
			BP, BFP, BKP-LL			20	μA
I_{CC4}	Stand by supply current	S_2 = V_{IL}, $\overline{S_1}$ = V_{IH}, Other inputs = 0 ~ V_{CC}				3	mA
C_i	Input capacitance (T_a = 25°C)	V_I = GND, V_I = 25mVrms, f = 1MHz				6	pF
C_o	Output capacitance (T_a = 25°C)	V_O = GND, V_O = 25mVrms, f = 1MHz				8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC} = 5V, T_a = 25°C

MITSUBISHI ELECTRIC

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits												Unit
		M5M5255-70 M5M5255-70L M5M5255-70LL			M5M5255-85 M5M5255-85L M5M5255-85LL			M5M5255-10 M5M5255-10L M5M5255-10LL			M5M5255-12 M5M5255-12L M5M5255-12LL			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	70			85			100			120			ns
$t_{a(A)}$	Address access time			70			85			100			120	ns
$t_{a(S_1)}$	Chip select 1 access time			70			85			100			120	ns
$t_{a(S_2)}$	Chip select 2 access time			70			85			100			120	ns
$t_{dis(S_1)}$	Output disable time after $\overline{S_1}$ high			30			30			35			40	ns
$t_{dis(S_2)}$	Output disable time after S_2 low			30			30			35			40	ns
$t_{en(S_1)}$	Output enable time after $\overline{S_1}$ low	5			10			10			10			ns
$t_{en(S_2)}$	Output enable time after S_2 high	5			10			10			10			ns
$t_{v(A)}$	Data valid time after address change	20			20			20			20			ns

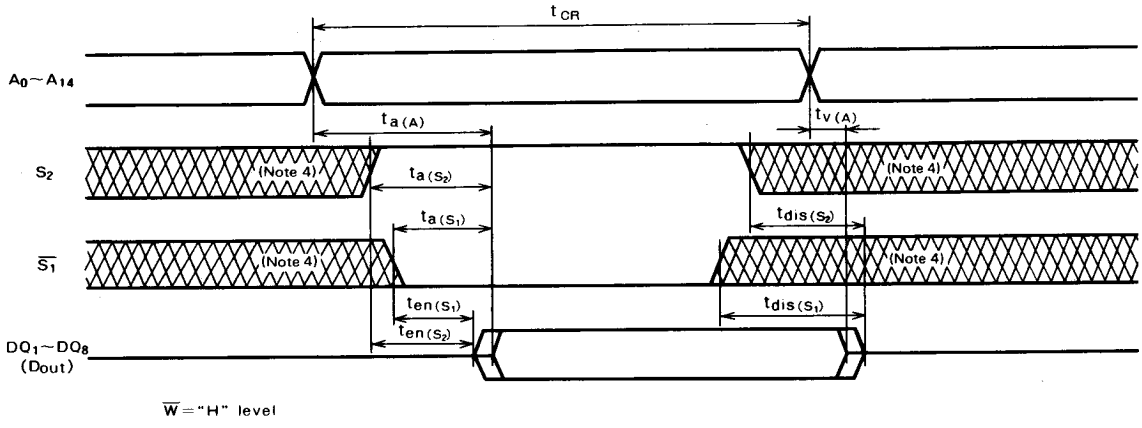
TIMING REQUIREMENTS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits												Unit
		M5M5255-70 M5M5255-70L M5M5255-70LL			M5M5255-85 M5M5255-85L M5M5255-85LL			M5M5255-10 M5M5255-10L M5M5255-10LL			M5M5255-12 M5M5255-12L M5M5255-12LL			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	70			85			100			120			ns
$t_{w(W)}$	Write pulse width	55			60			60			70			ns
$t_{su(A)}$	Address set up time	0			0			0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	65			75			80			85			ns
$t_{su(S_1)}$	Chip select set up time	65			75			80			85			ns
$t_{su(S_2)}$	Chip select set up time	65			75			80			85			ns
$t_{su(D)}$	Data set up time	30			35			35			40			ns
$t_{h(D)}$	Data hold time	0			0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			25			30			35			40	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			10			10			ns

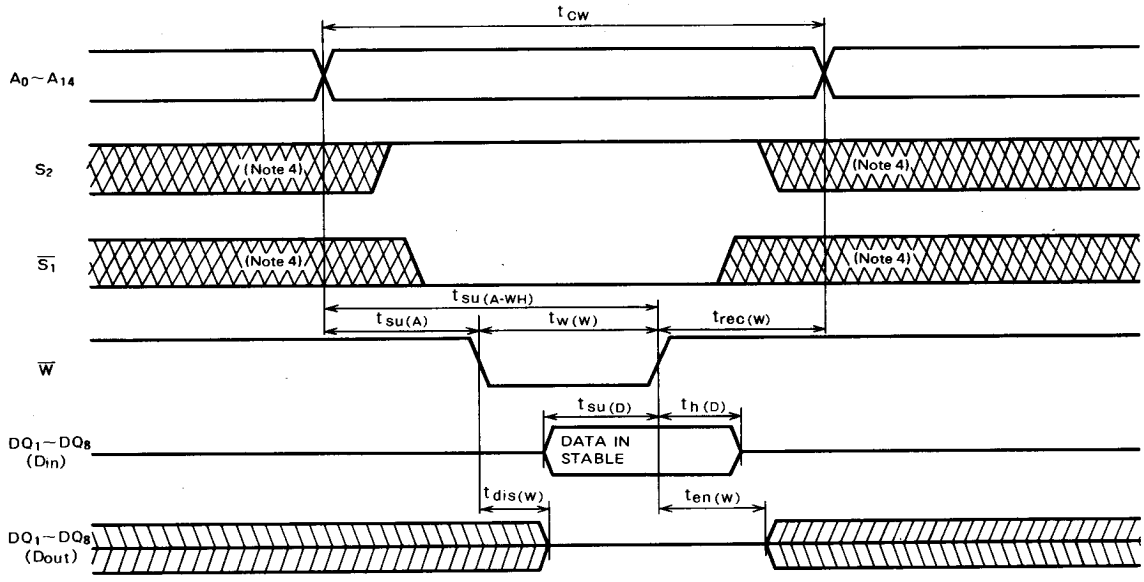
TIMING DIAGRAM

Read cycle

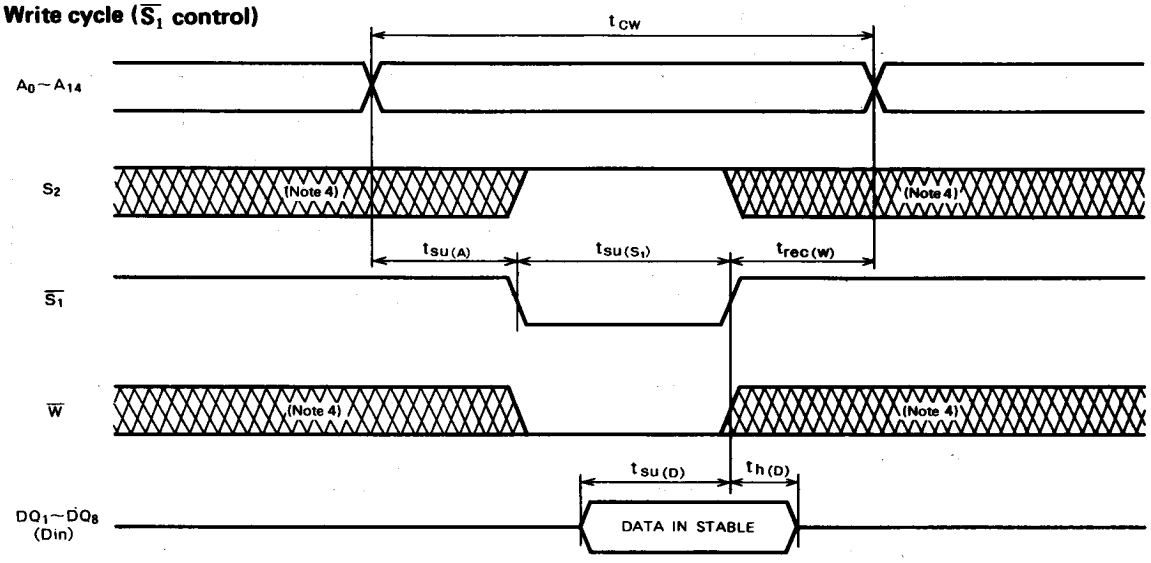


$\overline{W}$ = "H" level

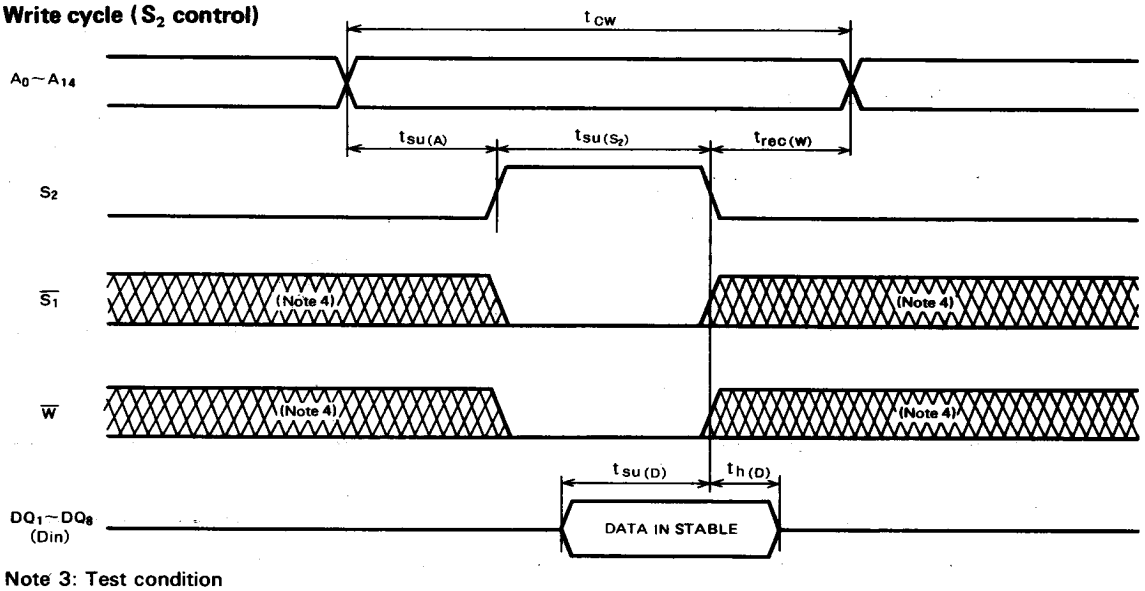
Write cycle ($\overline{W}$ control)



Write cycle ($\overline{S_1}$ control)



Write cycle (S_2 control)



Note 3: Test condition

Input pulse level .... V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall time 10ns
Reference level ..... V_{OH} = V_{OL} = 1.5V
Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})
Output loads ..... Fig. 1, C_L = 100pF (BP, BFP, BKP-85, -10, -12, -85L, -10L, -12L, -85LL, -10LL, -12LL)
C_L = 30pF (BP, BFP, BKP-70, -70L, -70LL)
C_L = 5pF (for t_{en}, t_{dis})

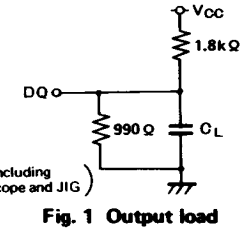


Fig. 1 Output load

Note 4: Hatching indicates the state is don't care.
5: Writing is executed while S_2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S_1}$ low or S_2 high, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S_1})}$	Chip select input $\overline{S_1}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$V_{I(S_2)}$	Chip select input S_2	4.5V ≦ $V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$ < 4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, Other inputs = 3V	BP, BFP, BKP			2	mA
			BP, BFP, BKP-L			50	μA
			BP, BFP, BKP-LL			10*	μA

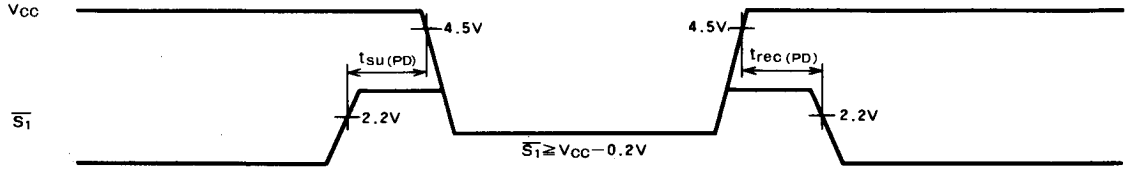
* T_a = 25°C, $I_{CC(PD)}$ = 1μA

TIMING REQUIREMENTS (T_a = 0 ~ 70°C, unless otherwise noted)

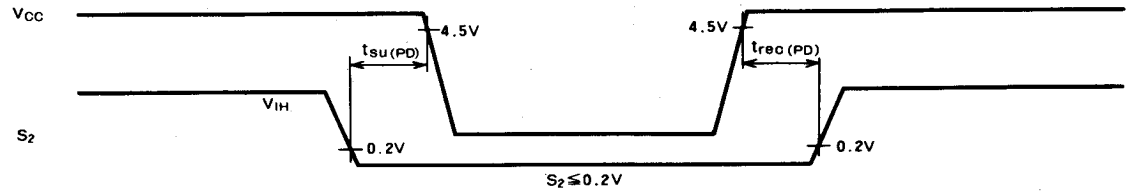
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control



S_2 control



MITSUBISHI ELECTRIC