M5M51008AFP,VP,RV-85VL,-10VL, -85VLL,-10VLL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008AFP, VP, RV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51008AVP, RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD). Two types of devices are available. M5M51008AVP(normal lead bend type package), M5M51008ARV(reverse lead bend type package). Using both types of devices, it becames very easy to design a printed circuit board.

FEATURES

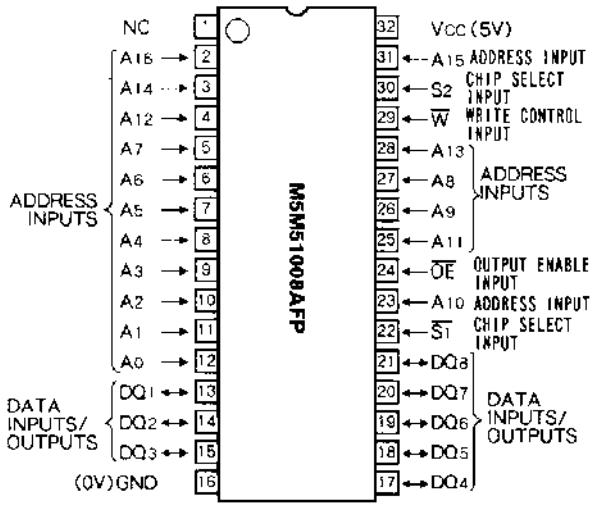
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51008AFP, VP, RV-85VL M5M51008AFP, VP, RV-10VL	85ns 100ns	15mA (1MHz)	55 μA
M5M51008AFP, VP, RV-85VLL M5M51008AFP, VP, RV-10VLL	85ns 100ns		11 μA

- Single +3.3V power supply
- Low stand-by current 0.3 μA(typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S1}$, S2
- Data hold on +2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  M5M51008AFP ····· 32pin 525 mil SOP
  M5M51008AVP, RV ····· 32pin 8 × 20mm² TSOP

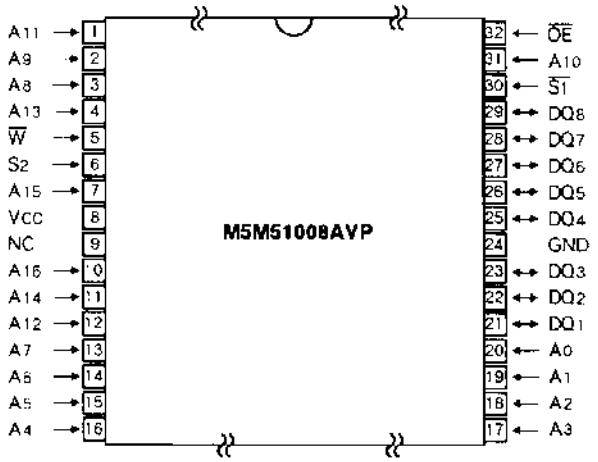
APPLICATION

Small capacity memory units

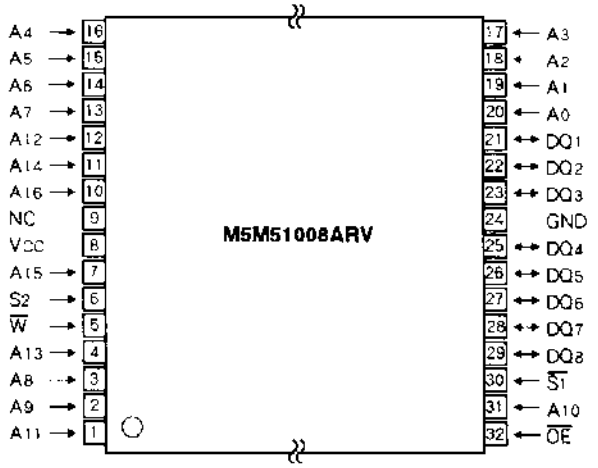
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A(FP)



Outline 32P3H-E(VP)



Outline 32P3H-F(RV)

NC : NO CONNECTION

M5M51008AFP, VP, RV-85VL, -85VLL : Under development

MITSUBISHI ELECTRIC

M5M51008AFP,VP,RV-85VL,-10VL,-85VLL,-10VLL

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FUNCTION

The operation mode of the M5M51008A series are determined by a combination of the device control inputs $\overline{S1}$, S2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S1}$ and the high level S2. The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S1}$ or S2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output state. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

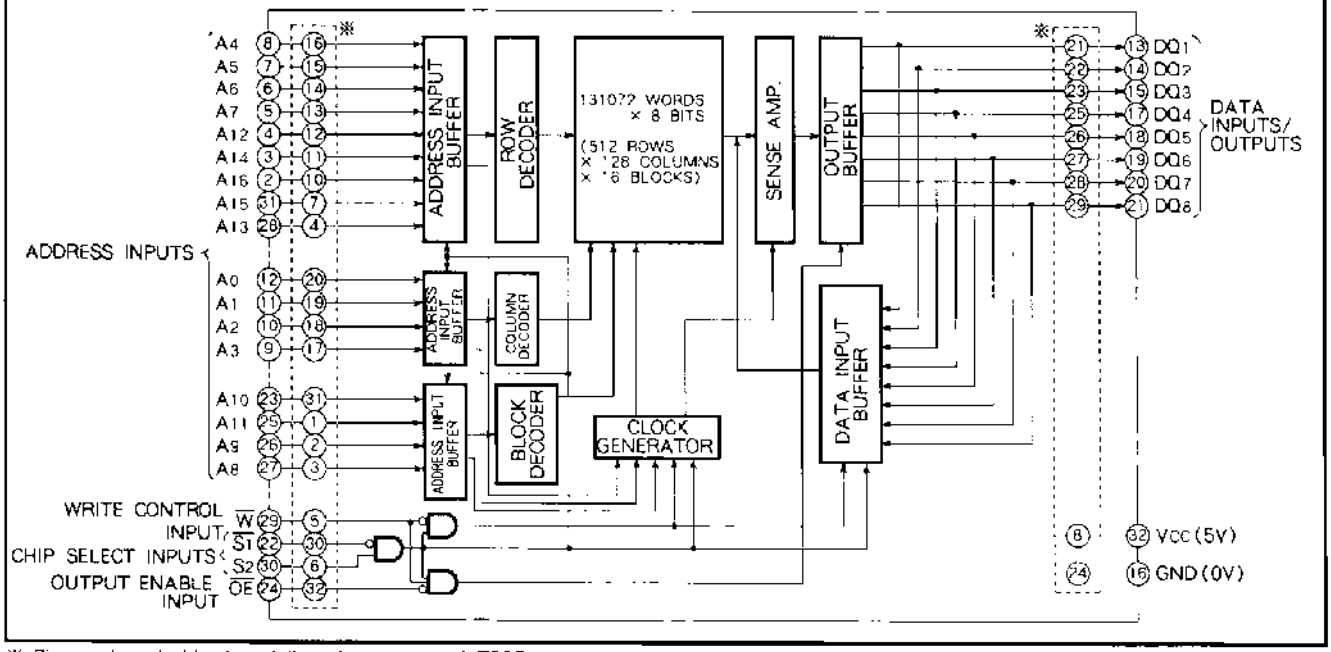
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S1}$ and S2 are in an active state ($\overline{S1}$ = L, S2 = H)

When setting $\overline{S1}$ at a high level or S2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S1}$ and S2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	S2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	D_{in}	Active
L	H	H	L	Read	D_{out}	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



※ Pin numbers inside dotted line show those of TSOP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage	With respect to GND	− 0.3 ~V_{CC} + 0.3	V
V_O	Output voltage	With respect to GND	0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 3.3 ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage			− 0.3		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = − 1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = − 0.1mA		Vcc−0.5			V
V_{OL}	Low level outout voltage	I_{OL} = 2mA				0.4	V
I_I	Input current	V_I = 0~V_{CC}				± 1	μA
I_O	Output current in off state	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (Min cycle)	Output-open (duty 100%), $\overline{S_1}$ = V_{IL}, S_2 = V_{IH}, other inputs = V_{IH} or V_{IL}			15	30	mA
I_{CC2}	Active supply current (1MHz)	Output-open (duty 100%)			8	15	mA
I_{CC3}	Stand-by current	S_2 ≦ 0.2V or $\overline{S_1}$ ≧ Vcc − 0.2V, S_2 ≧ Vcc − 0.2V, other inputs = 0~Vcc	-VL			55	μA
			-VLL		0.3	11	μA
I_{CC4}	Stand-by current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL}, other inputs = 0~V_{CC}				0.33	mA

CAPACITANCE (Ta = 0~70℃, Vcc = 3.3 ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_i = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_o = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into an IC is positive (no mark).
2. Typical value is Vcc = 3.3V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ·····V_{IH} = 2.2V, V_{IL} = 0.4V

Input rise and fall time·····5ns

Reference level ·····V_{OH} = V_{OL} = 1.5V

Output loads ·····Fig.1, C_L = 30pF (FP, VP, RV-85VL,-10VL, -85VLL,-10VLL)

C_L = 5pF (for t_{en}, t_{dis})

Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

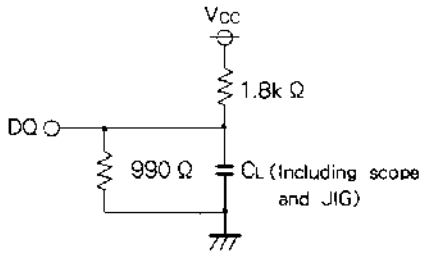


Fig. 1 Output load

(2) READ CYCLE

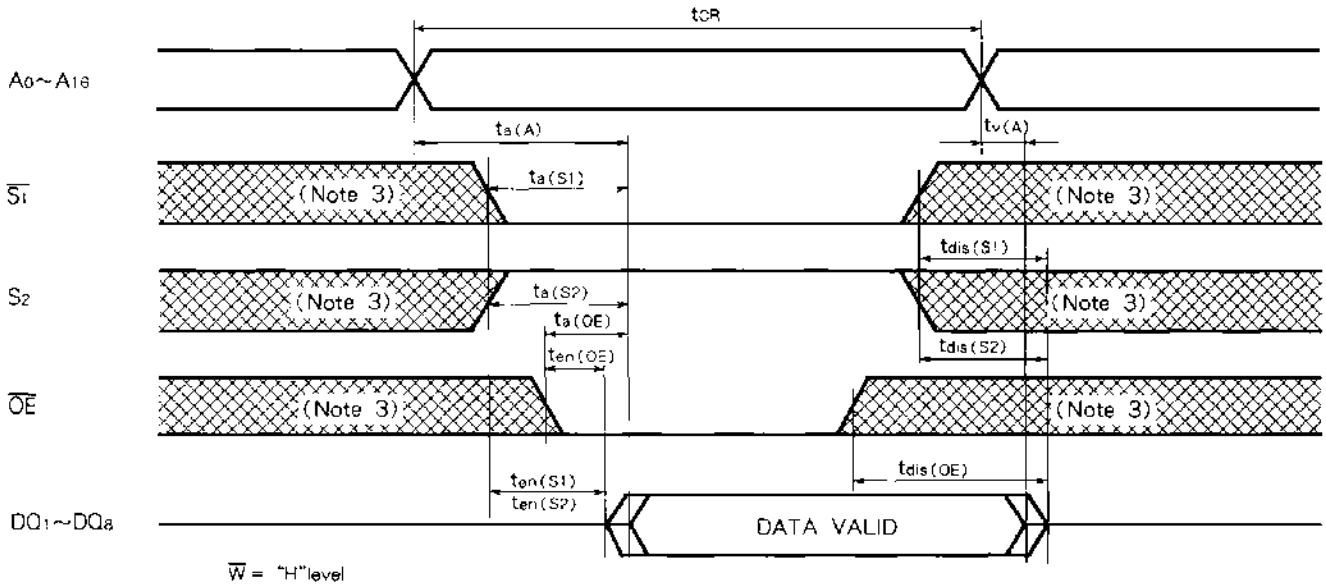
Symbol	Parameter	Limits						Unit
		M5M51008A -85VL,-85VLL			M5M51008A -10VL,-10VLL			
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	85			100			ns
$t_{a(A)}$	Address access time			85			100	ns
$t_{a(S1)}$	Chip select 1 access time			85			100	ns
$t_{a(S2)}$	Chip select 2 access time			85			100	ns
$t_{a(OE)}$	Output enable access time			45			50	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			30			35	ns
$t_{dis(S2)}$	Output disable time after S_2 low			30			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			35	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	10			10			ns
$t_{en(S2)}$	Output enable time after S_2 high	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			ns
$t_{v(A)}$	Data valid time after address	10			10			ns

(3) WRITE CYCLE

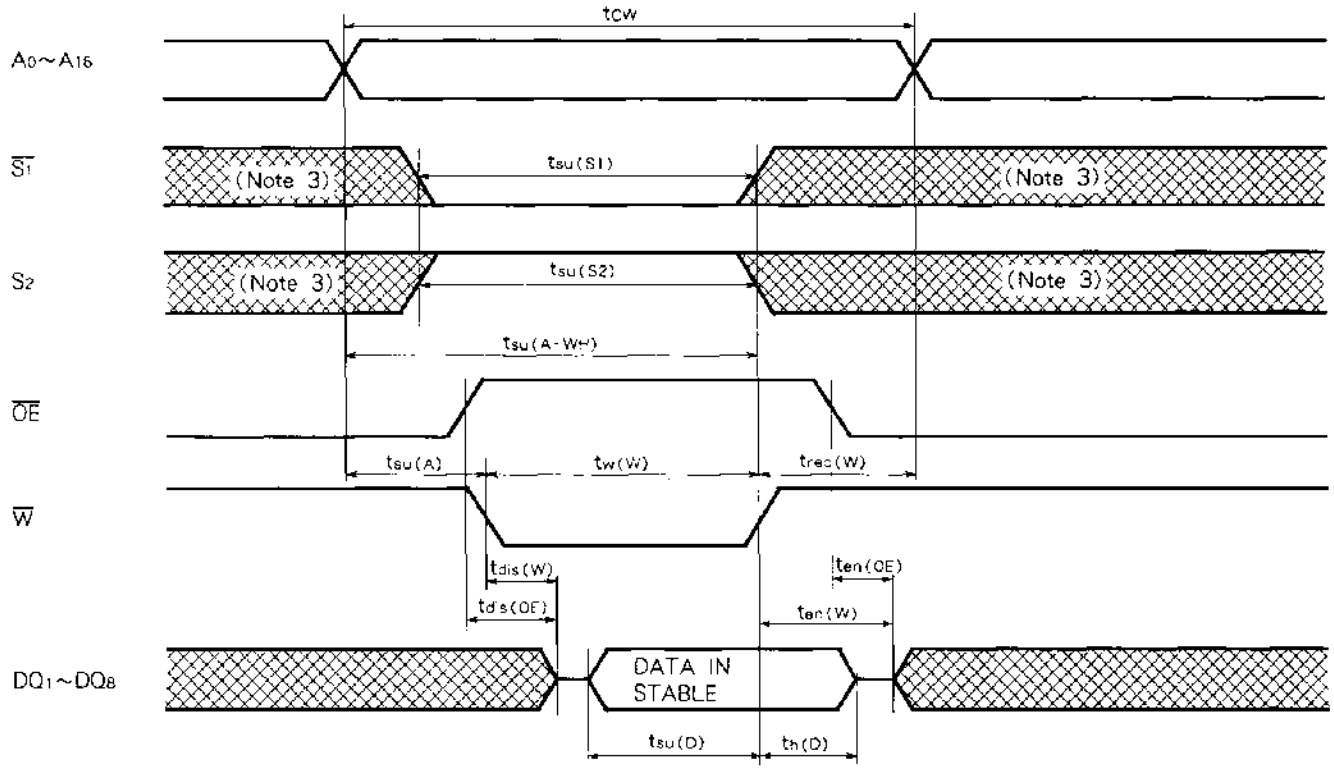
Symbol	Parameter	Limits						Unit
		M5M51008A -85VL,-85VLL			M5M51008A -10VL,-10VLL			
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	85			100			ns
$t_{w(W)}$	Write pulse width	65			75			ns
$t_{su(A)}$	Address set up time	0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$	75			85			ns
$t_{su(S1)}$	Chip select 1 set up time	75			85			ns
$t_{su(S2)}$	Chip select 2 set up time	75			85			ns
$t_{su(D)}$	Data set up time	35			40			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low			30			35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high			30			35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5			5			ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5			5			ns

(4) TIMING DIAGRAMS

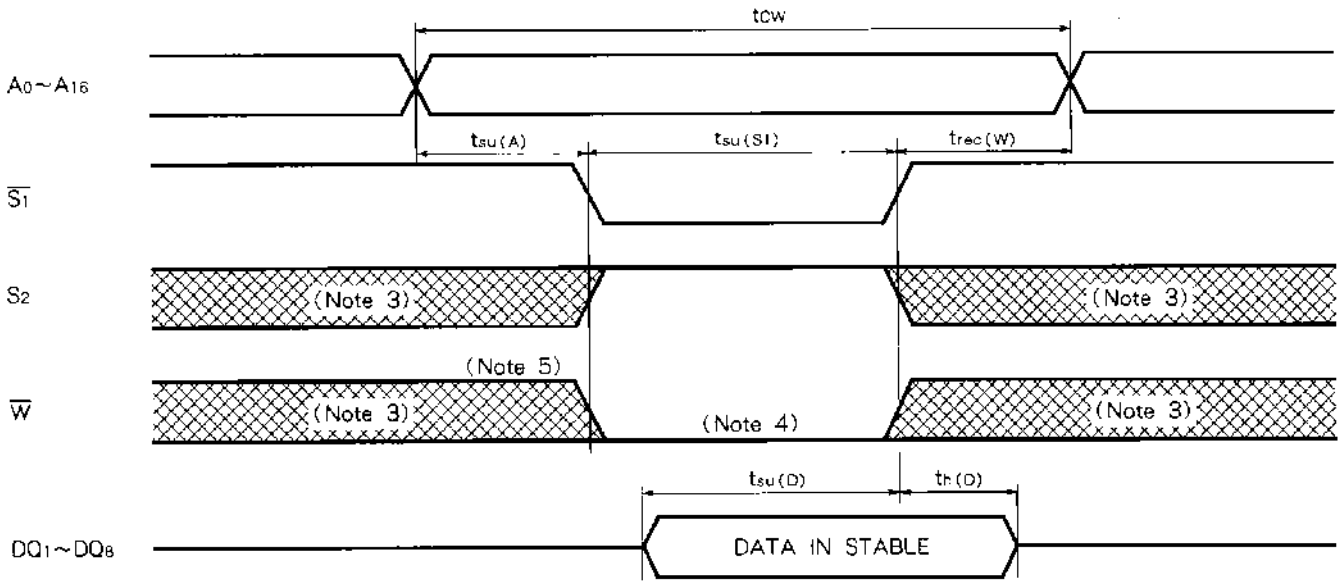
Read cycle



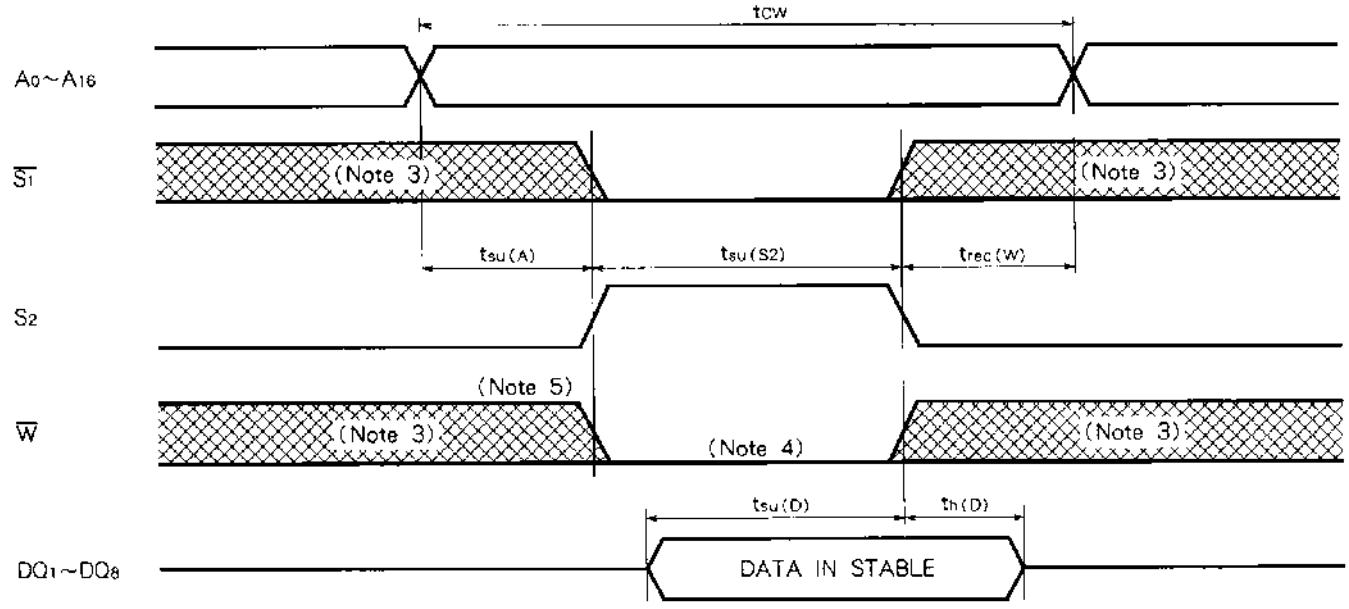
Write cycle ($\overline{W}$ control mode)



Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3. Hatching indicates the state is "don't care".
4. Writing is executed while S2 high overlaps $\overline{S1}$ and $\overline{W}$ low.
5. When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
6. Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Typ	Max	Unit
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{ST})}$	Chip select input $\overline{S_1}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V ≦ $V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$ < 4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V S_2 ≦ 0.2V or $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V	-VL			50	μA
			-VLL		0.3	10 (Note 7)	

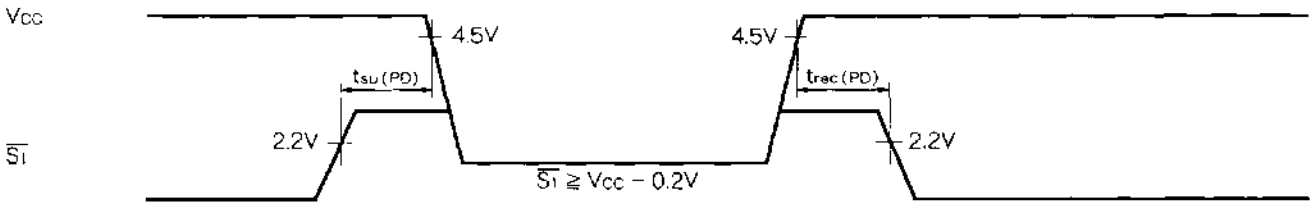
Note 7. $I_{CC(PD)}$ = 1 μA in case of T_a = 25℃.

(2) TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control mode