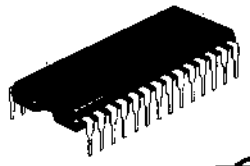


PRELIMINARY
Notice: This is not a final specification
Some parameters are subject to change

M5M51004P,J-35,-45

1M (256K x 4)

1048576-BIT(262144-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M51004 is a family of 262144-word by 4-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high-speed application. These devices operate on a single 5V supply, and are TTL compatible. They include power down feature as well.

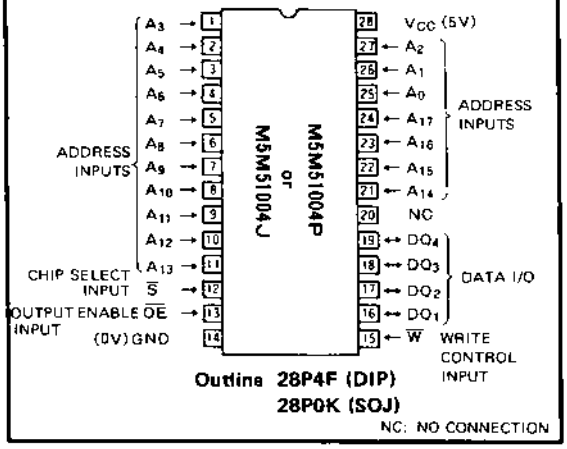
FEATURES

- Fast access time M5M51004P, J-35 . . . . . 35ns (max)
  M5M51004P, J-45 . . . . . 45ns (max)
- Low power dissipation Active . . . . . 400mW (typ)
  Stand by . . . . . 5mW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus

APPLICATION

High-speed memory systems

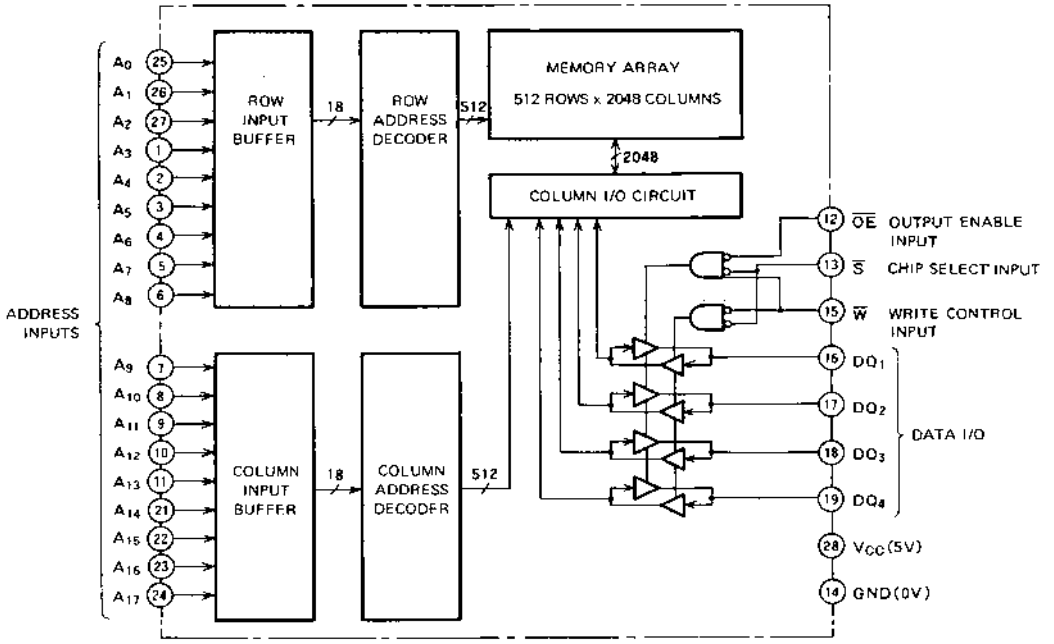
PIN CONFIGURATION (TOP VIEW)



Outline 28P4F (DIP)
28P0K (SOJ)

NC: NO CONNECTION

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M5M51004P,J-35,-45

1048576-BIT(262144-WORD BY 4-BIT) CMOS STATIC RAM

FUNCTION

A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period address signals must be stable. When $\overline{W}$ is low, the DQ terminals are maintained in the high impedance state, so it is possible to connect D and Q terminal directly.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ and $\overline{OE}$ to low if the address signals are stable, the data is available at DQ terminal.

When $\overline{S}$ is high, the chip is the non-selectable state, disabling both reading and writing. In this case, the output is in the floating (high-impedance) state, useful for OR-tie with other devices.

Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

Signal $\overline{S}$ controls the power-down features. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Not select	Hi-Z	Stand by
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H		Hi-Z	Active

Note H: V_{IH}, L: V_{IL}, X: Don't care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
P_d	Power dissipation		1	W
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		−65~+150	°C

* Pulse width ≤ 20ns, in case of DC, −0.5V

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Units
V_{IH}	High-level input voltage			2.4		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.5*		0.6	V
V_{OH}	High-level output voltage	I_{OH}=−4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL}=8mA				0.4	V
I_I	Input current	V_I=0~V_{CC}+0.3V				2	μA
I_{OZ}	Off-state output current	$V_{I(S)}$=V_{IH}, V_O=0~V_{CC}				10	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(S)}$=V_{IL}, Output open	AC (Min cycle)			120	mA
			DC		60	75	mA
I_{CC2}	Standby current	$V_{I(S)}$=V_{IH}	AC (Min cycle)			40	mA
			DC			30	mA
I_{CC3}	Stand by current	$V_{I(S)}$≧V_{SS}−0.2V, other V_I≦0.2V or V_I≧V_{CC}−0.2V			1	10	mA

* −3.0V in case of AC (Pulse width ≤ 20ns)

CAPACITANCE (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Units
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			5	pF
$C_{I/O}$	Input output capacitance	$V_{I/O}$=GND, $V_{I/O}$=25mVrms, f=1MHz			5	pF

Note 1: Current flowing into an IC is positive, out is negative

AC ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

(1) MEASUREMENT CONDITIONS

Input pulse level . . . . . V_{IH} = 3V, V_{IL} = 0V
Input rise and fall time 3ns
Input timing reference level . . . . V_{IH} = 2.4V, V_{IL} = 0.6V
Output timing reference level . . . V_{OH} = 2V, V_{OL} = 0.8V

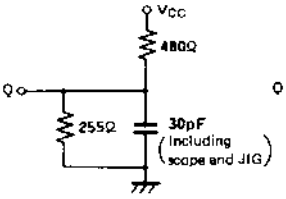


Fig. 1 Output load

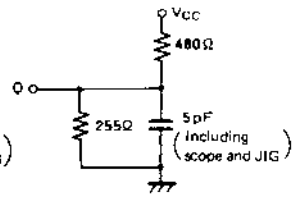


Fig. 2 Output load for ten, tdis

(2) READ CYCLE

Symbol	Parameter	Limits						Units
		M5M51004-35			M5M51004-45			
		Min	Typ	Max	Min	Typ	Max	
$t_{c(R)}$	Read cycle time	35			45			ns
$t_{a(A)}$	Address access time			35			45	ns
$t_{a(S)}$	Chip select access time			35			45	ns
$t_{a(OE)}$	Output enable access time			18			23	ns
$t_{v(A)}$	Data valid time after address	5			5			ns
$t_{en(S)}$	Chip selection to output active	5			5			ns
$t_{dis(S)}$	Output disable time from $\overline{S}$ high	0		20	0		20	ns
$t_{an(OE)}$	Output enable time after $\overline{OE}$ low	0			0			ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0		10	0		15	ns
t_{pu}	Power-up time after chip selection	0			0			ns
t_{pd}	Power-down time after chip selection			35			45	ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Units
		M5M51004-35			M5M51004-45			
		Min	Typ	Max	Min	Typ	Max	
$t_{c(W)}$	Write cycle time	35			45			ns
$t_{su(S)}$	Chip select setup time	30			35			ns
$t_{su(A)1}$	Address setup time ($\overline{W}$)	0			0			ns
$t_{su(A)2}$	Address setup time ($\overline{S}$)	0			0			ns
$t_{w(W)}$	Write pulse width	30			35			ns
$t_{rec(W)}$	Write recovery time	5			5			ns
$t_{su(D)}$	Data setup time	15			20			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{dis(W)}$	Output disable time from $\overline{W}$	0		15	0		15	ns
$t_{en(W)}$	Output enable time from $\overline{W}$	0			0			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	30			35			ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0		10	0		15	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0			0			ns

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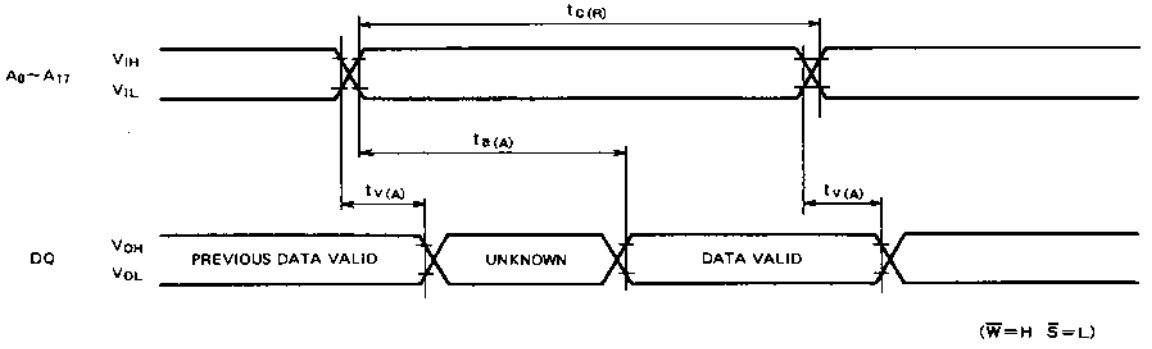
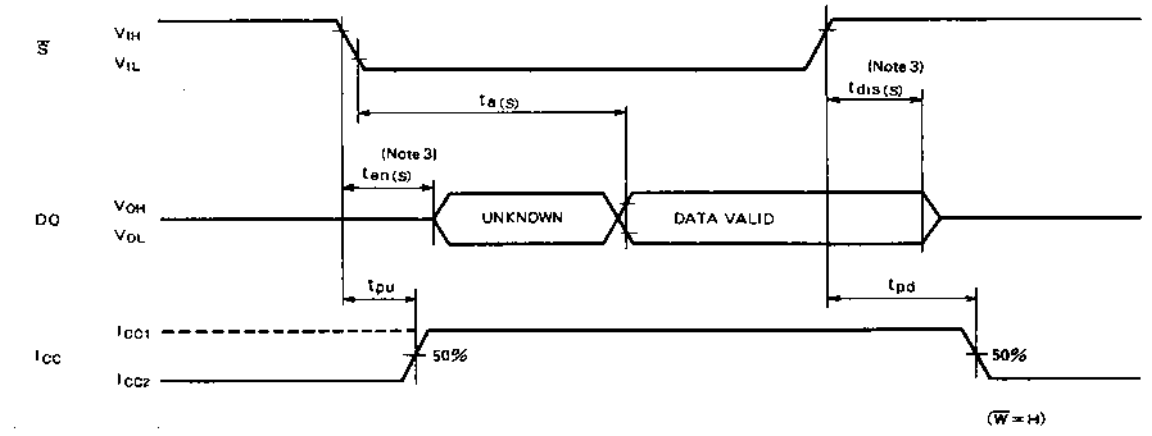
(4) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



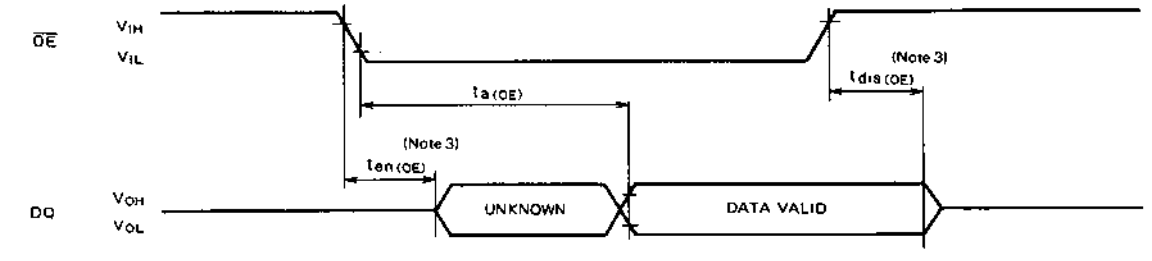
($\overline{W}$=H $\overline{S}$=L)

Read cycle 2 (Note 2)



($\overline{W}$=H)

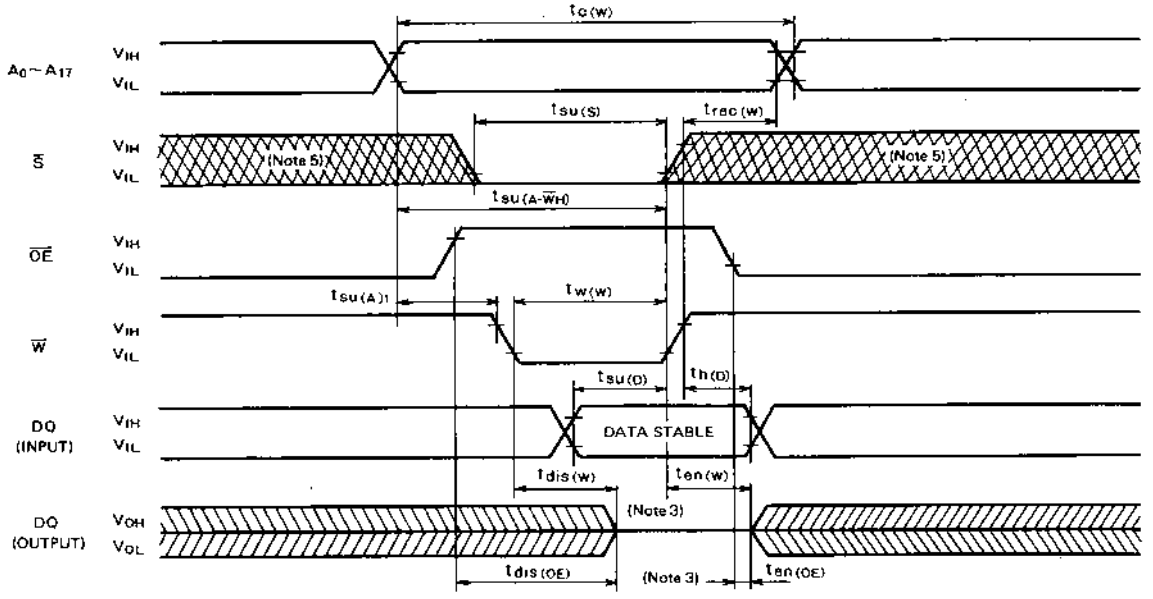
Read cycle 3 (Note 4)



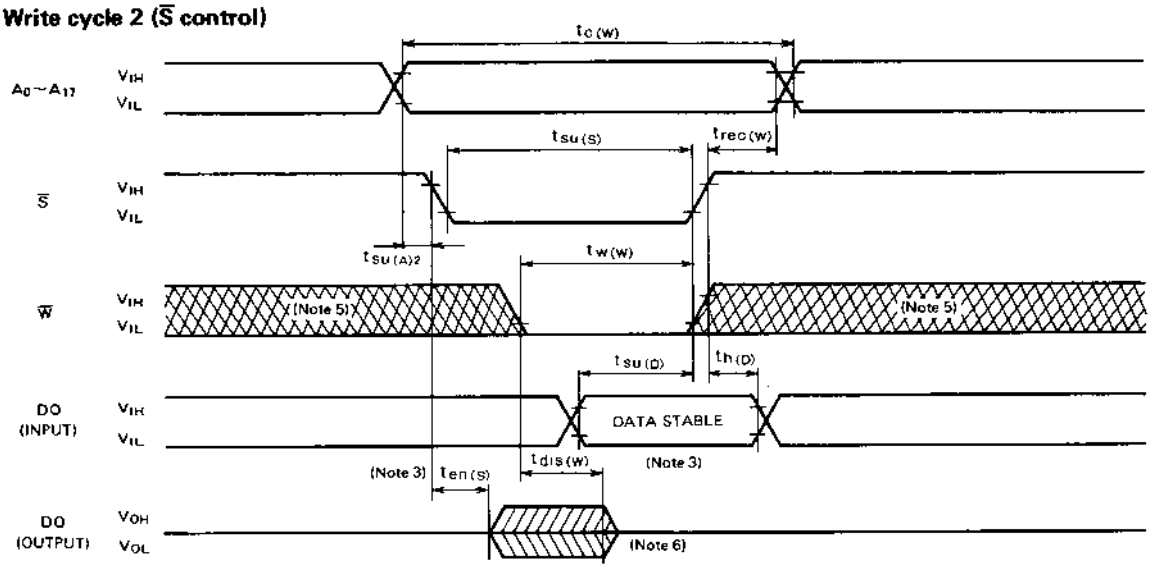
Note 2: Addresses valid prior to or coincident with $\overline{S}$ transition low.
3: Transition is measured ±500mV from steady state voltage with specified loading in Fig. 2.
4: Address and $\overline{S}$ valid prior to $\overline{OE}$ transition low by $(t_{a(A)} - t_{a(OE)})$, $(t_{a(S)} - t_{a(OE)})$.

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control)



Write cycle 2 ($\overline{S}$ control)



Note 5: Hatching indicates the states don't care.
6 When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S}$, the outputs are maintained in the high impedance.

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