

# M5M27C101P,FP,J,VP,RV-15

1048576-BIT(131072-WORD BY 8-BIT)  
CMOS ONE TIME PROGRAMMABLE ROM

### DESCRIPTION

The Mitsubishi M5M27C101P,FP,J,VP,RV-15 are high-speed 1048576 bit one time programmable read only memories. They are suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C101P,FP,J,VP,RV-15 are fabricated by N-channel double polysilicon gate for Memory and CMOS technology for peripheral circuits, and are available in 32 pin plastic packages (DIP, SOP, PLCC) and 40 pin plastic packages (TSOP).

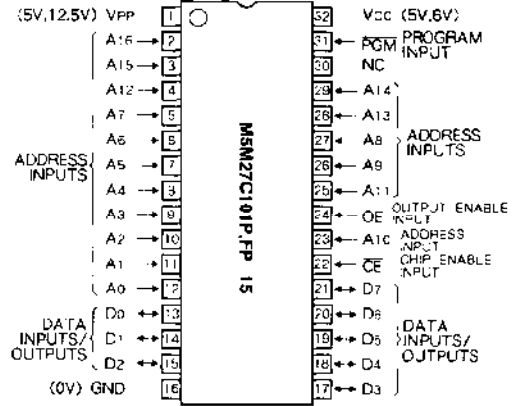
### FEATURES

- 131072 word x 8 bit organization
- Package
  - DIP.....M5M27C101P-15
  - SOP (525mil).....M5M27C101FP-15
  - PLCC.....M5M27C101J-15
  - TSOP.....M5M27C101VP-15
  - TSOP (Reverse).....M5M27C101RV-15
- Access time.....150ns (max.)
- Two line control  $\overline{OE}$ ,  $\overline{CE}$
- Low power current ( $I_{cc}$ ): Active.....50mA (max.)  
Stand-by.....1mA (max.)
- Single 5V power supply (read operation)
- Programming voltage.....12.5V
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 32 pin DIP, PLCC, Pin-compatible with 1Mbit EPROM
- Byte programming algorithm
- Page programming algorithm

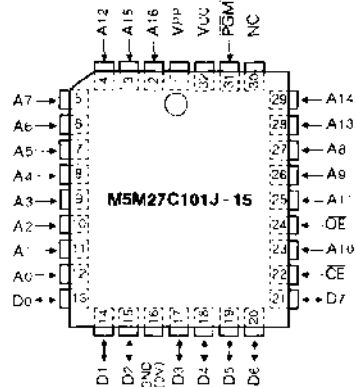
### APPLICATION

Microcomputer systems and peripheral equipment

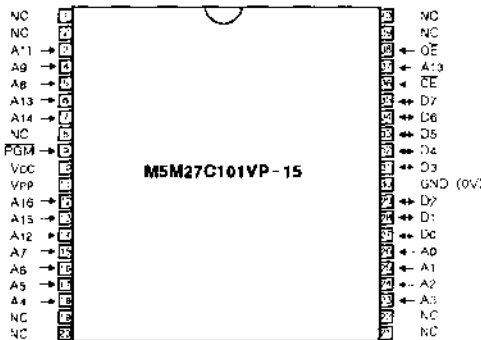
### PIN CONFIGURATION (TOP VIEW)



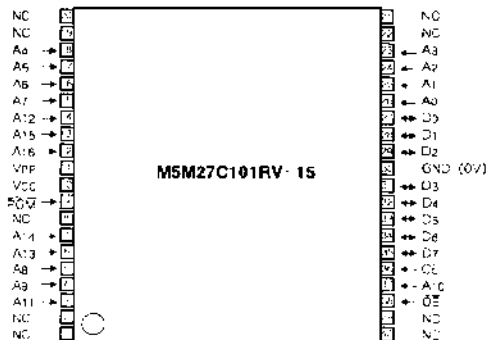
Outline 32P4 (DIP: P)  
32P2M-A (SOP: FP)



Outline 32P0 (PLCC: J)



Outline 40P3J-A (TSOP: VP)



Outline 40P3J-B (TSOP: RV: Reverse)

(Inner leads of pin no. 1-2, 19-20, 21-22, 39-40 are connected each other.)

NC: NO CONNECTION

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## FUNCTION

### Read

Set the  $\overline{CE}$  and  $\overline{OE}$  terminals to the read mode (low level). Low level input to  $\overline{CE}$  and  $\overline{OE}$  and address signals to the address inputs ( $A_0 \sim A_6$ ) make the data contents of the designated address location available at the data input/output ( $D_0 \sim D_7$ ). When the  $\overline{CE}$  or  $\overline{OE}$  signal is high, data input/output are in a floating state.

When the  $\overline{OE}$  signal is high, the device is in the stand-by mode or power-down mode.

### Programming

#### (Byte programming algorithm)

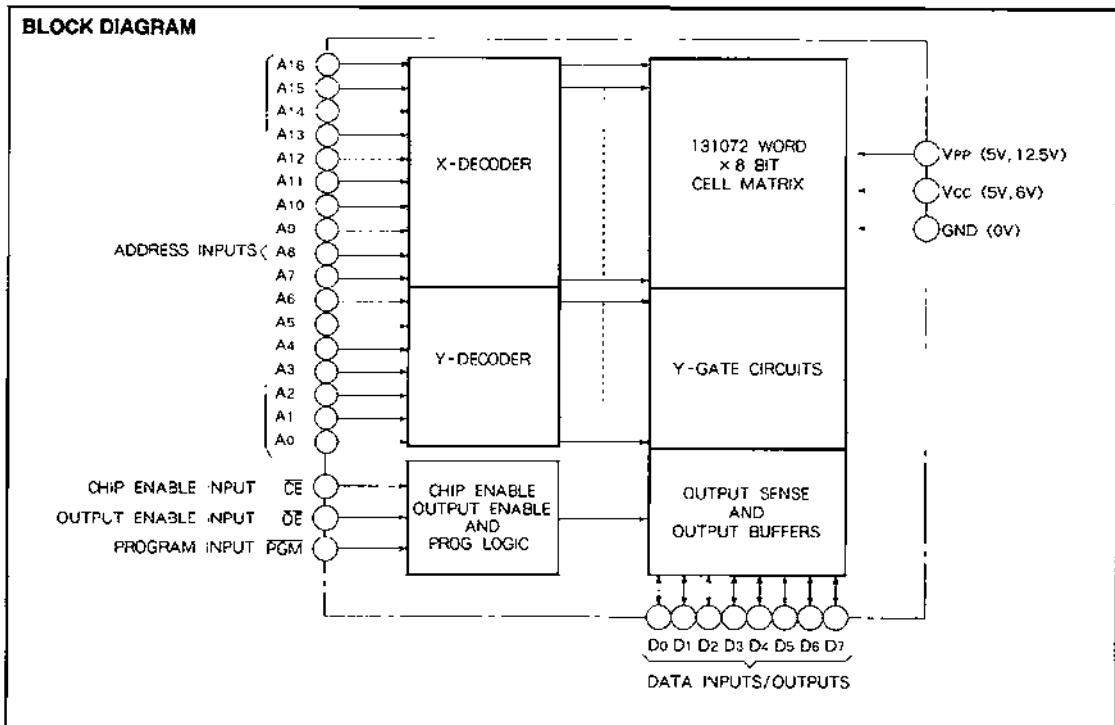
The M5M27C101P, FP, J, VP, RV-15 enter the byte programming mode when 12.5V is supplied to the  $V_{PP}$  power supply input.  $\overline{CE}$  is at low level and  $\overline{OE}$  is at high level. A location is designated by address signals ( $A_6 \sim A_0$ ), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ( $D_0 \sim D_7$ ). In this state, byte programming is completed when  $\overline{PGM}$  is at low level.

#### (Page programming algorithm)

Page programming feature of the M5M27C101P, FP, J, VP, RV-15 allow 4 bytes of data to be simultaneously programmed. The destination addresses for a page programming operation must reside on the same page; that is  $A_2$  through  $A_6$  must not change. At first, the M5M27C101P, FP, J, VP, RV-15 enter the page data latch mode when  $V_{PP} = 12.5V$ ,  $\overline{CE} = "H"$ ,  $\overline{OE} = "L"$  and  $\overline{PGM} = "H"$ . The four locations in same page are designated by address signals ( $A_0, A_1$  change) and the data to be programmed must be applied to each location at 8 bits in parallel to the data inputs ( $D_0 \sim D_7$ ). In this state, the data (4-bytes) latch is completed. Then the M5M27C101P, FP, J, VP, RV-15 enter the page programming mode when  $\overline{OE} = "H"$ . In this state, page (4-bytes) programming is completed when  $\overline{PGM} = "L"$ .

### Erase

The M5M27C101P, FP, J, VP, RV-15 cannot be erased, because they are packaged in plastic without in plastic transparent lid.



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**MODE SELECTION**

Mode	Pins	CE	OE	PGM	Vpp	Vcc	Data I/O
Read		V <sub>IL</sub>	V <sub>IL</sub>	X*	5V	5V	Data out
Output disable		V <sub>IL</sub>	V <sub>IH</sub>	X*	5V	5V	Floating
Stand-by (Power down)		V <sub>IH</sub>	X*	X*	5V	5V	Floating
Byte program		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	12.5V	6V	Data in
Program verify		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	12.5V	6V	Data out
Page data latch		V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	12.5V	6V	Data in
Page program		V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	12.5V	6V	Floating
Program inhibit		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	12.5V	6V	Floating
		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	12.5V	6V	
		V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	12.5V	6V	
		V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	12.5V	6V	

\* : X can be either V<sub>IL</sub> or V<sub>IH</sub>.

**ABSOLUTE MAXIMUM RATINGS (Note 1)**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>I1</sub>	All input or output voltage except V <sub>PP</sub> - A <sub>9</sub>	With respect to Ground	- 0.6~7	V
V <sub>I2</sub>	V <sub>PP</sub> supply voltage		- 0.6~14.0	V
V <sub>I3</sub>	A <sub>9</sub> supply voltage		0.6~13.5	V
T <sub>OP</sub>	Operating temperature		- 10~80	°C
T <sub>STG</sub>	Storage temperature		- 65~150	°C

Note 1 : Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

**READ OPERATION**

**DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>PP</sub> = V<sub>CC</sub>, unless otherwise noted)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>LI</sub>	Input leakage current	V <sub>IN</sub> = 0~V <sub>CC</sub>			10	μA
I <sub>LO</sub>	Output leakage current	V <sub>OUT</sub> = 0~V <sub>CC</sub>			10	μA
I <sub>PP1</sub>	V <sub>PP</sub> current read/stand-by	V <sub>PP</sub> = 5.5V		1	100	μA
I <sub>SB1</sub>	V <sub>CC</sub> current stand-by	CE = V <sub>IH</sub>			1	mA
I <sub>SB2</sub>		CE = V <sub>CC</sub>		1	100	μA
I <sub>CC1</sub>	V <sub>CC</sub> current Active	CE = OE = V <sub>IL</sub> , DC, I <sub>OUT</sub> = 0mA			50	mA
I <sub>CC2</sub>		CE = V <sub>IL</sub> , f = 6.7MHz, I <sub>OUT</sub> = 0mA			50	mA
V <sub>IL</sub>	Input low voltage		- 0.1		0.8	V
V <sub>IH</sub>	Input high voltage			2.0	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 2.1mA			0.45	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = - 400 μA	2.4			V

Note 2 : Typical values are at T<sub>a</sub> = 25°C and nominal supply voltages.

**AC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>PP</sub> = V<sub>CC</sub>, unless otherwise noted)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>a</sub> (AD)	Address to output delay	CE = OE = V <sub>IL</sub>			150	ns
t <sub>a</sub> (CE)	CE to output delay	OE = V <sub>IL</sub>			150	ns
t <sub>a</sub> (OE)	Output enable to output delay	CE = V <sub>IL</sub>			60	ns
t <sub>DF</sub>	Output enable high to output float	CE = V <sub>IL</sub>	0		50	ns
t <sub>OH</sub>	Output hold from CE, OE or address		0			ns

Note 3 : V<sub>CC</sub> must be applied simultaneously V<sub>PP</sub> and removed simultaneously V<sub>PP</sub>.

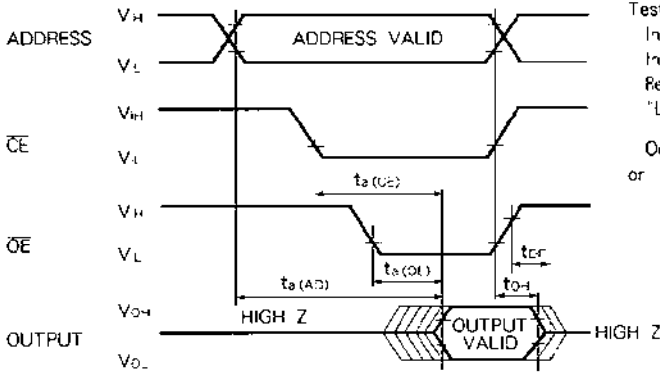
**CAPACITANCE**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>IN</sub>	Input capacitance (Address, CE, OE, PGM)	T <sub>a</sub> = 25°C, f = 1MHz, V <sub>i</sub> = V <sub>o</sub> = 0V			10	pF
C <sub>OUT</sub>	Output capacitance				15	pF

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## AC WAVEFORMS



Test conditions for A.C. characteristics

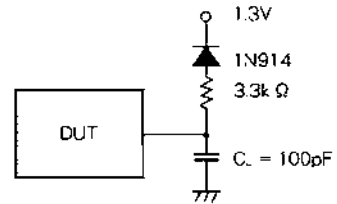
Input voltage : V<sub>L</sub> = 0.45V, V<sub>H</sub> = 2.4V

Input rise and fall times (10%~90%) : ≤ 20ns

Reference voltage at timing measurement: Input, Output  
"L" = 0.8V, "H" = 2V.

Output load: 1TTL gate + C<sub>L</sub> (= 100pF)

or



## PROGRAM OPERATION

### BYTE PROGRAMMING ALGORITHM

First set V<sub>CC</sub> = 6V, V<sub>PP</sub> = 12.5V and then set an address to first address to be programmed. After applying 0.2ms program pulse (PGM) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 0.2ms program pulse. The programmer continues 0.2ms pulse-then verify routines until the device verify correctly or twenty five of these pulse-then verify routines have been completed. The programmer also maintains its total

number of 0.2ms pulse applied to that address in register X. And then applied a program pulse X times of 0.2ms width as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. When the entire addresses have been programmed completely, all addresses should be verified with V<sub>CC</sub> = V<sub>PP</sub> = 5V.

## DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>L</sub>	Input leakage current	V <sub>IN</sub> = 0~V <sub>CC</sub>			10	μA
V <sub>O-L</sub>	Output low voltage (verify)	I <sub>O-L</sub> = 2.1 mA			0.45	V
V <sub>O-H</sub>	Output high voltage (verify)	I <sub>O-H</sub> = 400 μA	2.4			V
V <sub>L</sub>	Input low voltage		0.1		0.8	V
V <sub>H</sub>	Input high voltage		2.0		V <sub>CC</sub>	V
I <sub>CC</sub>	V <sub>CC</sub> supply current				50	mA
I <sub>PP</sub>	V <sub>PP</sub> supply current	CE = PGM = V <sub>L</sub>			50	mA

## AC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>AS</sub>	Address setup time		2			μs
t <sub>CE-S</sub>	OE setup time		2			μs
t <sub>DS</sub>	Data setup time		2			μs
t <sub>AH</sub>	Address hold time		0			μs
t <sub>D-H</sub>	Data hold time		2			μs
t <sub>DFP</sub>	Chip enable to output float delay		0		130	ns
t <sub>VCS</sub>	V <sub>CC</sub> setup time		2			μs
t <sub>VPS</sub>	V <sub>PP</sub> setup time		2			μs
t <sub>rw</sub>	PGM initial program pulse width		0.19	0.2	0.21	ms
t <sub>CPW</sub>	PGM over program pulse width		0.19		5.25	ms
t <sub>CE-S</sub>	OE setup time		2			μs
t <sub>CE</sub>	Data valid from OE				150	ns

Note 4: V<sub>CC</sub> must be applied simultaneously V<sub>PP</sub> and removed simultaneously V<sub>PP</sub>.



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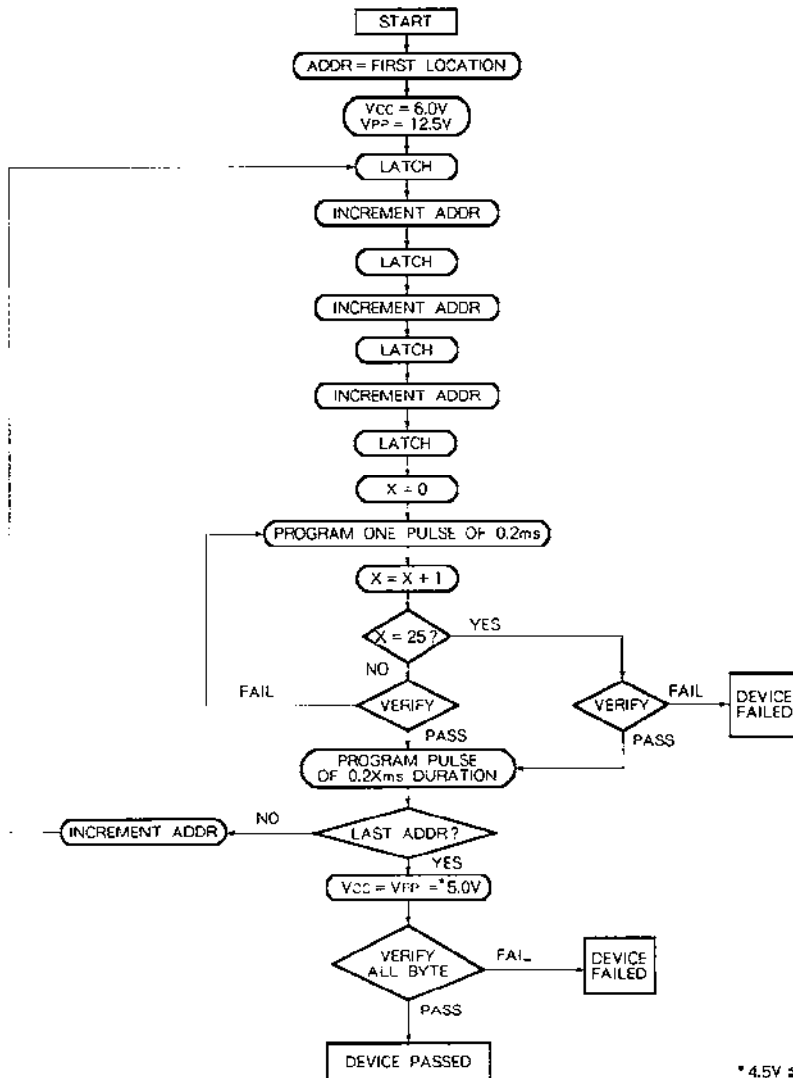
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## PAGE PROGRAMMING ALGORITHM

First set  $V_{CC} = 6V$ ,  $V_{PP} = 12.5V$  and then set an address to first page address to be programmed. After data of 4bytes are latched, these latch data are programmed simultaneously by applying 0.2ms program pulse. Then a verify is performed. If each output data is not verified correctly, apply one more 0.2ms program pulse. The programmer continues 0.2ms pulse-then-verify routines until each output data is verified correctly or twenty five of these pulse-then-verify routines have been completed.

The programmer also maintains its total number of 0.2ms pulse applied to that page addresses in register X. And then applied a program pulse X times of 0.2ms width as an overprogram pulse. When the programming procedure above is finished, step to the next page address and repeat this procedure till last page address to be programmed. When the entire page addresses have been programmed completely, all addresses should be verified with  $V_{CC} = V_{PP} = 5V$ .

## PAGE PROGRAMMING ALGORITHM FLOW CHART



\* 4.5V ≤ V<sub>CC</sub> = V<sub>PP</sub> ≤ 5.5V

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**DC ELECTRICAL CHARACTERISTICS** ( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6\text{V} \pm 0.25\text{V}$ ,  $V_{PP} = 12.5\text{V} \pm 0.3\text{V}$ , unless otherwise noted)

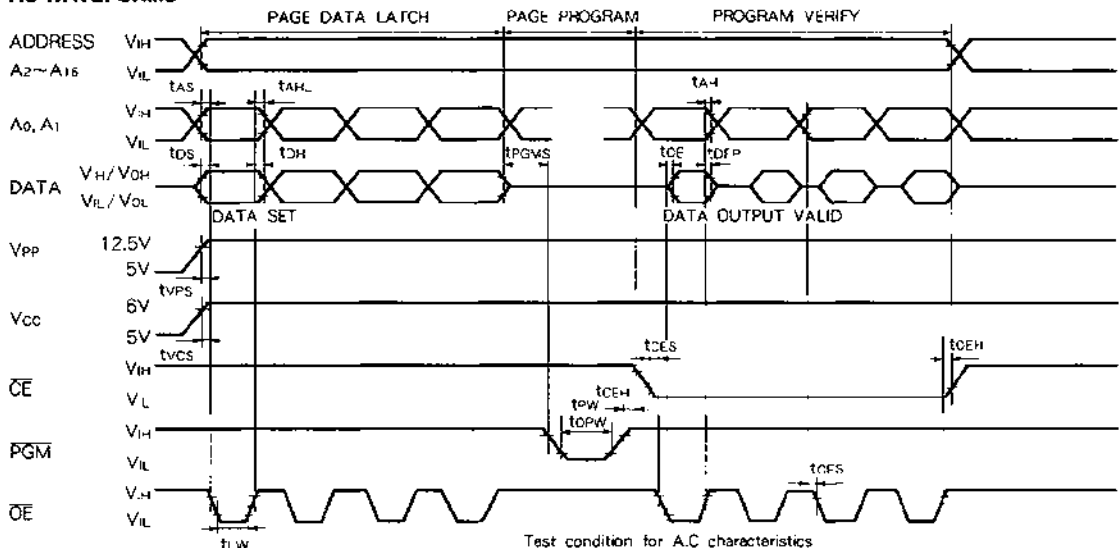
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{LI}$	Input leakage current	$V_{IN} = 0\text{V} \sim V_{CC}$			10	$\mu\text{A}$
$V_{OL}$	Output low voltage (verify)	$I_{OL} = 2.1\text{mA}$			0.45	V
$V_{OH}$	Output high voltage (verify)	$I_{OH} = -400\mu\text{A}$	2.4			V
$V_{IL}$	Input low voltage		-0.1		0.8	V
$V_{IH}$	Input high voltage		2.0		$V_{CC}$	V
$I_{CC}$	$V_{CC}$ supply current				50	mA
$I_{PP}$	$V_{PP}$ supply current	PGM = $V_{IL}$			100	mA

**AC ELECTRICAL CHARACTERISTICS** ( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6\text{V} \pm 0.25\text{V}$ ,  $V_{PP} = 12.5\text{V} \pm 0.3\text{V}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{AS}$	Address setup time		2			$\mu\text{s}$
$t_{CES}$	$\text{OE}$ setup time		2			$\mu\text{s}$
$t_{CS}$	Data setup time		2			$\mu\text{s}$
$t_{AH}$	Address hold time		0			$\mu\text{s}$
$t_{AHL}$			2			$\mu\text{s}$
$t_{DH}$	Data hold time		2			$\mu\text{s}$
$t_{DFP}$	$\text{OE}$ to output float delay		0		130	ns
$t_{VCS}$	$V_{CC}$ setup time		2			$\mu\text{s}$
$t_{VPS}$	$V_{PP}$ setup time		2			$\mu\text{s}$
$t_{PW}$	PGM initial program pulse width		0.19	0.2	0.21	ms
$t_{OPW}$	PGM over program pulse width		0.19		5.25	ms
$t_{CES}$	$\text{OE}$ setup time		2			$\mu\text{s}$
$t_{CE}$	Data valid from $\text{OE}$				50	ns
$t_{LW}$	Data latch time		1			$\mu\text{s}$
$t_{PGMS}$	PGM setup time		2			$\mu\text{s}$
$t_{CFH}$	$\text{OE}$ hold time		2			$\mu\text{s}$
$t_{CEH}$	$\text{OE}$ hold time		2			$\mu\text{s}$

Note 5:  $V_{CC}$  must be applied simultaneously  $V_{PP}$  and removed simultaneously  $V_{PP}$ .

**AC WAVEFORMS**



Test condition for A.C characteristics  
input voltage:  $V_L = 0.45\text{V}$ ,  $V_H = 2.4\text{V}$   
input rise and fall time: (10%~90%) :  $\leq 20\text{ns}$   
Reference voltage at timing measurement: Input, Output  
"L" = 0.8V, "H" = 2V

MITSUBISHI LSIs  
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 CMOS ONE TIME PROGRAMMABLE ROM**

**DEVICE IDENTIFIER MODE**

The Device Identifier Mode allows the reading of a binary code from the OTP ROM that identifies the manufacturer and device type.

The PROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

**M5M27C101P,FP,J,VP,RV-15 DEVICE IDENTIFIER CODE**

Code	Pin	A <sub>0</sub>	D <sub>7</sub>	C <sub>b</sub>	D <sub>c</sub>	D <sub>e</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Hex Data
Manufacturer code	V <sub>IL</sub>	0	0	0	1	1	1	0	0	0	1C
Device code	V <sub>H</sub>	1	0	0	0	0	0	1	1	83	

Note 6: A<sub>9</sub> = 12.0V ± 0.5V  
 A<sub>1</sub>~A<sub>8</sub>, A<sub>10</sub>~A<sub>16</sub>:  $\overline{CE}$ ,  $\overline{OE}$  = V<sub>IL</sub>, PGM = V<sub>H</sub>  
 V<sub>CC</sub> = V<sub>PP</sub> = 5V ± 10%

**RECOMMENDED SCREENING CONDITION**

The following screening test is recommended before using.

