# M52346SP

## SYNC SIGNAL PROCESSOR

### DESCRIPTION

When a separate sync signal (polarity, positive and negative; 1～5Vp-p), composite sync signal (polarity, positive and negative ; 1～5Vp-p), and sync ON video signal (polarity, negative) are input, M52346SP semiconductor integrated circuit automatically selects a suitable one, and shapes its waveform. This IC is optimal for automatic tracking type displays.

### FEATURES

- Sync input on/off data and polarity data can be output.
- Pulse output pins are an open collector output type.
- Regarding clamp pulse output, the trigger of clamp pulses is generated at the latter edge of sync ON video signal input. The trigger is also generated at the latter edge of separate sync signal input or composite sync signal input.
- 20-pin shrink dual in-line package.

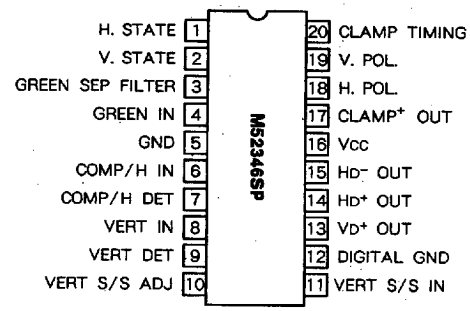
### APPLICATION

Display monitors

### RECOMMENDED OPERATING CONDITION

Supply voltage range ..... 11～13V
Rated supply voltage ..... 12V

### PIN CONFIGURATION (TOP VIEW)

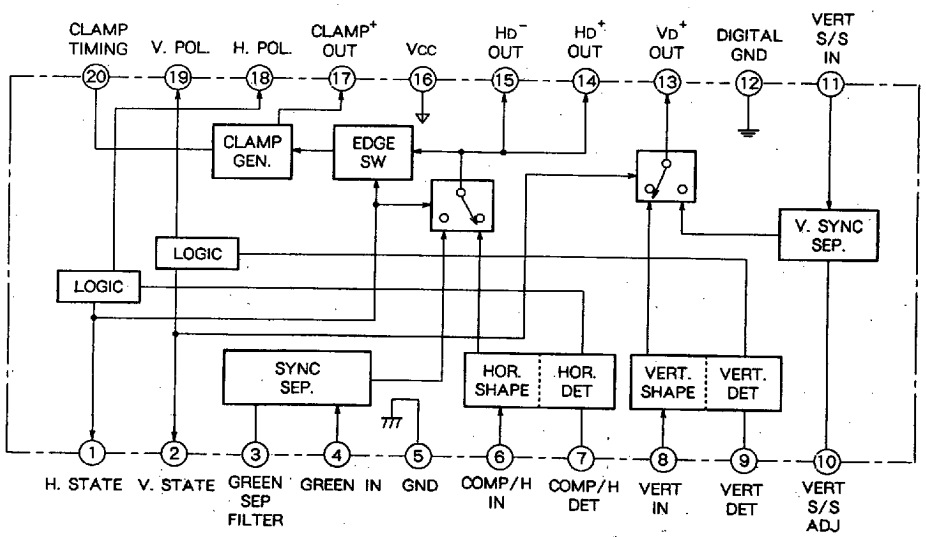



Outline 20P4B

### SPECIFICATIONS

- When a sync ON video signal is input : Sync ≧ 0.2Vp-p (polarity : negative)
- When a composite sync signal or separate sync signal is input : 1～5Vp-p (Polarity : positive and negative)
- $f_H \leqq 200kHz$
- Pulse output is an open collector type. Logical output is a TTL type.

### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** (Ta = 25℃, unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 14.0 | V |
| $P_d$ | Power dissipation | 1000 | mW |
| $T_{opr}$ | Operating temperature | −20～+85 | ℃ |
| $T_{stg}$ | Storage temperature | −40～+150 | ℃ |

**ELECTRICAL CHARACTERISTICS** (Ta = 25℃, $V_{CC}$ = 12V, $V_{DD}$ = 12V, unless otherwise noted)

| Symbol | Parameter | Test conditions: Switching conditions 4 | 6 | 8 | 16 | Input pin | Input conditions | Output pin | Output waveform | Limits: Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Icc | Circuit current | 2 | 2 | 2 | 2 | 16 | | A | | 25 | 35 | 45 | mA | No input to pins ④, ⑥ and ⑧. Grounded to GND with capacitance. $V_{DD}$ is open. |
| 1OH | Pin① output "High" level | 2 | 1 | 1 | 1 | 6 | 7.5μs 16kHz 1$V_{P-P}$ | 1 | DC | 4.0 | 5.0 | 5.3 | V | |
| | | | | | | 8 | 7.5μs 16kHz 1$V_{P-P}$ | | | | | | | |
| 1OL | Pin① output "Low" level | 2 | 1 | 1 | 1 | 6 | 7.5μs 16kHz 0.7$V_{P-P}$ | 1 | DC | − | − | 0.5 | V | Input signal 0.7$V_{P-P}$ is equivalent to NO SYNC |
| | | | | | | 8 | 7.5μs 16kHz 0.7$V_{P-P}$ | | | | | | | |
| 2OH | Pin② output "High" level | 2 | 1 | 1 | 1 | 6 | 7.5μs 16kHz 1$V_{P-P}$ | 2 | DC | 4.0 | 5.0 | 5.3 | V | |
| | | | | | | 8 | 7.5μs 16kHz 1$V_{P-P}$ | | | | | | | |
| 2OL | Pin② output "Low" level | 2 | 1 | 1 | 1 | 6 | 7.5μs 16kHz 0.7$V_{P-P}$ | 2 | DC | − | − | 0.5 | V | Input signal 0.7$V_{P-P}$ is equivalent to NO SYNC |
| | | | | | | 8 | 7.5μs 16kHz 0.7$V_{P-P}$ | | | | | | | |
| 18OH | Pin⑱ output "High" level | 2 | 1 | 1 | 1 | 6 | 7.5μs 16kHz 1$V_{P-P}$ | 18 | DC | 4.0 | 5.0 | 5.3 | V | |
| | | | | | | 8 | 7.5μs 16kHz 1$V_{P-P}$ | | | | | | | |

Refer to table 1 for truth values

**ELECTRICAL CHARACTERISTICS** (Cont.)

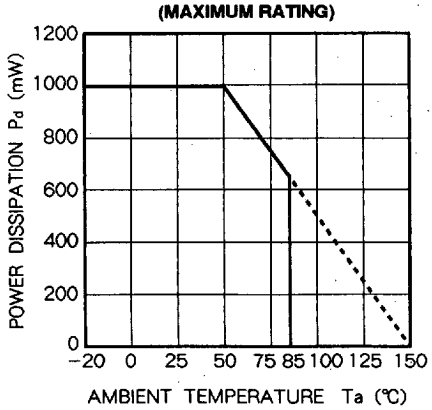
| Symbol | Parameter | Test conditions: Switching conditions 4 | 6 | 8 | 16 | Input pin | Input conditions | Output pin | Output waveform | Limits: Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 18OL | Pin⑱ output "Low" level | 2 | 1 | 1 | 1 | 6 | 7.5µs 16kHz 1VP-P | 18 | DC | – | – | 0.5 | V | Refer to table 1 for truth values |
| | | | | | | 8 | 7.5µs 16kHz 1VP-P | | | | | | | |
| 19OH | Pin⑲ output "High" level | 2 | 1 | 1 | 1 | 6 | 7.5µs 16kHz 1VP-P | 19 | DC | 4.0 | 5.0 | 5.3 | V | |
| | | | | | | 8 | 7.5µs 16kHz 1VP-P | | | | | | | |
| 19OL | Pin⑲ output "Low" level | 2 | 1 | 1 | 1 | 6 | 7.5µs 16kHz 1VP-P | 19 | DC | – | – | 0.5 | V | |
| | | | | | | 8 | 7.5µs 16kHz 1VP-P | | | | | | | |
| $V_{10}$ | Threshold voltage | 2 | 2 | 2 | 1 | | | 10 | DC | 0.7 | 1.0 | 1.4 | V | |
| SS – NV | Sync-Sep Sync input signal maximum noise amplitude voltage | 1 | 2 | 2 | 1 | 4 | 1.5µs 16kHz 0.1VP-P | 14 | There should be no pulse output | – | – | 0.1 | V | Input signal of 0.1VP-P is dummy noise signal. |
| SS – LV | Sync-Sep Sync input signal minimum amplitude voltage | 1 | 2 | 2 | 1 | 4 | 1.5µs 16kHz 0.2VP-P | 14 | 16kHz There should be no pulse output during this period | 0.2 | – | – | V | Check that there is no malfunction due to noise |
| 15OL | Pin⑮ HD⁻ output "Low" level | 2 | 1 | 2 | 1 | 6 | 7.5µs 16kHz 1VP-P | 15 | .....V Meas | – | – | 0.5 | V | |
| 14OL | Pin⑭ HD⁺ output "Low" level | 2 | 1 | 2 | 1 | 6 | 7.5µs 16kHz 1VP-P | 14 | .....V Meas | – | – | 0.5 | V | |
| 17OL | Pin⑰ CP⁺ output "Low" level | 2 | 1 | 2 | 1 | 6 | 7.5µs 16kHz 1VP-P | 17 | .....V Meas | – | – | 0.5 | V | |
| 13OL | Pin⑬ VD⁺ output "Low" level | 2 | 2 | 1 | 1 | 8 | 7.5µs 16kHz 1VP-P | 13 | .....V Meas | – | – | 0.5 | V | |

**ELECTRICAL CHARACTERISTICS** (Cont.)

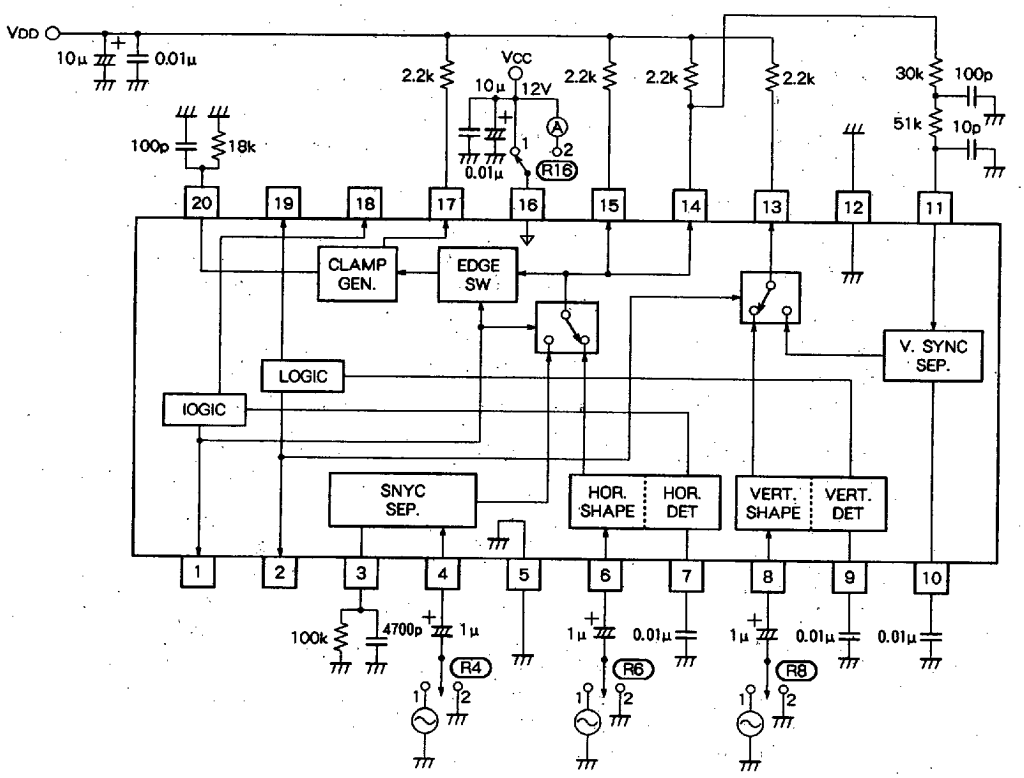
| Symbol | Parameter | Test conditions: Switching conditions 4 | 6 | 8 | 16 | Input pin | Input conditions | Output pin | Output waveform | Limits: Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $HD^-$–DA | $HD^-$– Delay time (A) | 2 | 1 | 2 | 1 | 6 | 7.5µs 16kHz 1Vp-p | 15 | Input (50%) Time Meas Output (50%) | – | 120 | 350 | ns | |
| $HD^-$–DB | $HD^-$– Delay time (B) | 2 | 1 | 2 | 1 | 6 | 7.5µs 16kHz 1Vp-p | 15 | Input (50%) Time Meas Output (50%) | – | 150 | 350 | ns | |
| $HD^+$–DA | $HD^+$– Delay time (A) | 2 | 1 | 2 | 1 | 6 | 7.5µs 16kHz 1Vp-p | 14 | Input (50%) Time Meas Output (50%) | – | 120 | 350 | ns | |
| $HD^+$–DB | $HD^+$– Delay time (B) | 2 | 1 | 2 | 1 | 6 | 7.5µs 16kHz 1Vp-p | 14 | Input (50%) Time Meas Output (50%) | – | 100 | 350 | ns | |
| $CP^+$–DT | $CP^+$– Delay time | 2 | 1 | 2 | 1 | 6 | 7.5µs 16kHz 1Vp-p | 17 | Input (50%) Time Meas Output (50%) | – | 180 | 350 | ns | |
| $CP^+$–PW | $CP^+$–PULSE – WIDTH | 2 | 1 | 2 | 1 | 6 | 7.5µs 16kHz 1Vp-p | 17 | Time Meas | 450 | 700 | 850 | ns | |
| $VD^+$–DA | $VD^+$– Delay time (A) | 2 | 2 | 1 | 1 | 8 | 7.5µs 16kHz 1Vp-p | 13 | Input (50%) Time Meas Output (50%) | – | 120 | 350 | ns | |
| $VD^+$–DB | $VD^+$– Delay time (B) | 2 | 2 | 1 | 1 | 8 | 7.5µs 16kHz 1Vp-p | 13 | Input (50%) Time Meas Output (50%) | – | 100 | 350 | ns | |

**TYPICAL CHARACTERISTICS**

**THERMAL DERATING (MAXIMUM RATING)**



## TEST CIRCUIT




Units Resistance : Ω
Capacitance : F

**Table1. Decoder logic output**

| Pin ⑥ input HD. COMP. | Pin ⑧ input VD | Output pin ① | ② | ⑱ | ⑲ |
|---|---|---|---|---|---|
| HD. COMP.(POS.) | NON | H | L | L | L |
| HD. COMP.(POS.) | VD (POS.) | H | H | L | L |
| HD. COMP.(POS.) | VD (NEG.) | H | H | L | H |
| HD. COMP.(NEG.) | NON | H | L | H | L |
| HD. COMP.(NEG.) | VD (POS.) | H | H | H | L |
| HD. COMP.(NEG.) | VD (NEG.) | H | H | H | H |
| NON | NON | L | L | L | L |
| NON | VD (POS.) | L | H | L | L |
| NON | VD (NEG.) | L | H | L | H |

**Table2. Allowable input amplitude voltage**

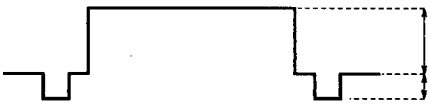
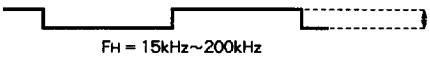
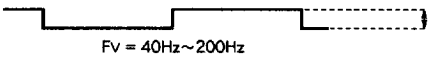
| | |
|---|---|
| Pin ④ input amplitude |  VV 0~2.1 (VP-P) VS 0.2~0.6 (VP-P) |
| Pin ⑥ input amplitude |  FH = 15kHz~200kHz VS 1.0~5.0 (VP-P) |
| Pin ⑧ input amplitude |  FV = 40Hz~200Hz VS 1.0~5.0 (VP-P) |

**Table3. The order of priority in output**

| Input signal (pin) | | | Output signal (pin) | | |
|---|---|---|---|---|---|
| Pin ④ | Pin ⑥ | Pin ⑧ | Pin ⑭ and ⑮ | Pin ⑬ | Pin ⑰ |
| ○ | × | × | 4 | 11 | 4 |
| ○ | ○ | × | 6 | 11 | 6 |
| ○ | × | ○ | 4 | 8 | 4 |
| ○ | ○ | ○ | 6 | 8 | 6 |
| × | × | × | × | × | × |
| × | ○ | × | 6 | 11 | 6 |
| × | × | ○ | × | 8 | × |
| × | ○ | ○ | 6 | 8 | 6 |

**Table4. Maximum allowable input signal pulse duty ratio**

**Pin ⑤ input pulse (HD. COMP.)** FH = 16kHz

| Maximum amplitude voltage (VP-P) | | 1.0 | 3.3 | 4.0 | 5.0 |
|---|---|---|---|---|---|
| POS. | % | 15.0 | 13.8 | 11.2 | 9.0 |
| | Time (μs) | 9.38 | 8.63 | 7.00 | 5.63 |
| NEG. | % | 15.0 | 13.0 | 10.5 | 8.8 |
| | Time (μs) | 9.38 | 8.13 | 6.56 | 5.50 |

**Pin ⑤ input pulse (VD)** FV = 60Hz

| Maximum amplitude voltage (VP-P) | | 1.0 | 3.3 | 4.5 | 5.0 |
|---|---|---|---|---|---|
| POS. | % | 14.1 | 12.1 | 9.8 | 7.7 |
| | Time (ms) | 2.35 | 2.02 | 1.63 | 1.28 |
| NEG. | % | 14.8 | 11.3 | 9.2 | 7.5 |
| | Time (ms) | 2.47 | 1.88 | 1.53 | 1.25 |

## APPLICATION METHOD

### 1. Input section

1) Green (Sync ON Video) input (pin ③ and ④)
Sync ON Video signals are input in negative polarity. For sync separation, the sync chip is clamped with an external capacitor connected to pin ④ as well as capacitance and resistance connected to pin ③. The pin ④ sync chip is approximately 4V.
Threshold voltage is set to a level that is approximately + 0.1V less than the sync chip.

2) Input of composite sync, H sync, and V sync signals
composite sync input is connected to pin ⑥. For sepatate sync input, H is connected to pin ⑥ and V is connected to pin ⑧. The bias of pin ⑥ and pin ⑧ is 6V, and the impedance is 10kΩ. Waveform shaping and polarity detection are conducted by a built-in double threshold converter.
The internal circuit is connected as shown in Fig. 2. The average DC voltage of input signals is called $V_2$. Threshold voltages are adjusted to $V_2 \pm 0.7V$.
Therefore, when the duty ratio is small as shown in Fig. 1, this IC works with an amplitude of approximately $0.7V_{P-P}$ or more. When the duty ratio is large, the optimal amplitude is approximately $1.4V_{P-P}$. Fig. 3 shows allowable input duty reference measured values.

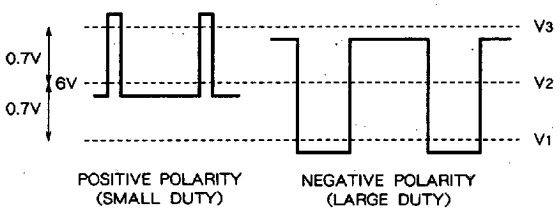



**Fig. 1**

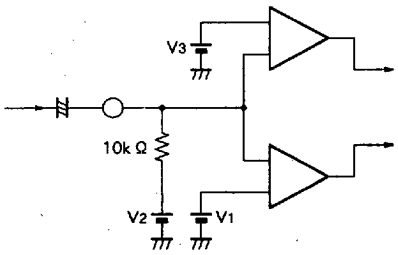



**Fig. 2**

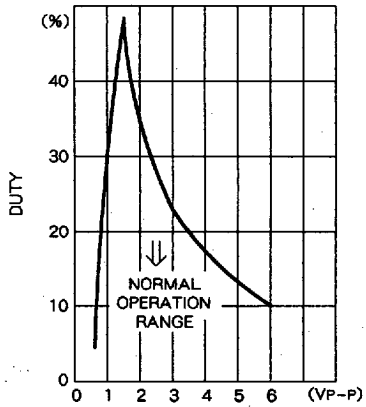



**Fig. 3**

Fig. 4 shows an application example in which the allowable duty ratio characteristic can be improved when input amplitude is $1.4V_{P-P}$ or more.

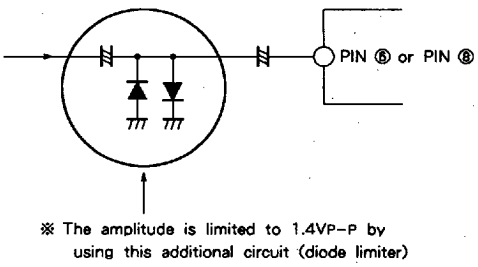



**Fig. 4**

When the IC is used at voltage outside the rated range, remove filters from pins ⑦ and ⑨, and check the waveform to ensure that it is as shown in Fig. 5.

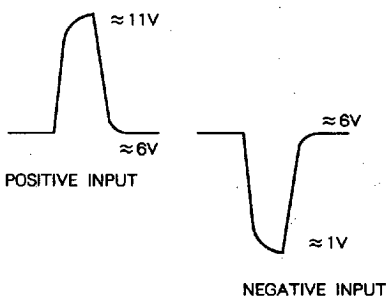



**Fig. 5**

3) Polarity detection and no-input detection (pins ⑦ and ⑨)
External capacitance is necessary as a filter to detect polarity and "no-input." The larger the capacitance, the smaller the ripple, diminishing malfunction probability. However, when large capacitance is provided, the responce slows down. Capacitance should be at least 0.05μF when input is 15kHz. It should be at least 10 μF when input is 60Hz. For operation with lower capacitance, check the filter pin waveform under conditions where input sync signal frequency and duty ratio are set to a minimum, and check that voltage is 7.5V or more (6.6V actually) when input is positive, and that voltage is 4.5V or less (5.5V actually) when input is negative.

4) VERT S/S IN (pin ⑪)
For V sync separation, signals are generated by externally integrating composite sync signals, and are then input.
The composite sync signals that are input to pin ⑥ (H + V) are output to pin ⑭ HD*. For V sync separation, pin ⑭ HD* output is externally integrated, and is input to pin ⑪. Check pin ⑪ waveform to see if the H element is adequately low.
In the IC, the sync separation threshold level is set to approximately 1V when no external adjustment is provided.

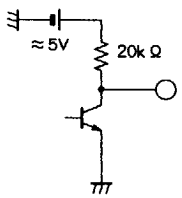
5) VERT S/S ADJ (pin ⑩)
The threshold voltage is approximately 1V when no external adjustment is provided. The threshold voltage is dependent on IC internal resistance. Pin ⑩ may be open ; however, if noise may give adverse effect, ground the pin with capacitor.
When the H element cannot be lowered sufficiently, connect resistance between pin ⑩ and Vcc to change the threshold level. (Provide resistance such that when $V_{DD}$(Digital Vcc) is 12V, the threshold voltage will be 8V or less ; and when $V_{DD}$ is 5V, the threshold voltage will be 4V or less.)
When there are serration pulses or other pulses during the V period, provide resistance such that the threshold voltage will be half as high as $V_{DD}$.

**2. CP-Width**

Timing pin (pin ⑳)
The time constant is determined depending on the current that flows out of pin ⑳ and timing pin capacitance. The current is normally determined depending on pin voltage and external resistance. When external resistance is 18kΩ (namely 200μA) and timing pin external capacitance is 100pF, the pulse width is 0.7μsec.

**3. Output stage**

1) Logic output (pins ①, ②, ⑱ and ⑲)
The output type is as shown below.
IC internal load resistance is 20kΩ.



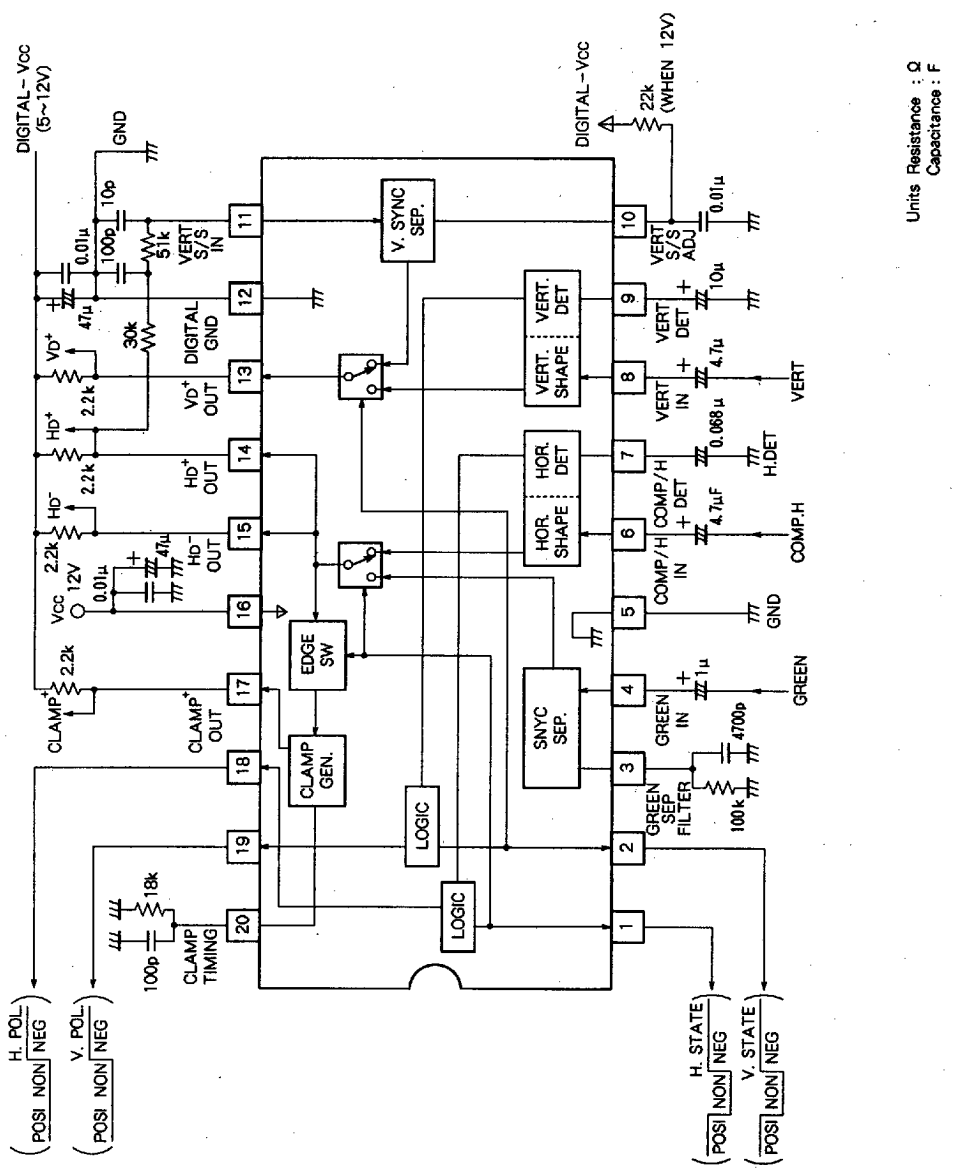

2) Pulse output (pins ⑬, ⑭, ⑮ and ⑰)
The pins are the open collector type as shown below. Current of approximately 6mA can be applied.

3) Power supply
Supply 12V to pin ⑯.
Supply digital Vcc = 5~12V as power supply for pulse output.

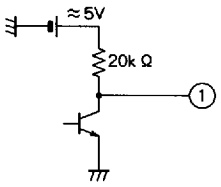
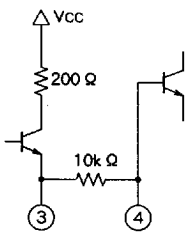
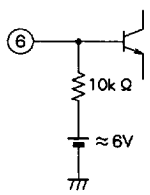
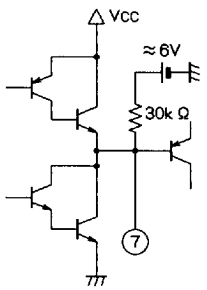

**4. Other**

Differences between M52036SP and M52346SP
The clamp pulse trigger is different between M52036SP and M52346SP when "S on G" and "H/H + V" are input simultaneously, or when only "H/H + V" is input.
M52036SP·····Generated at the first edge of "H/H + V" input.
M52346SP·····Generated at the latter edge of "H/H + V" input.
M52346SP clamp pulses are generated at the latter edge of signals that have been given priority.
We believe this arrangement makes this IC more useful with MAC signals.
The M52346SP pin configuration is the same as that of M52036SP.

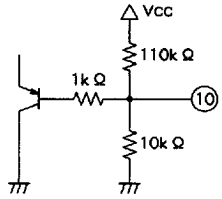
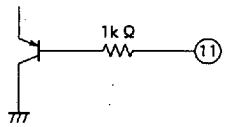
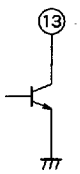
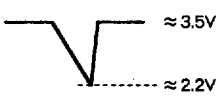
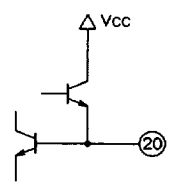
**RECOMMENDED CIRCUIT** ($f_H$ = 15kHz, $f_V$ = 60Hz)



## DESCRIPTION OF PIN

| Pin no. | Name | Pin voltage | Equivalent circuit | Description of pin |
|---|---|---|---|---|
| ① | H. STATE | 0VDC or 5VDC |  | Horizontal sync signal logic output pin.<br>Outputs "H" when pin ⑥ input signal is positive ;<br>outputs "L" when there is no input ; and outputs "H" when pin ⑥ input signal is negative. |
| ② | V. STATE | 0VDC or 5VDC | The same as pin ① | Vertical sync signal logic output pin.<br>Outputs "H" when pin ⑧ input signal is positive ;<br>outputs "L" when there is no input ; and outputs "H" when pin ⑧ input signal is negative. |
| ③ | GREEN SEP FILTER | When open<br>≈4V |  | GREEN (Video) SEP FILTER pin.<br>Biases itself according to external capacitance (C) and resistance (R) time constant.<br>Resistance (R) is a discharging type, and is provided to enhance self-biasing circuit responding characteristics.<br>The smaller the resistance, the smaller the self-biasing circuit gain. |
| ④ | GREEN IN | When open<br>≈4V | | GREEN (Sync on Video) input pin.<br>C-connected, and inputs Green (Sync on Video) signal.<br>Sync is negative. |
| ⑤ | GND | —— | —— | Grounding |
| ⑥ | COMP/H IN | When open<br>≈6V |  | Composite sync/H sync input pin.<br>Bias is approximately 6V, and impedance is 10k Ω.<br>Waveform shaping and polarity detection are conducted by built-in double threshold comparator. The optimal input amplitude is approximately 1.5VP-P. The waveform shaping and polarity detection are possible when the duty is approximately 50% or less. |
| ⑦ | COMP/H DET | When open<br>≈6V<br>(No signal) |  | External capacitance is required as filter pin for polarity detection and no-input detection. The larger the capacitance, the smaller the ripple, reducing malfunction probability. However, detection response becomes slow. |
| ⑧ | VERT IN | When open<br>≈6V | The same as pin ⑥ | V sync input pin<br>The same as pin ⑥ |
| ⑨ | VERT DET | When open<br>≈6V<br>(No signal) | The same as pin ⑦ | The same as pin ⑦ |

**DESCRIPTION OF PIN** (Cont.)

| Pin no. | Name | Pin voltage | Equivalent circuit | Description of pin |
|---|---|---|---|---|
| ⑩ | VERT S/S ADJ | When open ≈1V |   | VERT S/S ADJ pin When no external adjustment is conducted, threshold voltage is approximately 1V. |
| ⑪ | VERT S/S IN | —— |   | VERT S/S IN pin Signals that are obtained by externally integrating compsite sync signals for V sync separation are input. |
| ⑫ | DIGITAL GND | —— | —— | Grounding |
| ⑬ | $VD^+$ OUT | |   | $VD^+$ Pulse output pin Open collector output type. Output amplitude is variable. Able to accommodate 6mA currents. |
| ⑭ | $HD^+$ OUT | | The same as pin ⑬ | $HD^+$ Pulse output pin The same as pin ⑬ |
| ⑮ | $HD^-$ OUT | | The same as pin ⑬ | $HD^-$ Pulse output pin The same as pin ⑬ |
| ⑯ | Vcc | 12V | —— | Power source |
| ⑰ | $CLAMP^+$ OUT | | The same as pin ⑬ | $Clamp^+$ Pulse output pin The same as pin ⑬ |
| ⑱ | H. POL. | 0VDC or 5VDC | The same as pin ① | Horizontal sync signal logic output pin. Outputs "L" when pin ⑥ input signal is positive or when there is no input to pin ⑥. Outputs "H" when pin ⑥ input signal is negative. |
| ⑲ | V. POL. | 0VDC or 5VDC | The same as pin ① | Horizontal sync signal logic output pin. Outputs "L" when pin ⑧ input signal is positive or when there is no input to pin ⑧. Outputs "H" when pin ⑧ input signal. |
| ⑳ | CLAMP TIMING |   |   | Clamp timing pin. Clamp pulse amplitude is determined depending on external capacitance (C) and resistance (R). The larger the C and R, the larger clamp pulse width. |