M29W102BT
M29W102BB

1 Mbit (64Kb x16, Boot Block)
Low Voltage Single Supply Flash Memory

- SINGLE 2.7 to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- ACCESS TIME: 50ns
- PROGRAMMING TIME
  - 10µs per Word typical
- 5 MEMORY BLOCKS
  - 1 Boot Block (Top or Bottom Location)
  - 2 Parameter and 2 Main Blocks
- PROGRAM/ERASE CONTROLLER
  - Embedded Word Program algorithm
  - Embedded Multi-Block/Chip Erase algorithm
  - Status Register Polling and Toggle Bits
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- TEMPORARY BLOCK UNPROTECTION MODE
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- M28F102 COMPATIBLE
  - Pin-out and Read Mode
- 20 YEARS DATA RETENTION
  - Defectivity below 1 ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code M29W102BT: 0099h
  - Bottom Device Code M29W102BB: 0098h

TSOP40 (N)
10 x 14mm

Figure 1. Logic Diagram

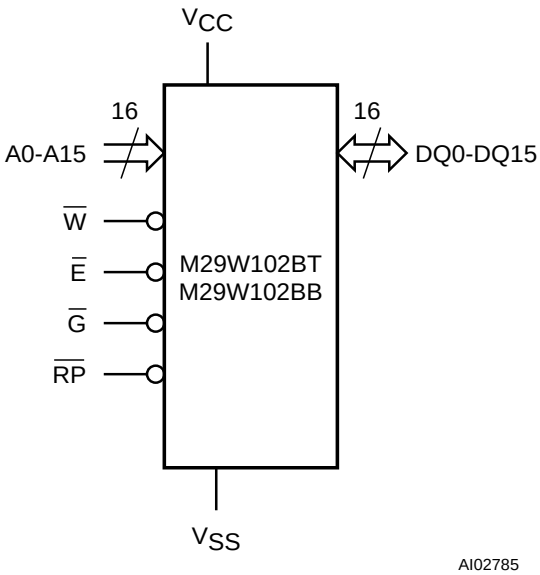


Figure 2. TSOP Connections

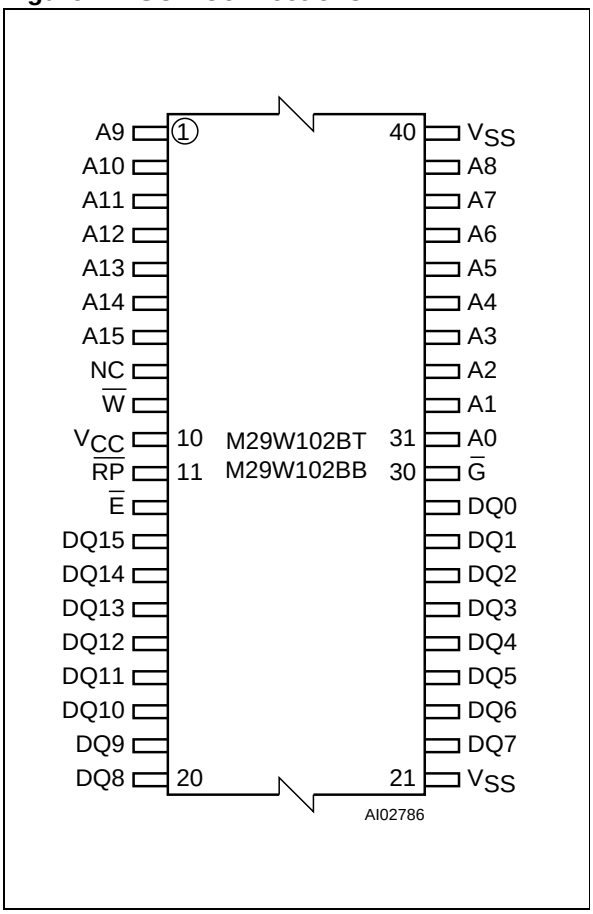


Table 1. Signal Names

A0-A15	Address Inputs
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

SUMMARY DESCRIPTION

The M29W102B is a 1 Mbit (64Kb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks in the memory are asymmetrically arranged, see Tables 3 and 4, Block Addresses. The first or last 32 Kwords have been divided into four additional blocks. The 8 Kword Boot Block can be used for small initialization code to start the microprocessor, the two 4 Kword Parameter Blocks can be used for parameter storage and the remaining 16 Kwords are a small Main Block where the application may be stored.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in a TSOP40 (10 x 14mm) package and it is supplied with all the bits erased (set to '1').

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (Temperature Range Option 1)	0 to 70	°C
	Ambient Operating Temperature (Temperature Range Option 6)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltage	–0.6 to 4	V
V_{CC}	Supply Voltage	–0.6 to 4	V
V_{ID}	Identification Voltage	–0.6 to 13.5	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns during transitions.

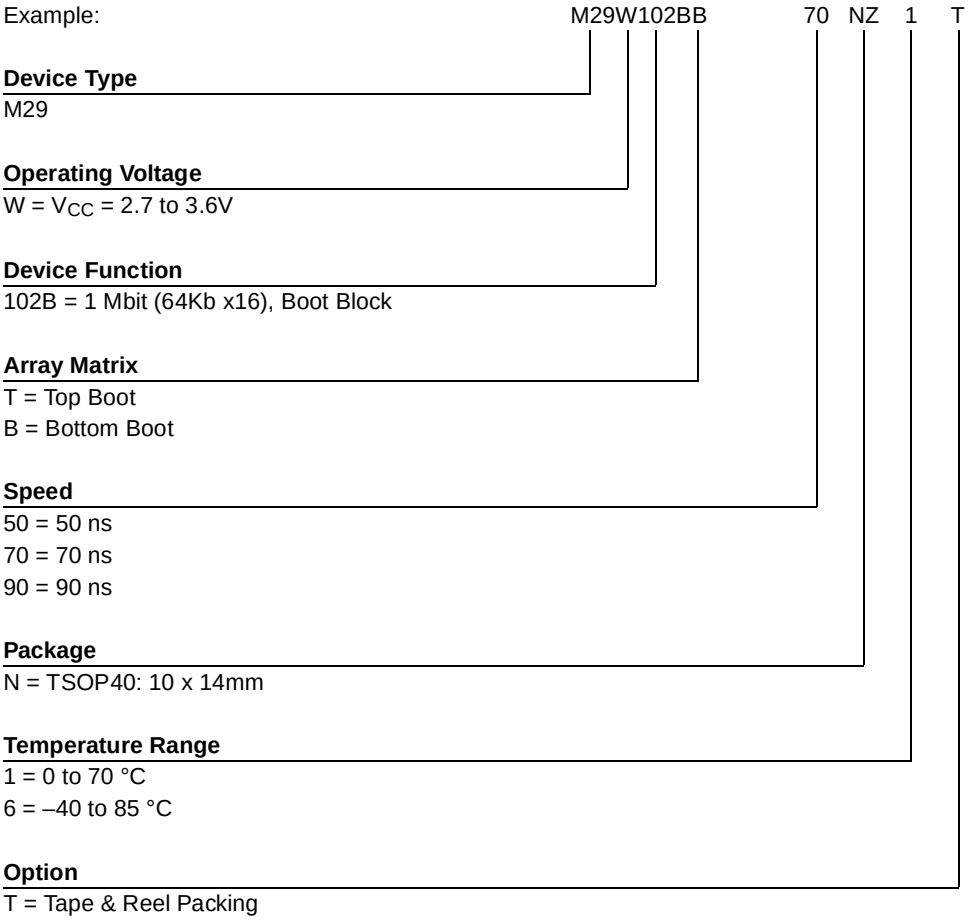
Table 3. Top Boot Block Addresses M29W102BT

#	Size (KWords)	Address Range
4	8	E000h-FFFFh
3	4	D000h-DFFFh
2	4	C000h-CFFFh
1	16	8000h-BFFFh
0	32	0000h-7FFFh

Table 4. Bottom Boot Block Addresses M29W102BB

#	Size (KWords)	Address Range
4	32	8000h-FFFFh
3	16	4000h-7FFFh
2	4	3000h-3FFFh
1	4	2000h-2FFFh
0	8	0000h-1FFFh

Table 16. Ordering Information Scheme



Note: The last two characters of the ordering code may be replaced by a letter code for preprogrammed parts, otherwise devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.