

# MOS INTEGRATED CIRCUITS



M 089  
M 099

## 2 x 8 CROSSPOINT MATRIX

- VERY LOW ON RESISTANCE
- HIGH CROSS-TALK AND OFF-STATE ISOLATION
- SERIAL SWITCH ADDRESSING,  $\mu$ -PROCESSOR COMPATIBLE

The M089 and M099 are 2x8 crosspoint matrices consisting of 16 N-channel MOS transistors. Both devices are similar in operation, the only difference being that in the M099 the "all switches reset" function is implemented by a microprocessor command.

Both devices have been specially designed to provide switches with low cross-talk, high off-state isolation (both better than -90 dB) and low on-resistance.

## ABSOLUTE MAXIMUM RATINGS\*

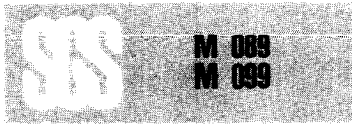
$V_{DD}^{**}$	Supply voltage	-0.5 to 17	V
$V_I$	Input voltage pins 4, 5, 12, 13	-0.5 to 17	V
$V_{IN}-V_{OUT}$	Differential voltage across any disconnected switch	10	V
$P_{tot}$	Total power dissipation	640	mW
$T_{op}$	Operating temperature range: for plastic	0 to 70	$^{\circ}C$
	for ceramic	-40 to 70	$^{\circ}C$
$T_{stg}$	Storage temperature range	-65 to 150	$^{\circ}C$

\* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\*\* With respect to  $V_{SS}$  (GND) pin.

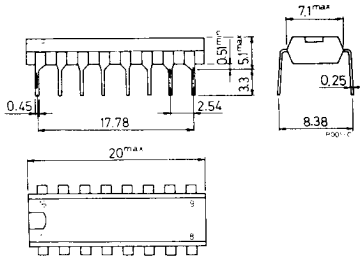
## ORDERING NUMBERS:

- M089/M099 B1 for dual-in-line plastic package
- M089/M099 D1 for dual-in-line ceramic package
- M089/M099 F1 for dual-in-line ceramic package, frit seal

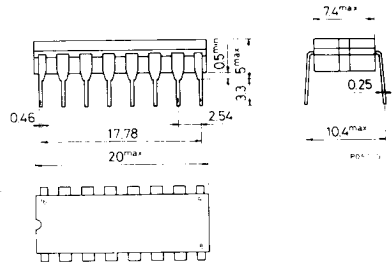


## MECHANICAL DATA (dimensions in mm)

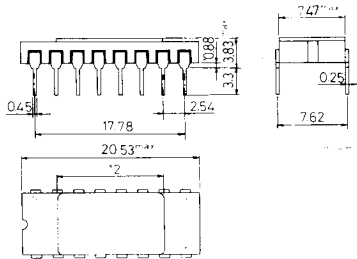
Dual-in-line plastic package



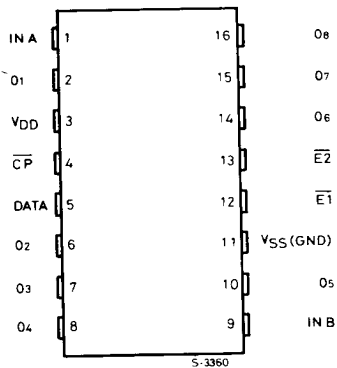
Dual-in-line ceramic package frit seal



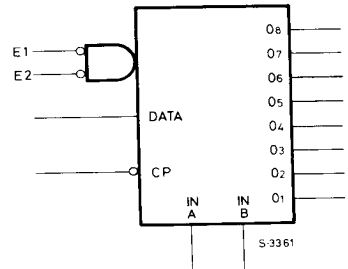
Dual-in-line ceramic package



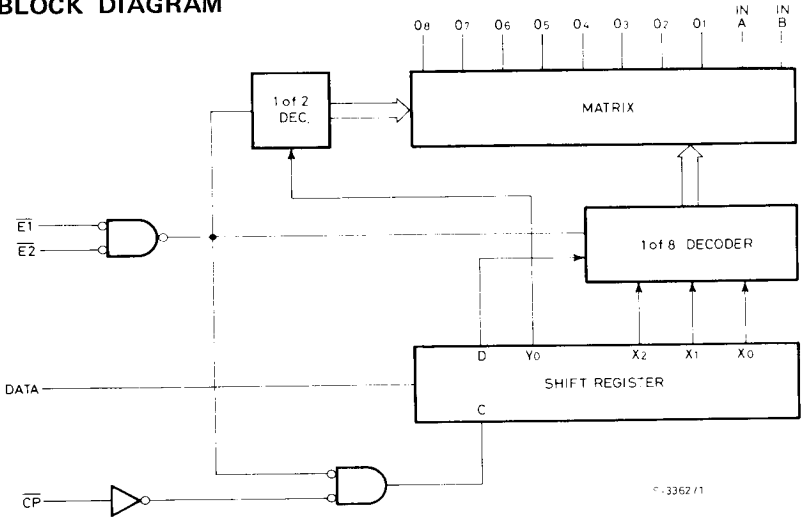
## PIN CONNECTIONS



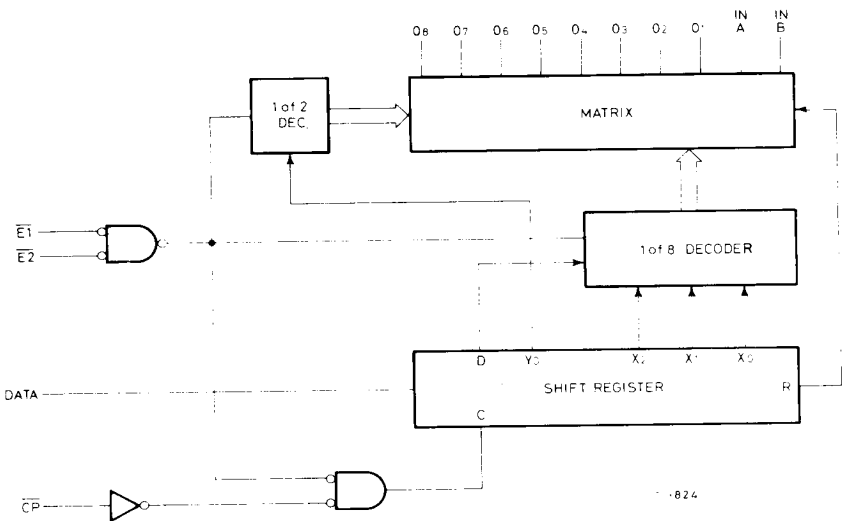
## LOGIC DIAGRAM

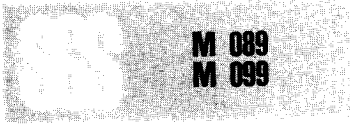


**M089 BLOCK DIAGRAM**



**M099 BLOCK DIAGRAM**

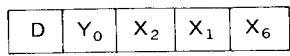




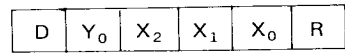
**M 089**  
**M 099**

### CIRCUIT DESCRIPTION

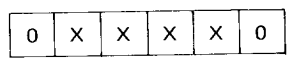
The M089 and M099 are capable of forming any combination of switch conditions in an 8x2 matrix. Each switch is individually set and a latch maintains it in its set condition. The switch address and control bits are loaded serially into an internal shift register (5 bit for M089, 6 bit for M099) when inputs  $E_1$ , and  $E_2$  are low. The address bits in both matrices consist of: 3 input selection bits ( $X_0$ - $X_2$ ) and a single output selection bit ( $Y_0$ ). A fifth (control) bit (D) defines whether the chosen switch is to be opened or closed. In the M099 a sixth bit (R) is an "all switch reset". Reset occurs on the low to high transition of the enable inputs when both D and R are zero. During normal selection the R bit must be a 1.



M089 Shift Register Bit Allocation



M099 Shift Register Bit Allocation



M099 Reset Word.

Data bits are clocked into the shift register on the high to low transition of the clock input (CP). If more than 5 (or 6 in the case of the M090) clock transmission are applied during loading of the shift register the last 5 (or 6) data bits are loaded into it. The status of the switch addressed changes on the low to high transition of one or both enable inputs.

### ENABLE INPUTS TRUTH TABLE

$\bar{E}_1$	$\bar{E}_2$	FUNCTION	
		M089	M099
L	L	Data Load	
	L	addressed switch changed	addressed switch changed or all switch reset
L			

**DATA BIT TRUTH TABLE**

- M089 -	
Data	Switch status after enable transition
L	disconnect
H	connect

**DATA AND RESET BIT TRUTH TABLE**

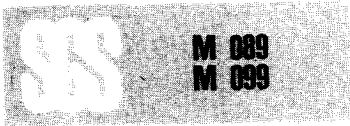
- M099 only -		
D	R	Switch status
L	L	all switches reset
H	L	no change
L	H	addressed switch disconnected
H	H	addressed switch connected

**DATA BITS TRUTH TABLE FOR SWITCH SELECTION**

	O <sub>1</sub> Y <sub>0</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>
IN A	1111	1011	1101	1001	1110	1010	1100	1000
IN B	0111	0011	0101	0001	0110	0010	0100	0000

For example to address the switch connecting IN A to O<sub>5</sub> the shift register must be loaded with the code:

	M089	M099
	D Y <sub>0</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub>	D Y <sub>0</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub> R
to connect	11110	111101
to disconnect	01110	011101



**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 0$  to  $70^{\circ}\text{C}$  for M089/M099 B1;  $-40$  to  $70^{\circ}\text{C}$  for M089/M099 F1, D1;  $V_{DD} = 14\text{V}$  to  $16\text{V}$  unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$R_{ON}^*$	ON-resistance	$T_{amb} = 25^{\circ}\text{C}$ $V_i(A, B) = 3.5\text{V}$ $V_{DD} = 14\text{V}$ $I_{D(min)} = 10\text{mA}$		10	15	$\Omega$
$\Delta R_{ON}$	ON-resistance variation in any package	$T_{amb} = 25^{\circ}\text{C}$ $V_i = 3.5\text{V}$ $V_{DD} = 14\text{V}$ $I_D = 10\text{mA}$			$\pm 2$	%
$I_{DD}$	Supply current				7	mA
$I_{LI}$	Input leakage	pins 4, 5, 12, 13	$V_i = 5\text{V}$		1	$\mu\text{A}$
		pins 1, 9	$V_{iA}, V_{iB} = 4.5\text{V}$ $V_{O1}, V_{O8} = 1.5\text{V}$		0.2	$\mu\text{A}$
			$V_{iA}, V_{iB} = 6\text{V}$ $V_{O1}, V_{O8} = 1.5\text{V}$		1	$\mu\text{A}$
$I_{LO}$	Output leakage	pins 2, 6, 7, 8, 10, 14, 15, 16	$V_{O1}, V_{O8} = 4.5\text{V}$ $V_{iA}, V_{iB} = 1.5\text{V}$		0.2	$\mu\text{A}$
		$V_{O1}, V_{O8} = 6\text{V}$ $V_{iA}, V_{iB} = 1.5\text{V}$		1	$\mu\text{A}$	
$V_{low}$	Logic 0 input level	All inputs	-0.3		0.8	V
$V_{high}$	Logic 1 input level	All inputs	4.5		$V_{DD}$	V
CT	Cross-talk attenuation	See fig. 4	90	95		dB
$I_O$	Off isolation	See fig. 5	90	95		dB
$f_{CL}$	Maximum clock input frequency	See fig. 6 for M089 See fig. 7 for M099			1	MHz
$T_{LG}$	Lag time		100			ns
$T_{LD1}$	Lead time		400			ns
$T_{LD2}$			150			
$T_{WR}$	Write time				3	$\mu\text{s}$
$t_w$	Clock pulse width		0.4		100	$\mu\text{s}$

\* See fig. 1 and 2 for  $R_{ON}$  variation with temperature and  $V_{BIAS}$ .

Fig. 1 -  $R_{ON}$  derating vs. temperature typ.

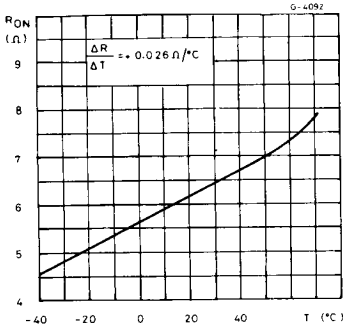
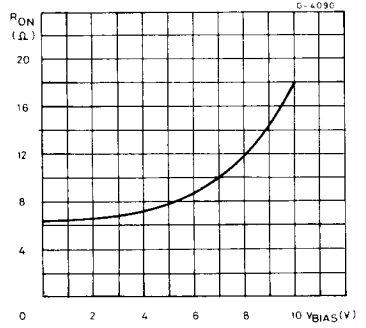


Fig. 2 -  $R_{ON}$  derating vs.  $V_{BIAS}$ .



**TEST CIRCUITS**

Fig. 3 -  $R_{ON}$  measurement

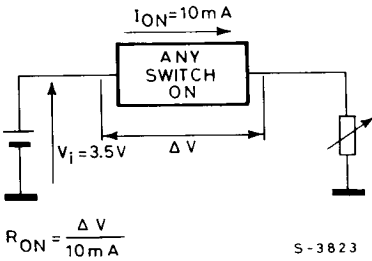


Fig. 4 - Crosstalk measurements

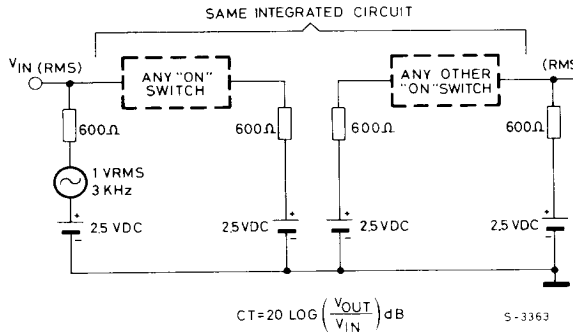
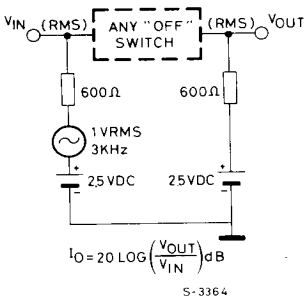


Fig. 5 - Off isolation measurement





## TIMING DIAGRAMS

Fig. 6 - M089 timing diagram

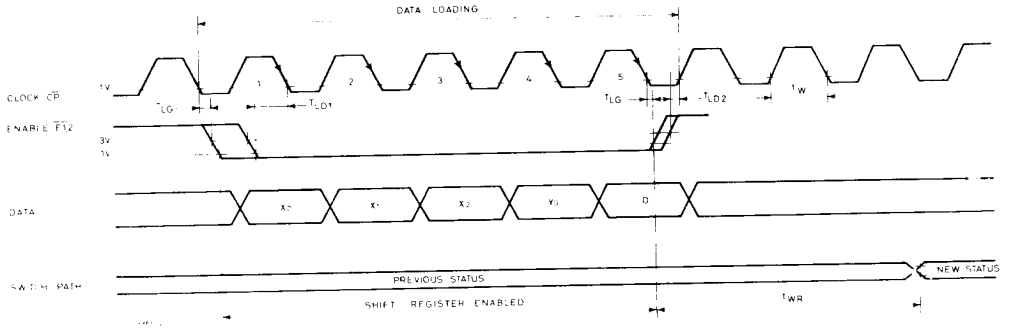


Fig. 7 - M099 timing diagram

