May 2000

National Semiconductor

LP3961/LP3964
800mA Fast Ultra Low Dropout Linear Regulators

General Description

The LP3961/LP3964 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very fast to step changes in load which makes them suitable for low voltage microprocessor applications. The LP3961/LP3964 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3961/LP3964 to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low dropout voltage; typically 24mV at 80mA load current and 240mV at 800mA load current.

Ground Pin Current: Typically 4mA at 800mA load current.

Shutdown Mode: Typically 15µA quiescent current when the shutdown pin is pulled low.

$\overline{\text{Error}}$ Flag: $\overline{\text{Error}}$ flag goes low when the output voltage drops 10% below nominal value (for LP3961).

SENSE: Sense pin improves regulation at remote loads. (For LP3964)

Precision Output Voltage: Multiple output voltage options are available ranging from 1.2V to 5.0V and adjustable, with a guaranteed accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

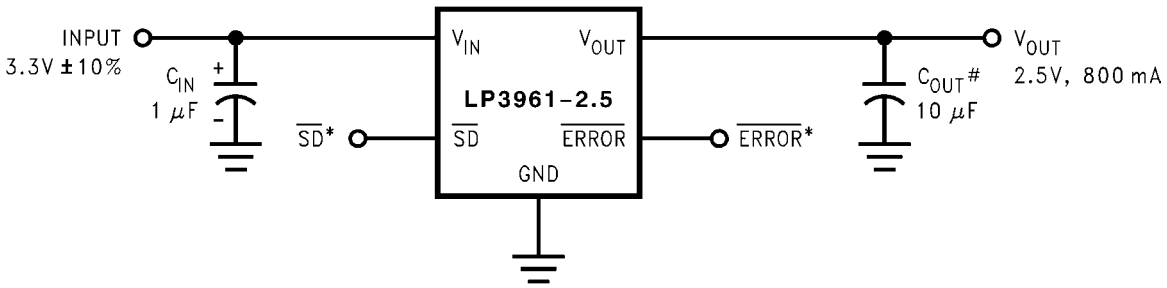
Features

- Ultra low dropout voltage
- Low ground pin current
- Load regulation of 0.02%
- 15µA quiescent current in shutdown mode
- Guaranteed output current of 0.8A DC
- Available in SOT-223,TO-263 and TO-220 packages
- Output voltage accuracy ± 1.5%
- $\overline{\text{Error}}$ flag indicates output status (LP3961)
- Sense option improves better load regulation (LP3964)
- Extremely low output capacitor requirements
- Overtemperature/overcurrent protection
- −40˚C to +125˚C junction temperature range

Applications

- Microprocessor power supplies
- GTL, GTL+, BTL, and SSTL bus terminators
- Power supplies for DSPs
- SCSI terminator
- Post regulators
- High efficiency linear regulators
- Battery chargers
- Other battery powered applications

Typical Application Circuits



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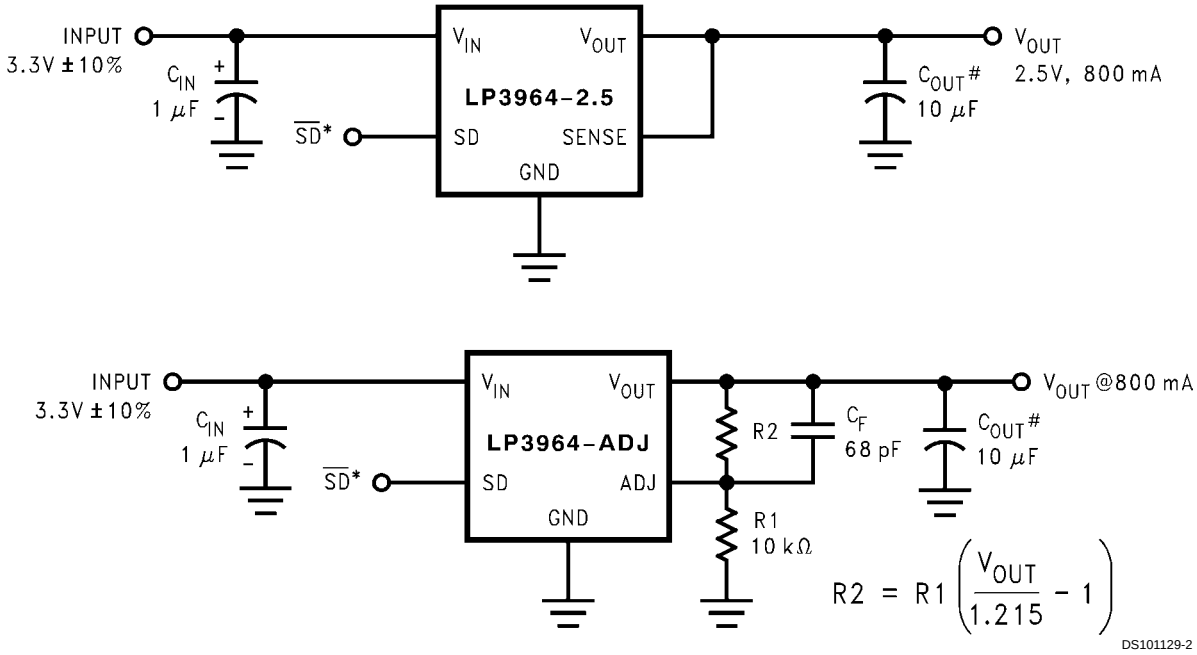
Minimum output capacitance is 10 µF to ensure stability over full load current range. More capacitance provides superior dynamic performance and additional stability margin.

*$\overline{\text{SD}}$ and $\overline{\text{ERROR}}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{\text{ERROR}}$ pin to ground if this function is not used. See applications section for more information.

Typical Application Circuits (Continued)



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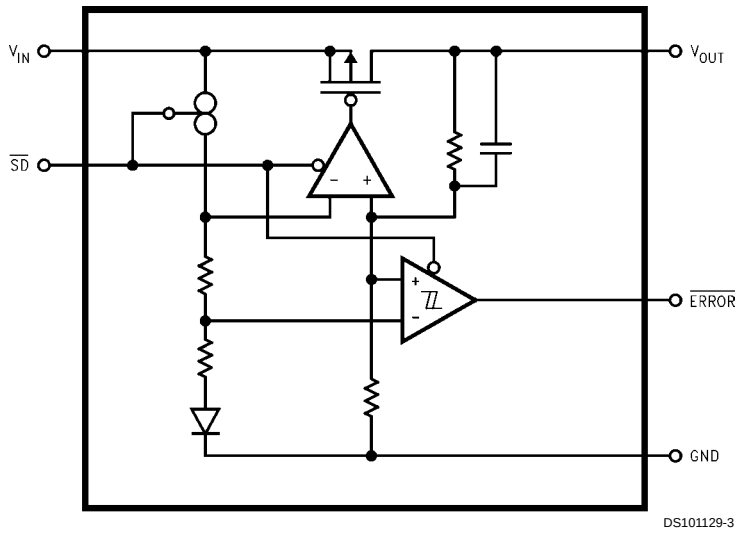
Minimum output capacitance is 10 µF to ensure stability over full load current range. More capacitance provides superior dynamic performance and additional stability margin.

*$\overline{SD}$ and $\overline{ERROR}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{ERROR}$ pin to ground if this function is not used. See applications section for more information.

Block Diagram LP3961



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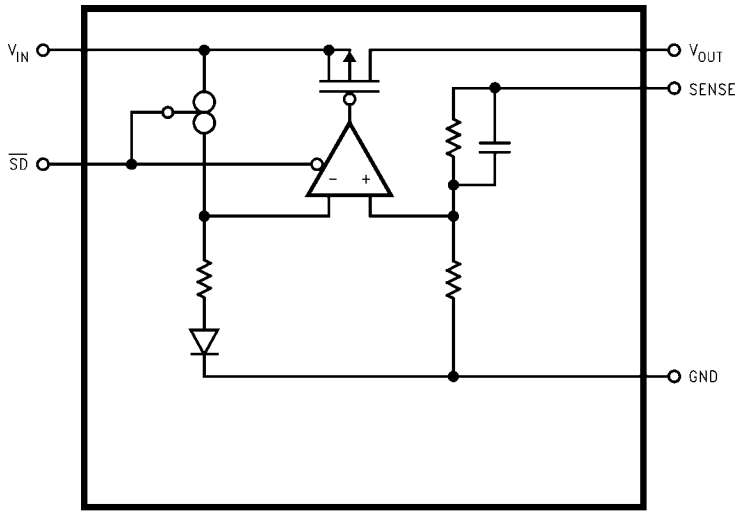
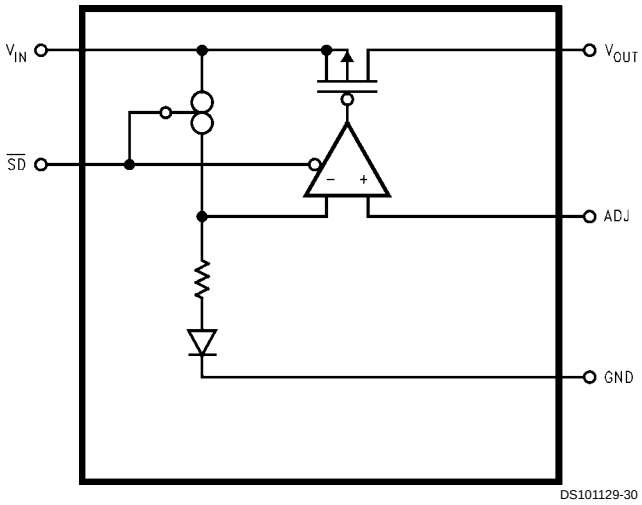
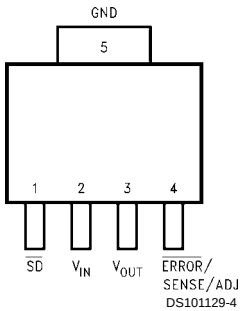
Block Diagram LP3964



Block Diagram LP3964-ADJ

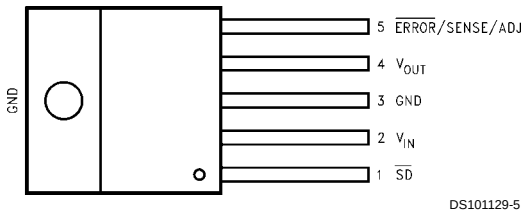


Connection Diagrams

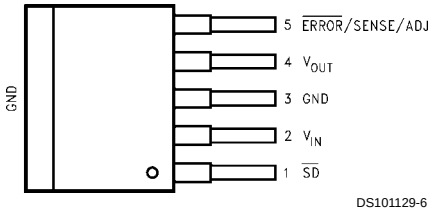


Top View
SOT 223-5 Package

Connection Diagrams (Continued)



Top View
TO220-5 Package
Bent, Staggered Leads



Top View
TO263-5 Package

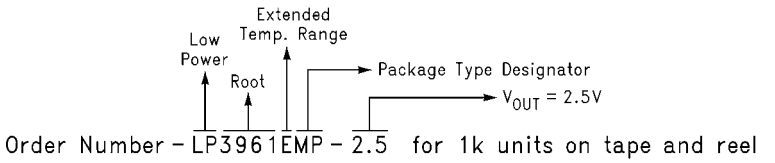
Pin Description for SOT223-5 Package

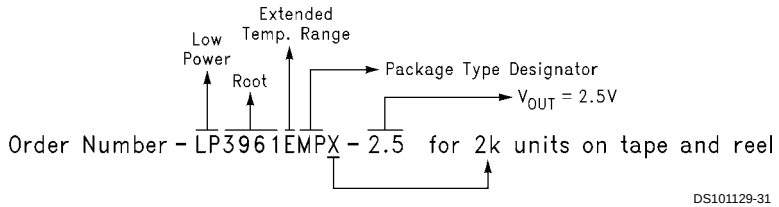
Pin #	LP3961		LP3964	
	Name	Function	Name	Function
1	$\overline{SD}$	Shutdown	$\overline{SD}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
4	$\overline{ERROR}$	$\overline{ERROR}$ Flag	SENSE/ADJ	Remote Sense Pin or output Adjust Pin
5	GND	Ground	GND	Ground

Pin Description for TO220-5 and TO263-5 Packages

Pin #	LP3961		LP3964	
	Name	Function	Name	Function
1	$\overline{SD}$	Shutdown	$\overline{SD}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	GND	Ground	GND	Ground
4	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
5	$\overline{ERROR}$	$\overline{ERROR}$ Flag	SENSE/ADJ	Remote Sense Pin or output Adjust Pin

Ordering Information





Package Type Designator is ″MP″ for SOT223 package, ″T″ for TO220 package, and ″S″ for TO263 package.

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Number	Description (Current, Option)	Package Type	Package Marking	Supplied As:
5.0	LP3961EMP-5.0	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBSB	1000 units on Tape and Reel
5.0	LP3961EMPX-5.0	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBSB	2000 units on Tape and Reel
3.3	LP3961EMP-3.3	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LAZB	1000 units on Tape and Reel
3.3	LP3961EMPX-3.3	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LAZB	2000 units on Tape and Reel
2.5	LP3961EMP-2.5	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBBB	1000 units on Tape and Reel
2.5	LP3961EMPX-2.5	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBBB	2000 units on Tape and Reel
1.8	LP3961EMP-1.8	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBAB	1000 units on Tape and Reel
1.8	LP3961EMPX-1.8	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBAB	2000 units on Tape and Reel
5.0	LP3964EMP-5.0	800mA, SENSE	SOT223-5	LBUB	1000 units on Tape and Reel
5.0	LP3964EMPX-5.0	800mA, SENSE	SOT223-5	LBUB	2000 units on Tape and Reel
3.3	LP3964EMP-3.3	800mA, SENSE	SOT223-5	LBJB	1000 units on Tape and Reel
3.3	LP3964EMPX-3.3	800mA, SENSE	SOT223-5	LBJB	2000 units on Tape and Reel
2.5	LP3964EMP-2.5	800mA, SENSE	SOT223-5	LBHB	1000 units on Tape and Reel
2.5	LP3964EMPX-2.5	800mA, SENSE	SOT223-5	LBHB	2000 units on Tape and Reel
1.8	LP3964EMP-1.8	800mA, SENSE	SOT223-5	LBFB	1000 units on Tape and Reel
1.8	LP3964EMPX-1.8	800mA, SENSE	SOT223-5	LBFB	2000 units on Tape and Reel
ADJ	LP3964EMP-ADJ	800mA, ADJ	SOT223-5	LBPB	1000 units on Tape and Reel

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage	Order Number	Description (Current, Option)	Package Type	Package Marking	Supplied As:
ADJ	LP3964EMPX-ADJ	800mA, ADJ	SOT223-5	LBPB	2000 units on Tape and Reel
5.0	LP3961ES-5.0	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-5.0	Rail
5.0	LP3961ESX-5.0	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ESX-5.0	Tape and Reel
3.3	LP3961ES-3.3	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-3.3	Rail
3.3	LP3961ESX-3.3	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-3.3	Tape and Reel
2.5	LP3961ES-2.5	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-2.5	Rail
2.5	LP3961ESX-2.5	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-2.5	Tape and Reel
1.8	LP3961ES-1.8	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-1.8	Rail
1.8	LP3961ESX-1.8	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-1.8	Tape and Reel
5.0	LP3964ES-5.0	800mA, SENSE	TO263-5	LP3964ES-5.0	Rail
5.0	LP3964ESX-5.0	800mA, SENSE	TO263-5	LP3964ES-5.0	Tape and Reel
3.3	LP3964ES-3.3	800mA, SENSE	TO263-5	LP3964ES-3.3	Rail
3.3	LP3964ESX-3.3	800mA, SENSE	TO263-5	LP3964ES-3.3	Tape and Reel
2.5	LP3964ES-2.5	800mA, SENSE	TO263-5	LP3964ES-2.5	Rail
2.5	LP3964ESX-2.5	800mA, SENSE	TO263-5	LP3964ES-2.5	Tape and Reel
1.8	LP3964ES-1.8	800mA, SENSE	TO263-5	LP3964ES-1.8	Rail
1.8	LP3964ESX-1.8	800mA, SENSE	TO263-5	LP3964ES-1.8	Tape and Reel
ADJ	LP3964ES-ADJ	800mA, ADJ	TO263-5	LP3964ES-ADJ	Rail
ADJ	LP3964ESX-ADJ	800mA, ADJ	TO263-5	LP3964ES-ADJ	Tape and Reel
5.0	LP3961ET-5.0	800mA, $\overline{\text{Error}}$ Flag	TO220-5	LP3961ET-5.0	Rail
3.3	LP3961ET-3.3	800mA, $\overline{\text{Error}}$ Flag	TO220-5	LP3961ET-3.3	Rail
2.5	LP3961ET-2.5	800mA, $\overline{\text{Error}}$ Flag	TO220-5	LP3961ET-2.5	Rail
1.8	LP3961ET-1.8	800mA, $\overline{\text{Error}}$ Flag	TO220-5	LP3961ET-1.8	Rail
5.0	LP3964ET-5.0	800mA, SENSE	TO220-5	LP3964ET-5.0	Rail
3.3	LP3964ET-3.3	800mA, SENSE	TO220-5	LP3964ET-3.3	Rail
2.5	LP3964ET-2.5	800mA, SENSE	TO220-5	LP3964ET-2.5	Rail
1.8	LP3964ET-1.8	800mA, SENSE	TO220-5	LP3964ET-1.8	Rail
ADJ	LP3964ET-ADJ	800mA, ADJ	TO220-5	LP3964ET-ADJ	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 5 sec.)	260˚C
ESD Rating (Note 3)	2 kV
Power Dissipation (Note 2)	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +7.5V
Shutdown Input Voltage (Survival)	−0.3V to V_{IN}+0.3V
Output Voltage (Survival), (Note 6), (Note 7)	−0.3V to +7.5V
I_{OUT} (Survival)	Short Circuit Protected
Maximum Voltage for $\overline{\text{ERROR}}$ Pin	V_{IN}+0.3V
Maximum Voltage for SENSE Pin	V_{OUT}+0.3V

Operating Ratings

Input Supply Voltage (Operating)	2.5V to 7.0V
Shutdown Input Voltage (Operating)	−0.3V to V_{IN}+0.3V
Maximum Operating Current (DC)	0.8A
Operating Junction Temp. Range	−40˚C to +125˚C

Electrical Characteristics LP3961/LP3964

Limits in standard typeface are for T_J = 25˚C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA, C_{OUT} =10µF, $V_{SD} = V_{IN}$-0.3V.

Symbol	Parameter	Conditions	Typ(Note 4)	LP3961/4 (Note 5)		Units
				Min	Max	
V_O	Output Voltage Tolerance (Note 8)	V_{OUT}+1V<V_{IN}<7.0V 10 mA < I_L < 800 mA	0	-1.5 **-3.0**	+1.5 **+3.0**	%
		3.135 ≤ V_{IN} ≤ 7.0 for V_{OUT} = 2.5V				
ΔV_{OL}	Output Voltage Line Regulation (Note 8)	V_{OUT}+1V<V_{IN}<7.0V,	0.02 **0.06**			%
$\Delta V_O / \Delta I_{OUT}$	Output Voltage Load Regulation (Note 8)	10 mA < I_L < 800 mA	0.02 **0.08**			%
V_{IN} - V_{OUT}	Dropout Voltage (Note 10)	I_L = 80 mA	24		30 **35**	mV
		I_L = 800 mA	240		300 **350**	
I_{GND}	Ground Pin Current In Normal Operation Mode	I_L = 80 mA	3		9 **10**	mA
		I_L = 800 mA	4		14 **15**	
I_{GND}	Ground Pin Current In Shutdown Mode (Note 11)	V_{SD} ≤ 0.2V	15		25 **75**	µA
$I_{O(PK)}$	Peak Output Current	(Note 2)	1.5	1.2 **1.1**		A
SHORT CIRCUIT PROTECTION						
I_{SC}	Short Circuit Current		2.8			A
OVER TEMPERATURE PROTECTION						
Tsh(t)	Shutdown Threshold		165			˚C
Tsh(h)	Thermal Shutdown Hysteresis		10			˚C
SHUTDOWN INPUT						
V_{SDT}	Shutdown Threshold	Output = High	V_{IN}	**V_{IN}−0.3**		V
		Output = Low	0		**0.2**	
T_{dOFF}	Turn-off delay	I_L = 800 mA	20			µs
T_{dON}	Turn-on delay	I_L = 800 mA	25			µs
I_{SD}	$\overline{\text{SD}}$ Input Current	$V_{SD} = V_{IN}$	1			nA

Electrical Characteristics
LP3961/LP3964 (Continued)

Limits in standard typeface are for T_J = 25˚C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA, C_{OUT} =10µF, $V_{SD} = V_{IN}$-0.3V.

Symbol	Parameter	Conditions	Typ(Note 4)	LP3961/4 (Note 5)		Units
				Min	Max	
ERROR FLAG COMPARATOR						
V_T	Threshold	(Note 9)	10	**5**	**16**	%
V_{TH}	Threshold Hysteresis	(Note 9)	5	**2**	**8**	%
$V_{EF(Sat)}$	$\overline{\text{Error}}$ Flag Saturation	I_{sink} = 100µA	0.02		**0.1**	V
Td	Flag Reset Delay		1			µs
I_{lk}	$\overline{\text{Error}}$ Flag Pin Leakage Current		1			nA
I_{max}	$\overline{\text{Error}}$ Flag Pin Sink Current	V_{Error} = **0.5V** (over temp.)	1			mA
AC PARAMETERS						
PSRR	Ripple Rejection	$V_{IN} = V_{OUT}$ + 1.5V C_{OUT} = 100uF V_{OUT} = 3.3V	60			dB
		$V_{IN} = V_{OUT}$ + 0.3V C_{OUT} = 100uF V_{OUT} = 3.3V	40			
$\rho_{n(l/f}$	Output Noise Density	f = 120Hz	0.8			µV
e_n	Output Noise Voltage (rms)	BW = 10Hz – 100kHz	150			µV (rms)
		BW = 300Hz – 300kHz	100			

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Charateristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO220 package must be derated at θ_{jA} = 50˚C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the TO263 surface-mount package must be derated at θ_{jA} = 60˚C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient. The devices in SOT223 package must be derated at θ_{jA} = 90˚C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient.

Note 3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Note 4: Typical numbers are at 25˚C and represent the most likely parametric norm.

Note 5: Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 6: If used in a dual-supply system where the regulator load is returned to a negative supply, the LP396X output must be diode-clamped to ground.

Note 7: The output PMOS structure contains a diode between the V_{IN} and V_{OUT} terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200mA of DC current and 1Amp of peak current.

Note 8: Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

Note 9: $\overline{\text{Error}}$ Flag threshold and hysteresis are specified as percentage of regulated output voltage.

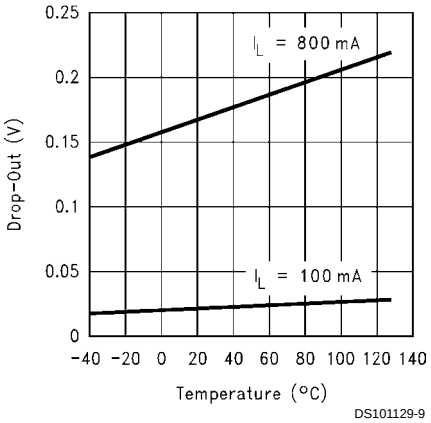
Note 10: Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V.

Note 11: This specification has been tested for −40˚C ≤ T_J ≤ 85˚C since the temperature rise of the device is negligible under shutdown conditions.

Typical Performance Characteristics

Unless otherwise specified, V_{IN} =$V_{O(NOM)}$ + 1V, V_{OUT}= 2.5V, C_{OUT} =10µF, I_{OUT} = 10mA, C_{IN} =10µF, V_{SD} = V_{IN}, and T_A = 25˚C.

Drop-Out Voltage Vs Temperature for Different Load Currents



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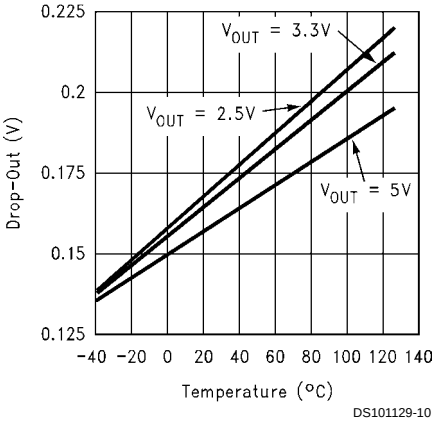
Drop-Out Voltage Vs Temperature for Different Output Voltages (I_{OUT} = 800mA)



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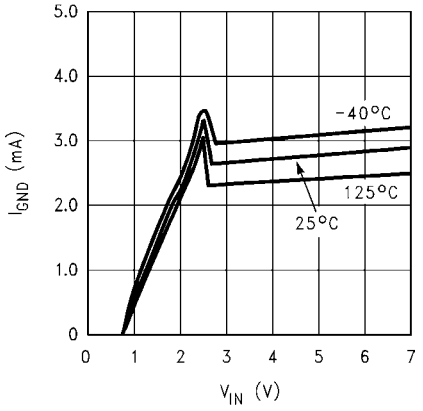
Ground Pin Current Vs Input Voltage (V_{SD}=V_{IN})



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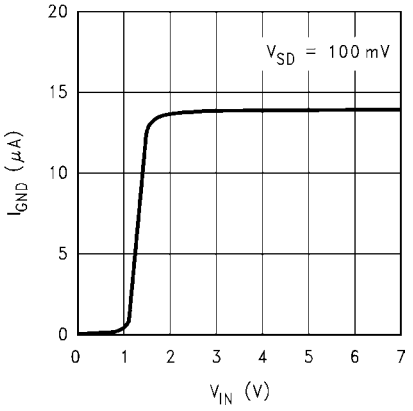
Ground Pin Current Vs Input Voltage (V_{SD}=100mV)



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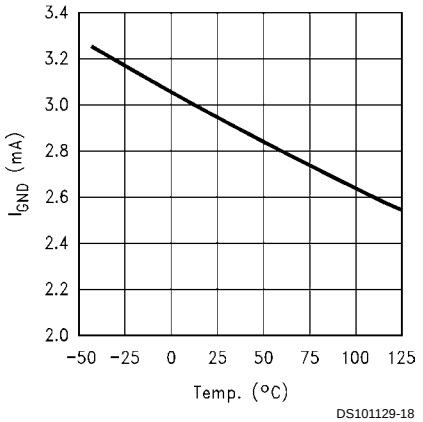
Ground Current Vs Temperature (V_{SD}=V_{IN})



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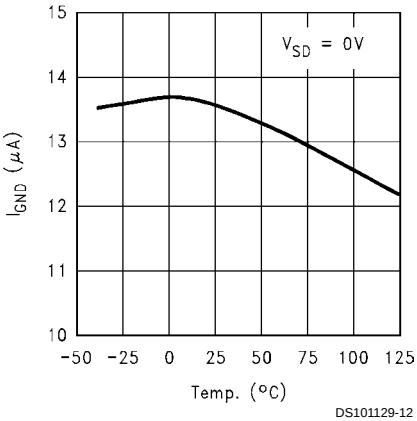
Ground Current Vs Temperature (V_{SD}=0V



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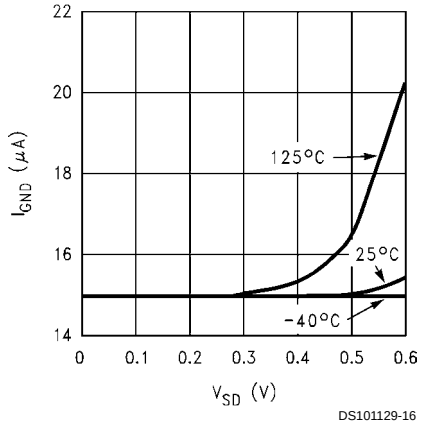
Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 2.5V$, $C_{OUT} = 10\mu F$, $I_{OUT} = 10mA$, $C_{IN} = 10\mu F$, $V_{SD} = V_{IN}$, and $T_A = 25^{\circ}C$. (Continued)

Ground Pin Current Vs Shutdown Pin Voltage



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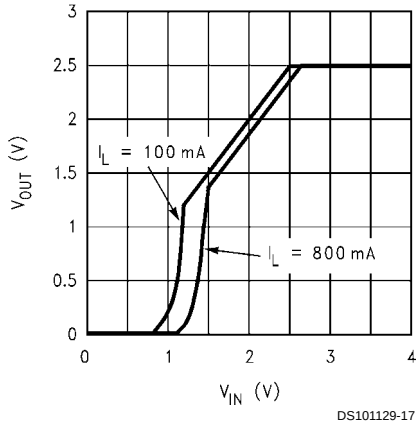
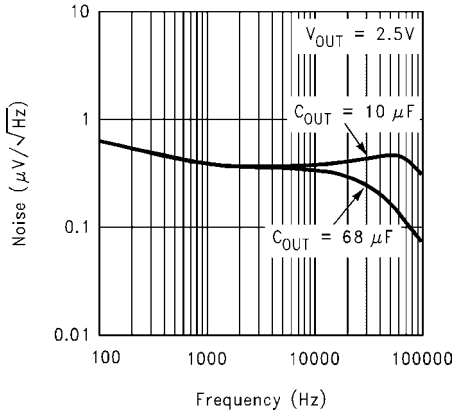
Input Voltage Vs Output Voltage



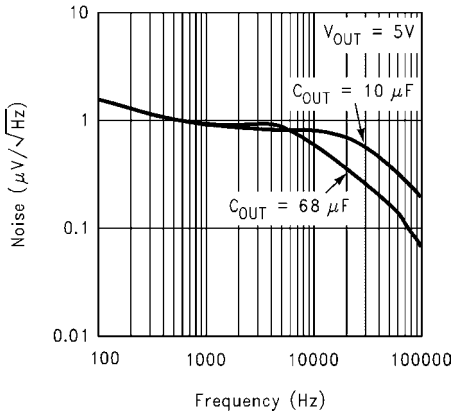
DS101129-17

Output Noise Density, V_{OUT}= 2.5V



DS101129-13

Output Noise Density, V_{OUT}= 5V



DS101129-14

Applications Information

Input Capacitor Selection

The LP3961 and LP3964 require a minimum input capacitance of 10µF between the input and ground pins to prevent any impedance interactions with the supply. This capacitor should be located very close to the V_{IN} pin. This capacitor can be of any type such as ceramic, tantalum, or aluminium. Any good quality capacitor which has good tolerance over temperature and frequency is recommended.

Output Capacitor Selection

The LP3961 and LP3964 require a minimum of 10µF capacitance between the output and ground pins for proper operation. LP3961 and LP3964 work best with Tantalum or Electrolytic capacitor. The output capacitor should have a good tolerance over temperature, voltage, and frequency. Larger capacitance provides better improved load dynamics and noise performance. The output capacitor should be connected very close to the Vout pin.

Output Adjustment

An adjustable output device has output voltage range of 1.215V to 5.1V. To obtain a desired output voltage, the following equation can be used with R1 always a 10kΩ resistor.

$$R2 = R1\left(\frac{V_{OUT}}{1.215} - 1\right)$$

For output stability, C_F must be between 68pF and 100pF.

Output Noise

Noise is specified in two ways-

Spot Noise or **Output noise density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Total output Noise or **Broad-band noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/√Hz or nV/√Hz and total output noise is measured in µV(rms).

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP3961/LP3964 achieves low noise performance and low quiescent current operation.

The total output noise specification for LP3961/LP3964 is presented in the Electrical Characteristics table. The Output noise density at different frequencies is represented by a curve under typical performance characteristics.

Short-Circuit Protection

The LP3961and LP3964 is short circuit protected and in the event of a peak over-current condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the section on thermal information for power dissipation calculations.

$\overline{\text{Error}}$ Flag Operation

The LP3961/LP3964 produces a logic low signal at the $\overline{\text{Error}}$ Flag pin when the output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The timing diagram in *Figure 1* shows the relationship between the $\overline{\text{ERROR}}$ and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the Error Flag.

The internal $\overline{\text{Error}}$ flag comparator has an open drain output stage. Hence, the $\overline{\text{ERROR}}$ pin should be pulled high through a pull up resistor. Although the $\overline{\text{ERROR}}$ pin can sink current of 1mA, this current is energy drain from the input supply. Hence, the value of the pull up resistor should be in the range of 100kΩ to 1MΩ. **The $\overline{\text{ERROR}}$ pin must be connected to ground if this function is not used.** It should also be noted that when the shutdown pin is pulled low, the $\overline{\text{ERROR}}$ pin is forced to be invalid for reasons of saving power in shutdown mode.

Applications Information (Continued)

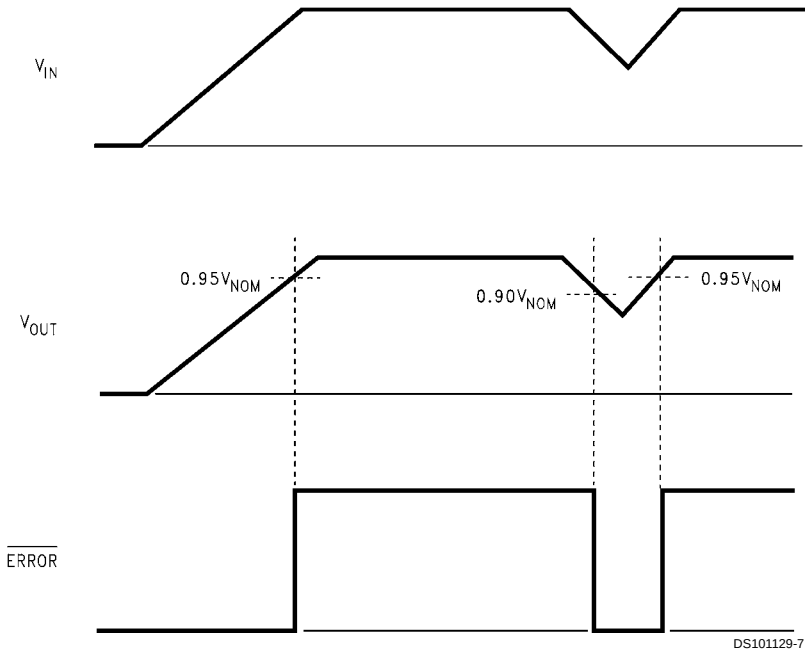


FIGURE 1. $\overline{\text{Error}}$ Flag Operation

Sense Pin

In applications where the regulator output is not very close to the load, LP3964 can provide better remote load regulation using the SENSE pin. *Figure 2* depicts the advantage of the SENSE option. LP3961 regulates the voltage at the output pin. Hence, the voltage at the remote load will be the regulator output voltage minus the drop across the trace resistance. For example, in the case of a 3.3V output, if the trace resistance is 100mΩ, the voltage at the remote load will be 3.22V with 800mAmps of load current, I_{LOAD}. The LP3964 regulates the voltage at the sense pin. Connecting the sense pin to the remote load will provide regulation at the remote load, as shown in *Figure 2*. If the sense option pin is not required, the sense pin must be connected to the V_{OUT} pin.

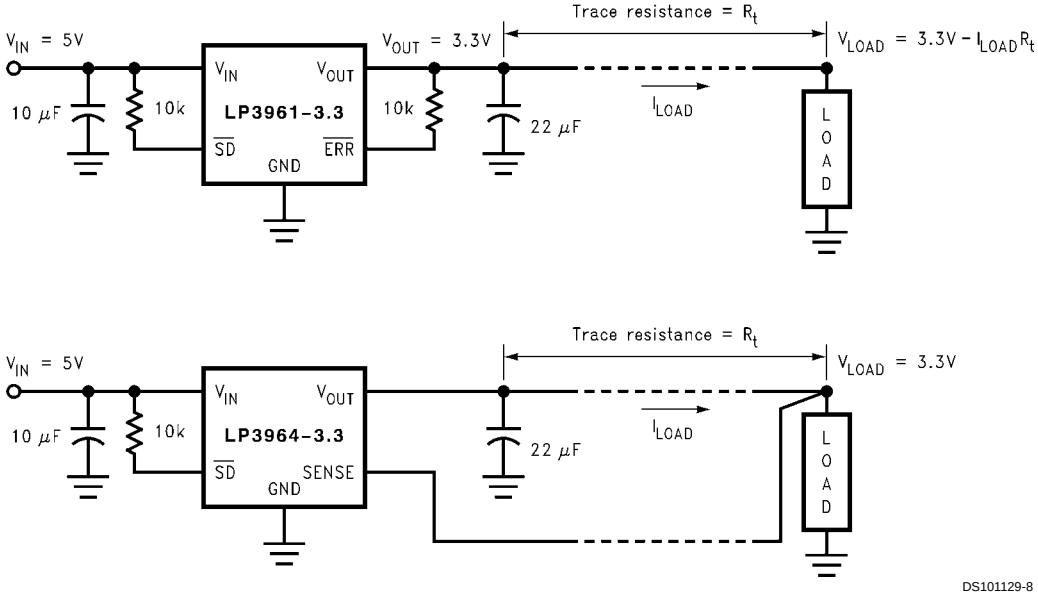


FIGURE 2. Improving remote load regulation using LP3964

Shutdown Operation

A CMOS Logic level signal at the shutdown ($\overline{SD}$) pin will turn-off the regulator. Pin $\overline{SD}$ must be actively terminated through a 10kΩ pull-up resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

Applications Information (Continued)

Dropout Voltage

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the output voltage. The LP3961/LP3964 use an internal MOSFET with an Rds(on) of 240mΩ (typically). For CMOS LDOs, the dropout voltage is the product of the load current and the Rds(on) of the internal MOSFET.

Reverse Current Path

The internal MOSFET in LP3961and LP3964 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200mA continuous and 1A peak.

Maximum Output Current Capability

LP3961 and LP3964 can deliver a continuous current of 800mA over the full operating temperature range. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$P_D = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN})I_{GND}$

where I_{GND} is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature($T_{J\text{-}max}$):

$T_{Rmax} = T_{Jmax} - T_{Amax}$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$\theta_{JA} = T_{Rmax} / P_D$

LP3961 and LP3964 are available in TO-220, TO-263, and SOT-223 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 60 °C/W for TO-220 package, ≥60 °C/W for TO-263 package, and ≥ 140 °C/W for SOT-223 package, no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

Heatsinking TO-220 Packages

The thermal resistance of a TO220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for TO263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$\theta_{HA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC}$.

In this equation, θ_{CH} is the thermal resistance from the junction to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. θ_{JC} is about 3°C/W for a TO220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

Heatsinking TO-263 and SOT-223 Packages

The TO-263 and SOT223 packages use the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. *Figure 3* shows a curve for the θ_{JA} of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

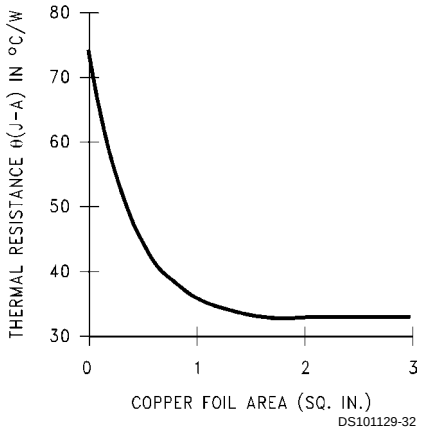


FIGURE 3. θ_{JA} vs Copper(1 Ounce) Area for TO-263 package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the TO-263 packag mounted to a PCB is 32°C/W.

Figure 4 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

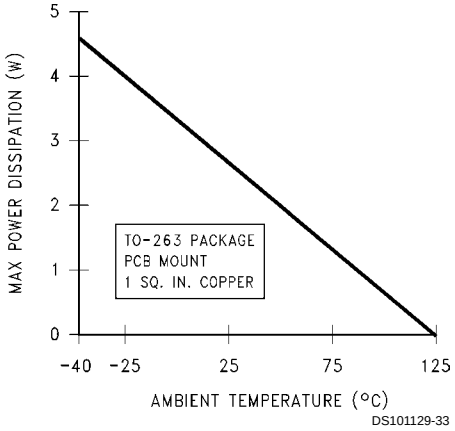


FIGURE 4. Maximum power dissipation vs ambient temperature for TO-263 package

Figure 5 shows a curve for the θ_{JA} of SOT-223 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

Applications Information (Continued)

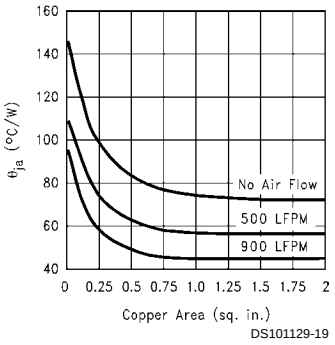


FIGURE 5. θ_{JA} vs Copper(1 Ounce) Area for SOT-223 package

The following figures show different layout scenarios for SOT-223 package.

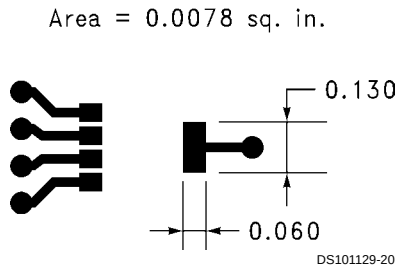


FIGURE 6. SCENARIO A, θ_{JA} = 148˚C/W

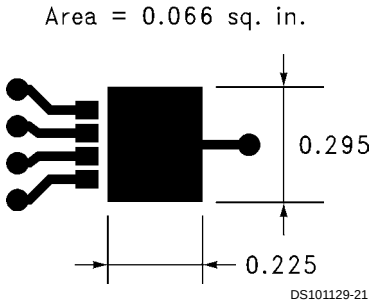


FIGURE 7. SCENARIO B, θ_{JA} = 125˚C/W

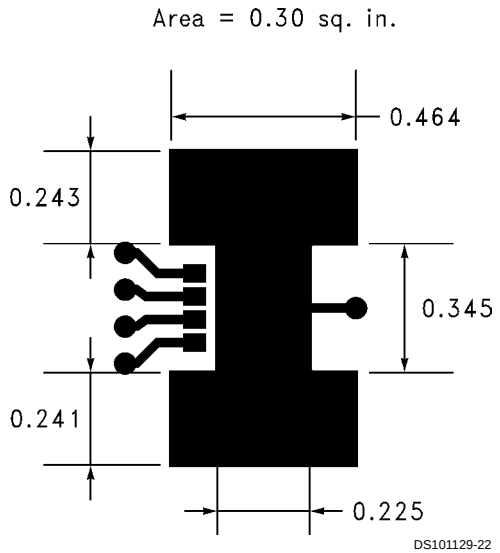


FIGURE 8. SCENARIO C, θ_{JA} = 92˚C/W

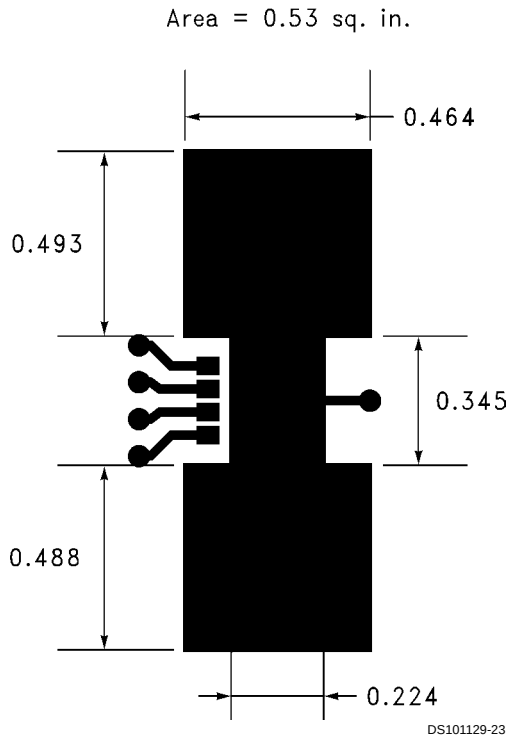


FIGURE 9. SCENARIO D, θ_{JA} = 83˚C/W

Applications Information (Continued)

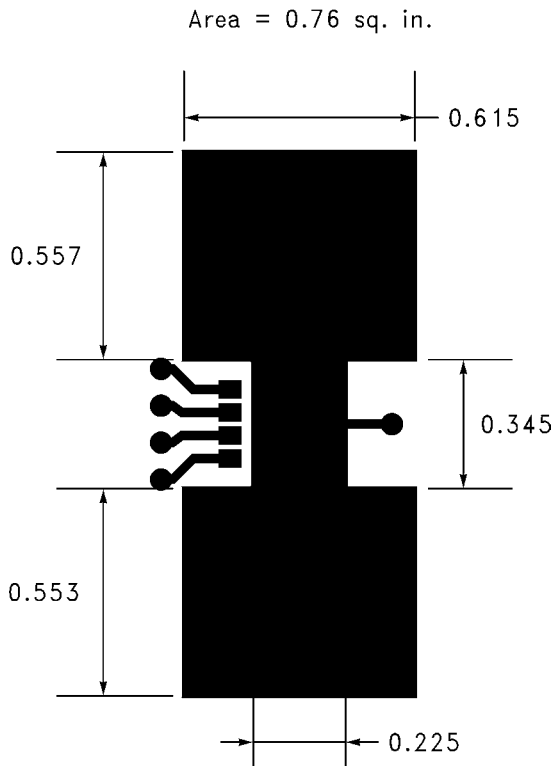


FIGURE 10. SCENARIO E, θ_{JA} = 77˚C/W

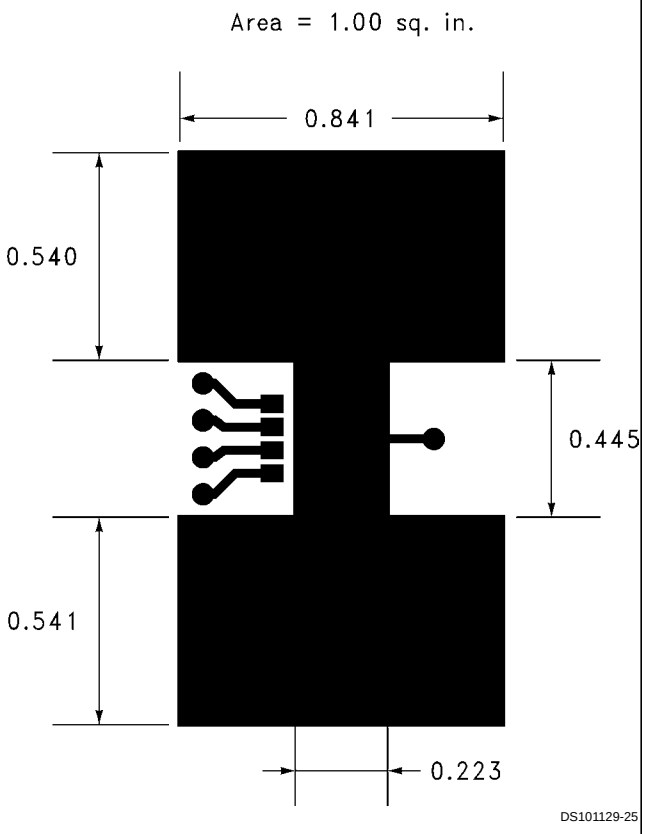


FIGURE 11. SCENARIO F, θ_{JA} = 75˚C/W

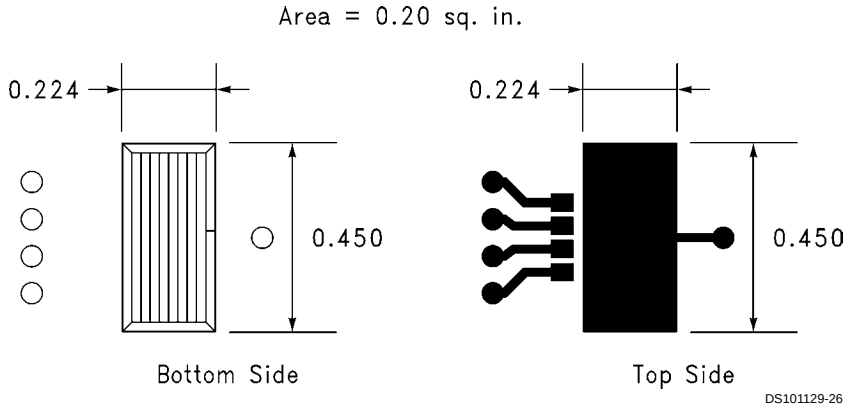


FIGURE 12. SCENARIO G, θ_{JA} = 113˚C/W

Applications Information (Continued)

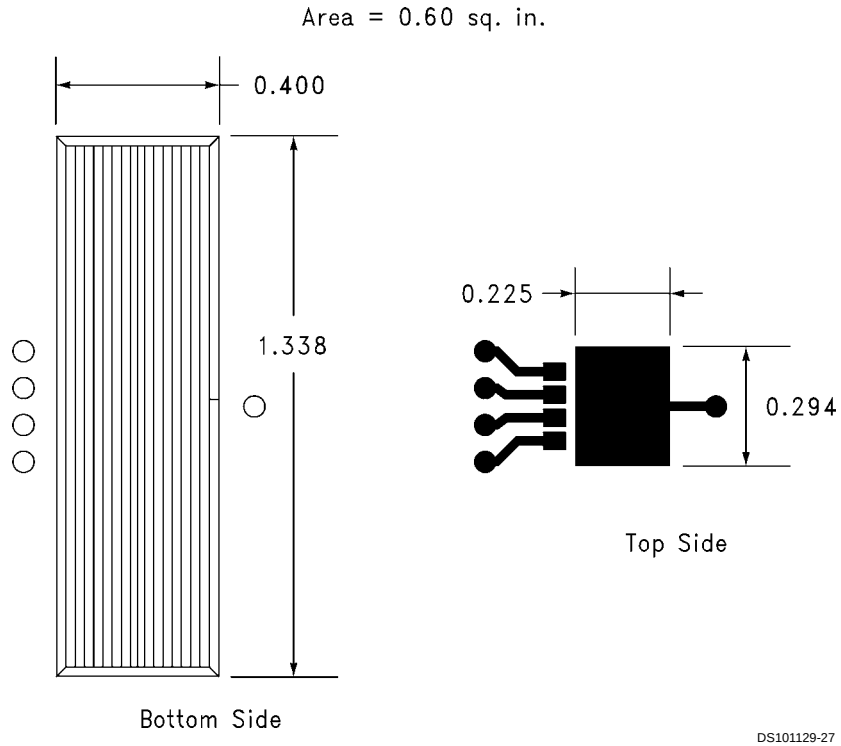


FIGURE 13. SCENARIO H, θ_{JA} = 79˚C/W

Applications Information (Continued)

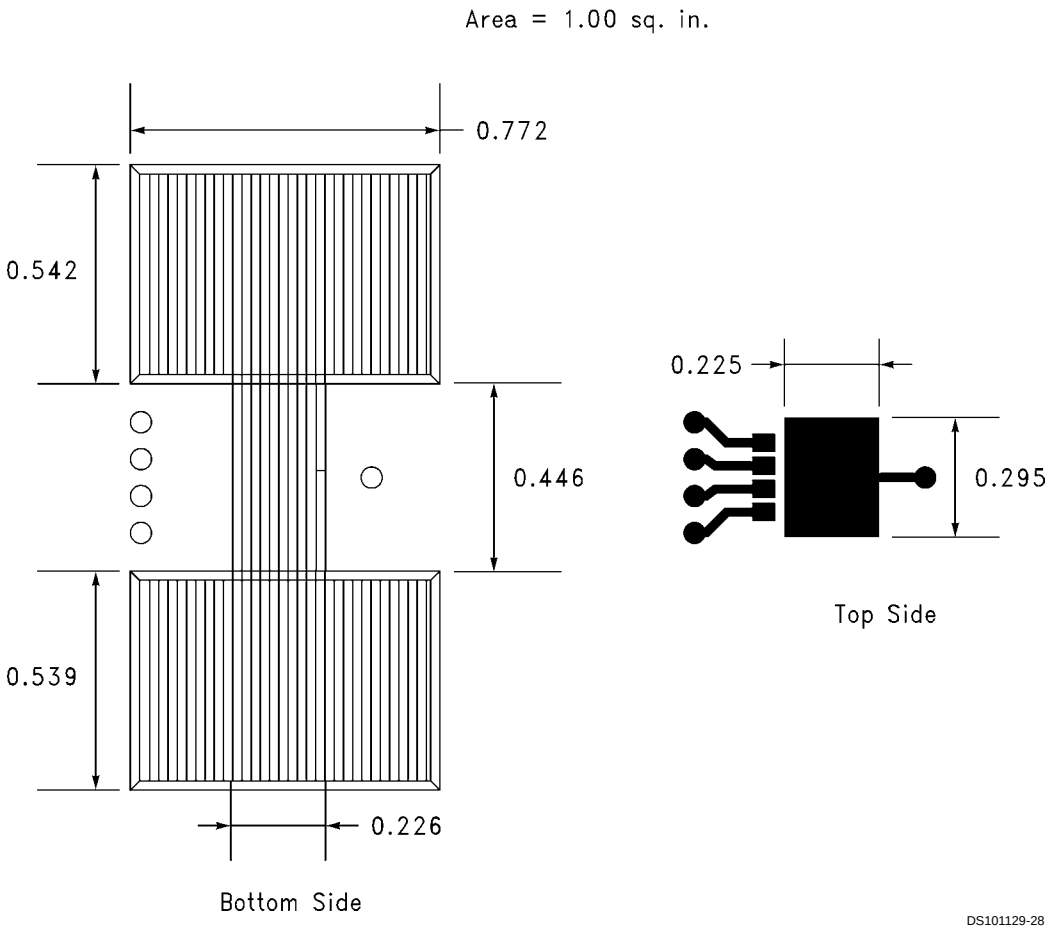
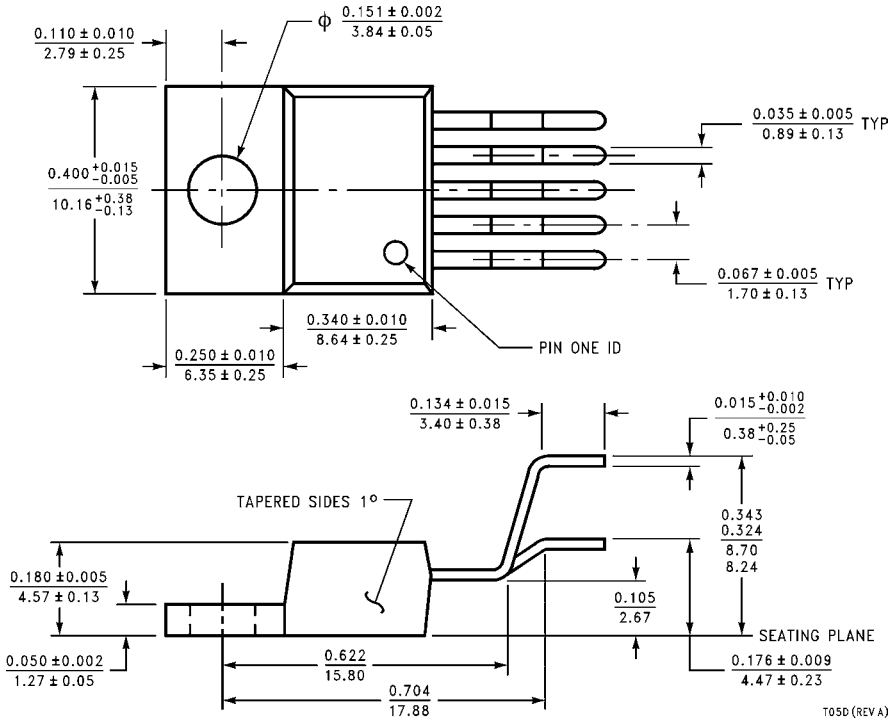


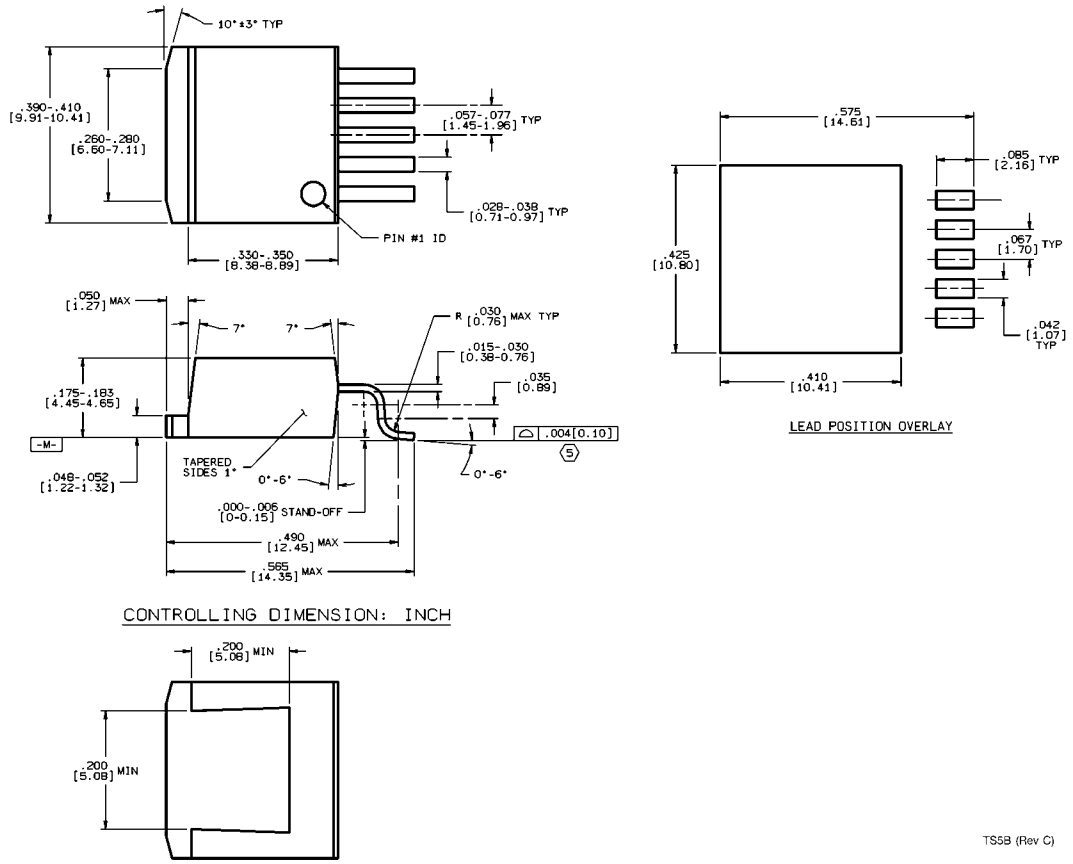
FIGURE 14. SCENARIO I, θ_{JA} = 78.5˚C/W

Physical Dimensions inches (millimeters) unless otherwise noted



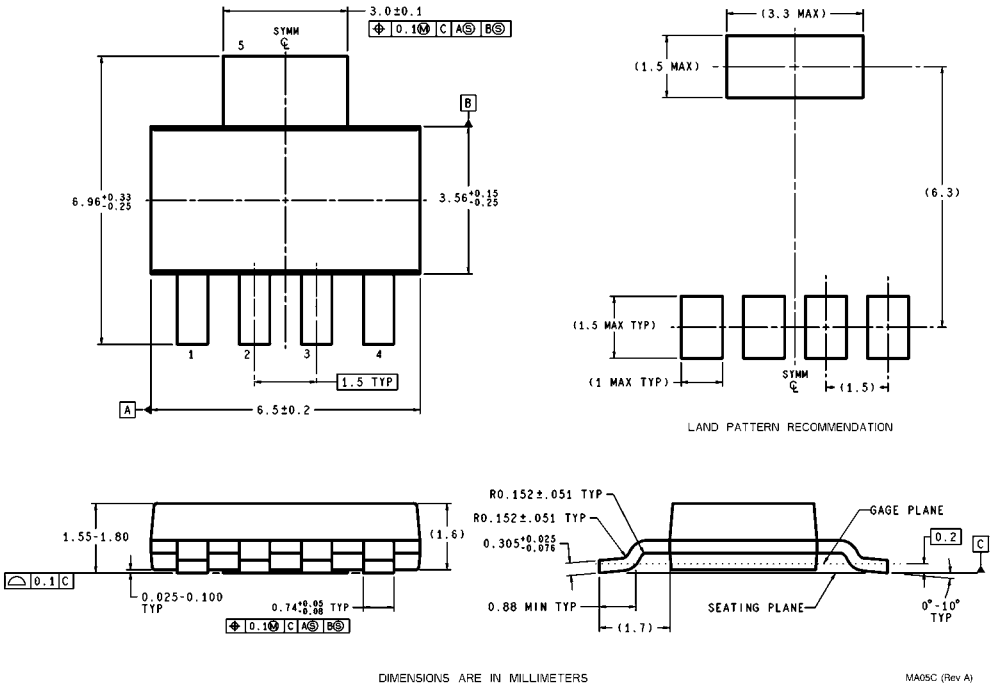
TO220 5-lead, Molded, Stagger Bend Package (TO220-5)
NS Package Number T05D
For Order Numbers, refer to the "Ordering Information" section of this document.

Physical Dimensions inches (millimeters) unless otherwise noted



TO263 5-Lead, Molded, Surface Mount Package (TO263-5)
NS Package Number TS5B
For Order Numbers, refer to the “Ordering Information” section of this document.

Physical Dimensions inches (millimeters) unless otherwise noted



SOT223, 5-Lead, Molded, Surface Mount Package (SOT223-5)
NS Package Number MA05C
For Order Numbers, refer to the "Ordering Information" section of this document.

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National Semiconductor Asia Pacific Customer Response Group
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