

# LM148/LM248/LM348 Quad 741 Op Amps

### **General Description**

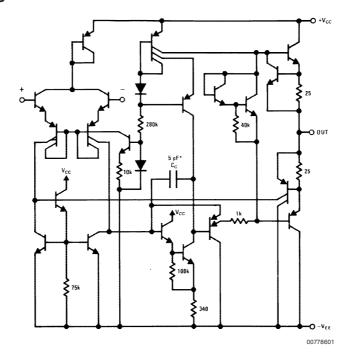
The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required. For lower power refer to LF444.

#### **Features**

- 741 op amp operating characteristics
- Class AB output stage no crossover distortion
- Pin compatible with the LM124
- Overload protection for inputs and outputs
- Low supply current drain: 0.6 mA/Amplifier
   Low input offset voltage: 1 mV
   Low input offset current: 4 nA
   Low input bias current 30 nA
- High degree of isolation between amplifiers: 120 dB
- Gain bandwidth product
- LM148 (unity gain): 1.0 MHz

### **Schematic Diagram**



\* 1 pF in the LM149

## **Absolute Maximum Ratings** (Note 4)

Distributors for availability and specifications.

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/

	LM148	LM248	LM348		
Supply Voltage	±22V	±18V	±18V		
Differential Input Voltage	±44V	±36V	±36V		
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous		
Power Dissipation (P <sub>d</sub> at 25°C) and					
Thermal Resistance $(\theta_{jA})$ , (Note 2)					
Molded DIP (N) P <sub>d</sub>	_	_	750 mW		
$ heta_{jA}$	_	_	100°C/W		
Cavity DIP (J) P <sub>d</sub>	1100 mW	800 mW	700 mW		
$ heta_{\sf JA}$	110°C/W	110°C/W	110°C/W		
Maximum Junction Temperature (T <sub>jMAX</sub> )	150°C	110°C	100°C		
Operating Temperature Range	$-55^{\circ}C \le T_A \le +125^{\circ}C$	$-25^{\circ}\text{C} \le \text{T}_{\text{A}} \le +85^{\circ}\text{C}$	$0^{\circ}C \le T_A \le +70^{\circ}C$		
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C		
Lead Temperature (Soldering, 10 sec.) Ceramic	300°C	300°C	300°C		
Lead Temperature (Soldering, 10 sec.) Plastic			260°C		
Soldering Information					
Dual-In-Line Package					
Soldering (10 seconds)	260°C	260°C	260°C		
Small Outline Package					
Vapor Phase (60 seconds)	215°C	215°C	215°C		
Infrared (15 seconds)	220°C	220°C	220°C		
See AN-450 "Surface Mounting Methods and Their I	Effect on Product Reliability	" for other methods of s	oldering surface		

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount

devices.

ESD tolerance (Note 5) 500V 500V

### **Electrical Characteristics**

(Note 3)

Parameter	Conditions	LM148			LM248			LM348			Units
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Input Offset Voltage	$T_A = 25^{\circ}C, R_S \le 10 \text{ k}\Omega$		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	T <sub>A</sub> = 25°C		4	25		4	50		4	50	nA
Input Bias Current	T <sub>A</sub> = 25°C		30	100		30	200		30	200	nA
Input Resistance	T <sub>A</sub> = 25°C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = 25^{\circ}C, V_S = \pm 15V$		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = 25^{\circ}C, V_S = \pm 15V$	50	160		25	160		25	160		V/mV
	$V_{OUT} = \pm 10V, R_L \ge 2 \text{ k}\Omega$										
Amplifier to Amplifier	$T_A = 25^{\circ}C$ , $f = 1 \text{ Hz to } 20 \text{ kHz}$										
Coupling	(Input Referred) See Crosstalk		-120			-120			-120		dB
	Test Circuit										
Small Signal Bandwidth	T <sub>A</sub> = 25°C,		1.0			1.0			1.0		MHz
	LM148 Series										
Phase Margin	T <sub>A</sub> = 25°C,		60			60			60		degrees
	LM148 Series (A <sub>V</sub> = 1)										
Slew Rate	$T_A = 25^{\circ}C$ ,		0.5			0.5			0.5		V/µs
	LM148 Series $(A_V = 1)$										
Output Short Circuit Current	$T_A = 25^{\circ}C$		25			25			25		mA
Input Offset Voltage	$R_S \le 10 \text{ k}\Omega$			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA

## **Electrical Characteristics** (Continued)

(Note 3)

Parameter	Conditions	LM148				LM248		LM348			Units
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Input Bias Current				325			500			400	nA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V,$	25			15			15			V/mV
	$R_L > 2 k\Omega$										
Output Voltage Swing	$V_{S} = \pm 15V, R_{L} = 10 \text{ k}\Omega$	±12	±13		±12	±13		±12	±13		V
	$R_L = 2 k\Omega$	±10	±12		±10	±12		±10	±12		V
Input Voltage Range	V <sub>S</sub> = ±15V	±12			±12			±12			V
Common-Mode Rejection	$R_S \le 10 \text{ k}\Omega$	70	90		70	90		70	90		dB
Ratio											
Supply Voltage Rejection	$R_S \le 10 \text{ k}\Omega, \pm 5\text{V} \le V_S \le \pm 15\text{V}$	77	96		77	96		77	96		dB

Note 1: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

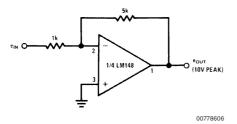
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dicated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum available power dissipation at any temperature is  $P_d = (T_{JMAX} - T_A)/\theta_{JA}$  or the 25°C  $P_{DMAX}$ , whichever is less.

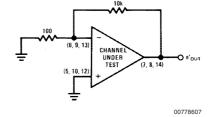
Note 3: These specifications apply for  $V_S = \pm 15V$  and over the absolute maximum operating temperature range  $(T_L \le T_A \le T_H)$  unless otherwise noted.

Note 4: Refer to RETS 148X for LM148 military specifications.

Note 5: Human body model, 1.5 k $\Omega$  in series with 100 pF.

## Cross Talk Test Circuit V<sub>S</sub> = ±15V





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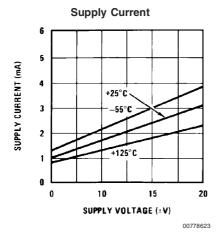
POSITIVE SUPPLY VOLTAGE (V)

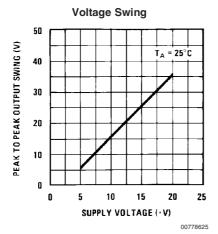
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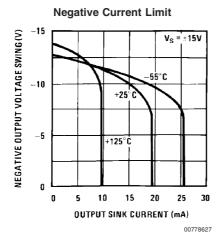
20

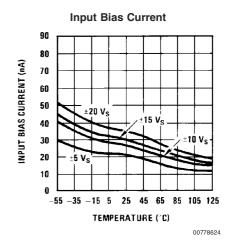
15

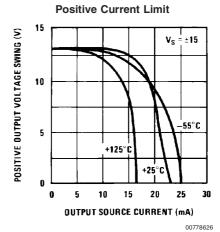
# **Typical Performance Characteristics**

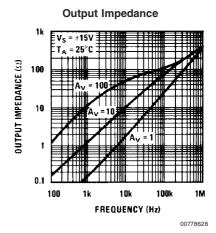






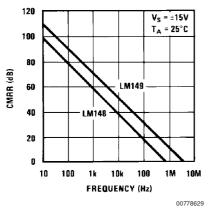




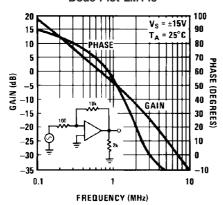


## **Typical Performance Characteristics** (Continued)



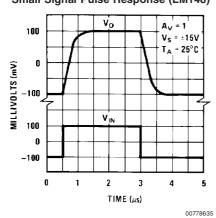


#### **Bode Plot LM148**

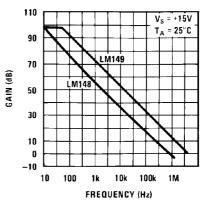


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### Small Signal Pulse Response (LM148)

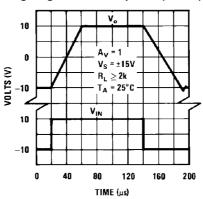


**Open Loop Frequency Response** 



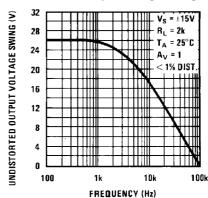
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#### Large Signal Pulse Response (LM148)

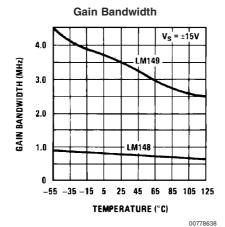


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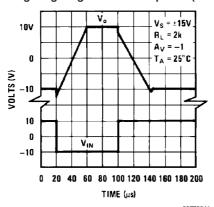
#### **Undistorted Output Voltage Swing**



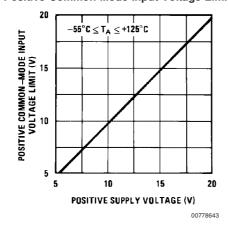
## Typical Performance Characteristics (Continued)

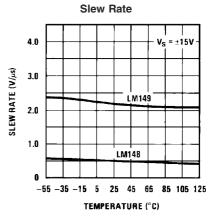


Inverting Large Signal Pulse Response (LM148)



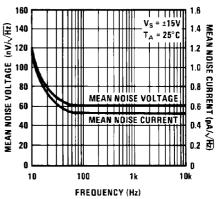
Positive Common-Mode Input Voltage Limit





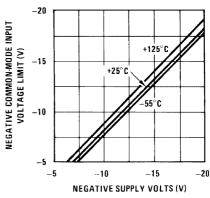
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Input Noise Voltage and Noise Current



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Negative Common-Mode Input Voltage Limit



## **Application Hints**

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

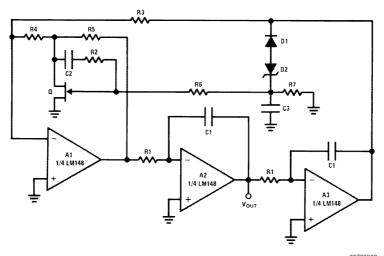
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

### Typical Applications—LM148

#### One Decade Low Distortion Sinewave Generator



$$f = \frac{1}{2\pi R1C1} \times \sqrt{K}, \, K = \frac{R4R5}{R3} \left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right), \quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right) \frac{1}{2}}$$

 $f_{MAX} = 5 \text{ kHz}, \text{ THD} \le 0.03\%$ 

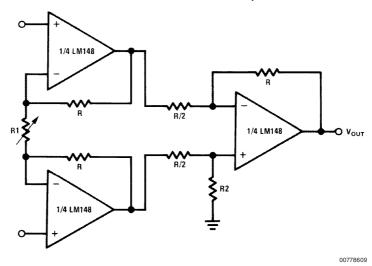
R1 = 100k pot. C1 = 0.0047  $\mu F,~C2$  = 0.01  $\mu F,~C3$  = 0.1  $\mu F,~R2$  = R6 = R7 = 1M,

R3 = 5.1k, R4 = 12 $\Omega,\,R5$  = 240 $\Omega,\,Q$  = NS5102, D1 = 1N914, D2 = 3.6V avalanche

diode (ex. LM103),  $V_S = \pm 15V$ 

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

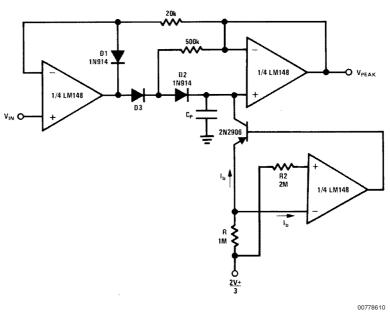
#### Low Cost Instrumentation Amplifier



 $V_{OUT} = 2\left(\frac{2R}{R1} + 1\right), V_{\overline{S}} - 3V \le V_{IN\,CM} \le {V_S}^+ - 3V,$ 

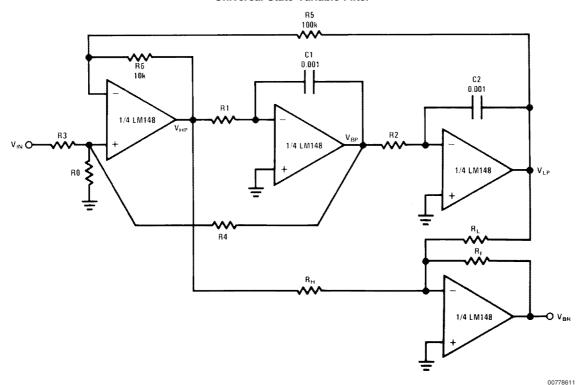
 $V_S = \pm 15V$ R = R2, trim R2 to boost CMRR

#### Low Drift Peak Detector with Bias Current Compensation



Adjust R for minimum drift D3 low leakage diode D1 added to improve speed  $V_S = \pm 15V$ 

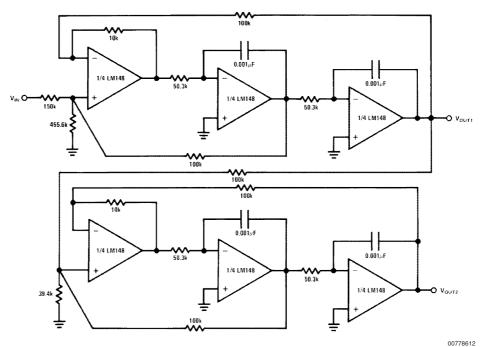
#### Universal State-Variable Filter



Tune Q through R0, For predictable results:  $f_Q Q \le 4 \times 10^4$  Use Band Pass output to tune for Q

$$\begin{split} &\frac{V_{(s)}}{V_{IN(s)}} = \frac{N_{(s)}}{D_{(s)}}, \; D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o^2 \\ &N_{HP(s)} = S^2 \, H_{OHP}, \; N_{BP(s)} = \frac{-s\omega_O \, H_{OBP}}{Q} \quad N_{LP} = \omega_o^2 \, H_{OLP}. \\ &f_o = \frac{1}{2\pi} \, \sqrt{\frac{R6}{R5}} \, \sqrt{\frac{1}{1112}}, \; t_i = R_i C_i, \; Q = \left(\frac{1 \, + \, R4 |R3 \, + \, R4 |R0}{1 \, + \, R6 |R5}\right) \left(\frac{R6}{R5} \frac{t_1}{t_2}\right)^{\frac{1}{2}} \\ &f_{NOTCH} = \frac{1}{2\pi} \left(\frac{R_H}{R_L \, t_1 \, t_2}\right)^{\frac{1}{2}}, \; H_{OHP} = \frac{1 \, + \, R6 |R5}{1 \, + \, R3 |R0 \, + \, R3 |R4}, \; H_{OBP} = \frac{1 \, + \, R4 |R3 \, + \, R4 |R0}{1 \, + \, R3 |R0 \, + \, R3 |R4} \\ &H_{OLP} = \frac{1 \, + \, R5 |R6}{1 \, + \, R3 |R0 \, + \, R3 |R4} \end{split}$$

#### A 1 kHz 4 Pole Butterworth

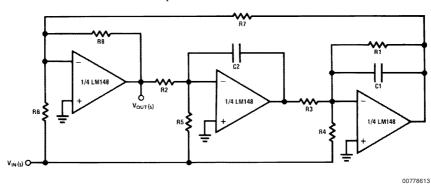


Use general equations, and tune each section separately

 $Q_{1stSECTION} = 0.541, \ Q_{2ndSECTION} = 1.306$ 

The response should have 0 dB peaking

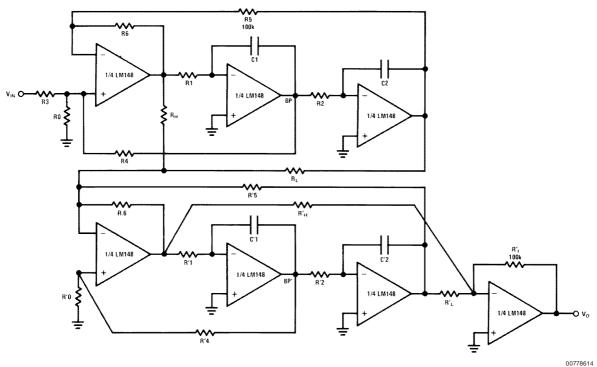
#### A 3 Amplifier Bi-Quad Notch Filter



$$\label{eq:Q} Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}}, \ \ f_0 = \frac{1}{2\pi} \sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}}, \ \ f_{NOTCH} = \frac{1}{2\pi} \sqrt{\frac{R6}{R3R5R7C1C2}}$$
 Necessary condition for notch: 
$$\frac{1}{R6} = \frac{R1}{R4R7}$$

Ex:  $f_{NOTCH} = 3$  kHz, Q = 5, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001  $\mu$ F Better noise performance than the state-space approach.

#### A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)



R1C1 = R2C2 = t

R'1C'1 = R'2C'2 = t'

 $f_{C}=1\ \text{kHz},\ f_{S}=2\ \text{kHz},\ f_{p}=0.543,\ f_{Z}=2.14,\ Q=0.841,\ f'_{P}=0.987,\ f'_{Z}=4.92,\ Q'=4.403,\ \text{normalized to ripple BW}$ 

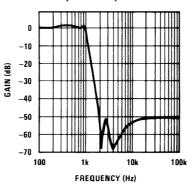
$$f = \frac{1}{2\pi R1C1} \times \sqrt{K}, K = \frac{R4R5}{R3} \left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right), \quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_D}\right)^{1/2}}$$

Use the BP outputs to tune Q, Q', tune the 2 sections separately

 $R1 = R2 = 92.6k, \ R3 = R4 = R5 = 100k, \ R6 = 10k, \ R0 = 107.8k, \ R_L = 100k, \ R_H = 155.1k,$ 

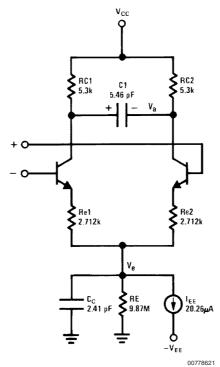
 $R'1 = R'2 = 50.9k, \;\; R'4 = R'5 = 100k, \;\; R'6 = 10k, \;\; R'0 = 5.78k, \;\; R'_L = 100k, \;\; R'_H = 248.12k, \;\; R'f = 100k. \;\; All \;\; capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; \mu F. \;\; All \;\; Capacitors are 0.001 \;\; All \;\; Al$ 

#### Lowpass Response



# **Typical Simulation**

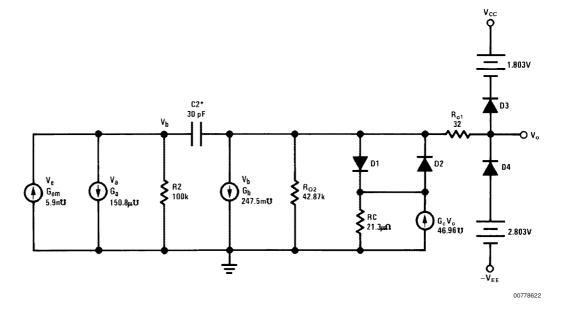
#### LM148, LM741 Macromodel for Computer Simulation



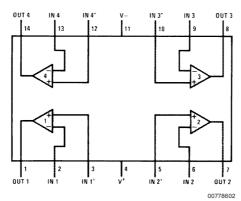
For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

**Note 6:**  $_{01} = 112I_S = 8 \times 10^{-16}$ 

**Note 7:**  $_{02} = 144 ^{*}C2 = 6 \text{ pF for LM} 149$ 



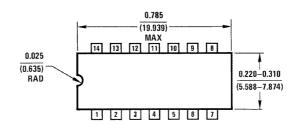
# **Connection Diagram**

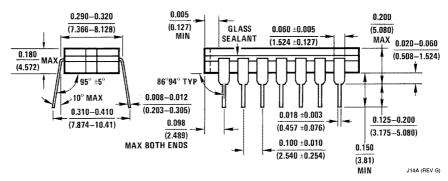


Top View
Order Number LM148J, LM148J/883, LM248J, LM348M, or LM348N
See NS Package Number J14A, M14A or N14A LM148J is available per JM38510/11001

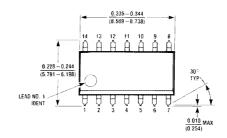
## Physical Dimensions inches (millimeters)

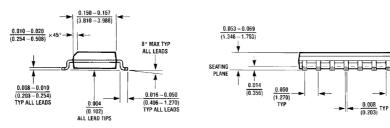
unless otherwise noted





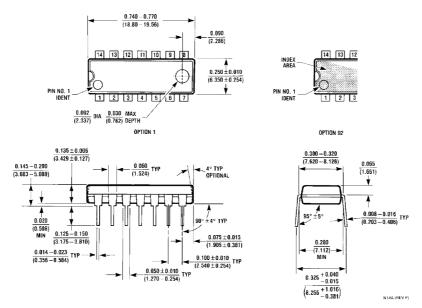
Ceramic Dual-In-Line Package (J)
Order Number LM148J, LM148J/883, LM248J
NS Package Number J14A





S.O. Package (M) Order Number LM348M or LM348MX NS Package Number M14A

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N) Order Number LM348N NS Package Number N14A

#### LIFE SUPPORT POLICY

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- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **BANNED SUBSTANCE COMPLIANCE**

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



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