



No.4040

LA7282,7282M

VCR Audio Signal Recording/
Playback Processor

Overview

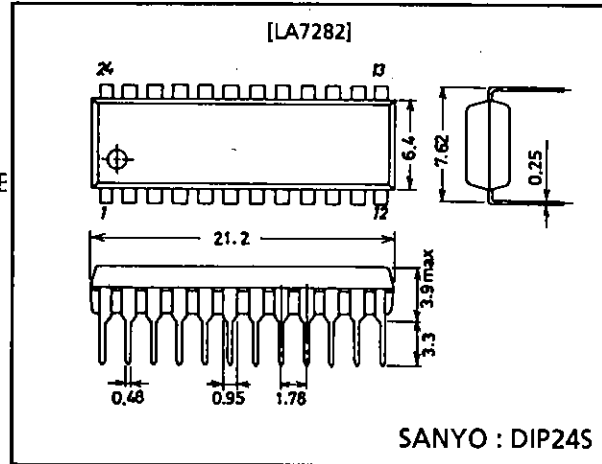
The LA7282 and 7282M are small package LSIs containing all functions necessary to record and playback VTR audio signal.

Features

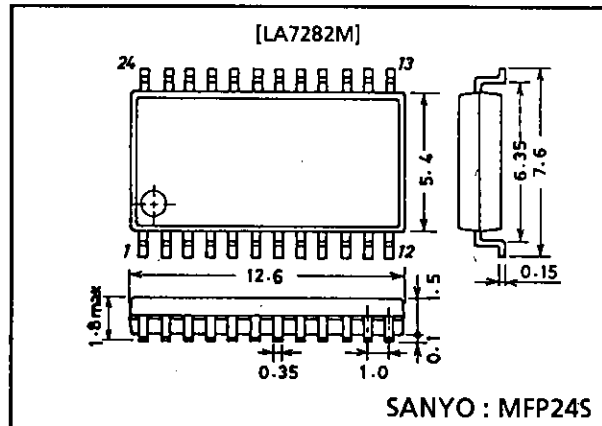
- Smaller package leaves large space for other components.
- Delete of In and Output electrolysis capacitor.
- Low capacitor (0.1 μ F) for the line amp inputs (PE IN and AUDIO IN)
- Non-Adjustment of PB Gain by less gain scatter

Package Dimensions

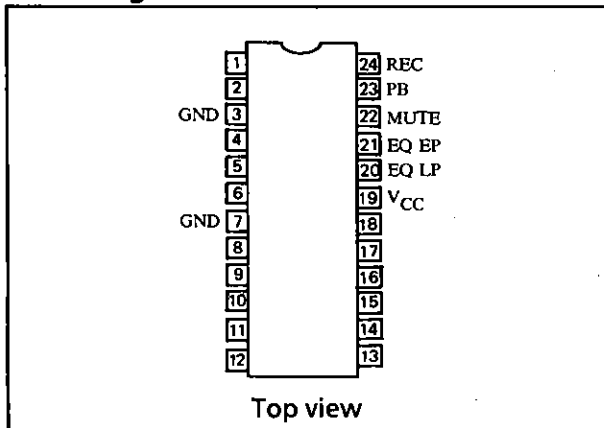
unit : mm
3067-DIP24S



unit : mm
3112-MFP24S



Pin Assignment



LA7282,7282M

Maximum Ratings at Ta = 25°C

				unit
Maximum Supply Voltage	V _{CC} max		14	V
Pin 1 Input Voltage	V _{IN1}	Ta = 65°C, f = 80 kHz (sin), I _{LK} = 10 μA	90 (±45)	Vp-p
Pin 1 Input Current	I _{IN1}		±1.5	mA
Allowable Power Dissipation	Pd max	Ta ≤ 65°C, when mounted on the recommended PCB	400	mW
Operating Temperature	Topr		-10 to +65	°C
Storage Temperature	Tstg		-55 to +125	°C

Operating Conditions at Ta = 25°C

				unit
Recommended Supply Voltage	V _{CC}		12.0	V
Operating Voltage Range	V _{CC} op		11.25 to 12.75	V

Operating Characteristics at Ta = 25°C, V_{CC} = 12 V, f = 1 kHz, OdBv = :1.0 Vrms

			min	typ	max	unit
Current Dissipation (EE)	I _{CCE}	Quiescent	8.0	12.0	17.0	mA
Current Dissipation (PB)	I _{CCP}	Quiescent	9.0	13.0	18.0	mA
Current Dissipation (REC)	I _{CCR}	Quiescent	7.0	10.0	14.0	mA
Overall Gain at PB Mode [Equalizing Amp]	V _G PB	EQ IN-LINE OUT, V _O = -5 dBv	59.0	59.5	60.0	dB
Open Loop Voltage Gain	V _G OE	V _O = -5 dBv	66.0	71.0		dB
Equivalent Input Noise Voltage	V _{NIE}	Rg = 2.2 kΩ, DIN Audio Filter		1.2	1.8	μVrms
Input Impedance [Line Amp]	Z _{INE}			130		kΩ
Voltage Gain (PB IN)	V _G LP	V _O = -5 dBv	21.0	21.5	22.0	dB
Voltage Gain (EE,REC IN)	V _G LR	V _O = -5 dBv	21.0	21.5	22.0	dB
Total Harmonic Distortion	THD _L	V _O = -5 dBv		0.3	0.5	%
Output Noise Voltage	V _{NOL}	DIN Audio Filter		-70.0	-64.0	dBv
Input Impedance (PB IN)	Z _{IN1}			120		kΩ
Input Impedance (EE,REC IN)	Z _{IN2}			120		kΩ
Maximum Output Voltage	V _{OML}	THD = 3%	1.5	2.1		Vrms
Output Voltage at ALC	V _{OA}	V _{IN} = -28 dBv	-9.0	-8.0	-7.0	dBv
ALC Effect	ALC	V _{IN} = -28 to -8 dBv		1.5	3.0	dB
Total Harmonic Distortion at ALC	THD _A	V _{IN} = -28 dBv		0.25	0.6	%
[Recording Amp]						
Voltage Gain (open loop)	V _G OR	V _O = -5 dBv	47.0	52.0		dB
Voltage Gain (closed loop)	V _G CR	V _O = -5 dBv	12.5	13.0	13.5	dB
Total Harmonic Distortion	THD _R	V _O = -5 dBv		0.1	0.3	%
Input Impedance	Z _{INR}			50		kΩ
Maximum Output Voltage	V _{OMR}	THD = 3%	1.5	2.0		Vrms
[Muting Circuit]						
On Voltage	V _{MON}	Pin 22, DC	3.8		6.0	V
Off Voltage	V _{MOFF}	Pin 22, DC	0		1.0	V
Mute Attenuation Level (PB,EE)	M _P , M _E		80.0	90.0		dB
Mute Attenuation Level (REC)	M _R		65.0	70.0		dB
[PB/EE Selector Circuit]						
PB Mode Hold Voltage	V _{PP}	Pin 23, DC	0		1.0	V
EE Mode Hold Voltage	V _{PE}	Pin 23, DC	3.3		6.0	V
[REC/EE Selector Circuit]						
REC Mode Hold Voltage	V _{RR}	Pin 24, DC	3.3		V _{CC}	V
EE Mode Hold Voltage	V _{RE}	Pin 24, DC	0		1.0	V

Continued on next page.

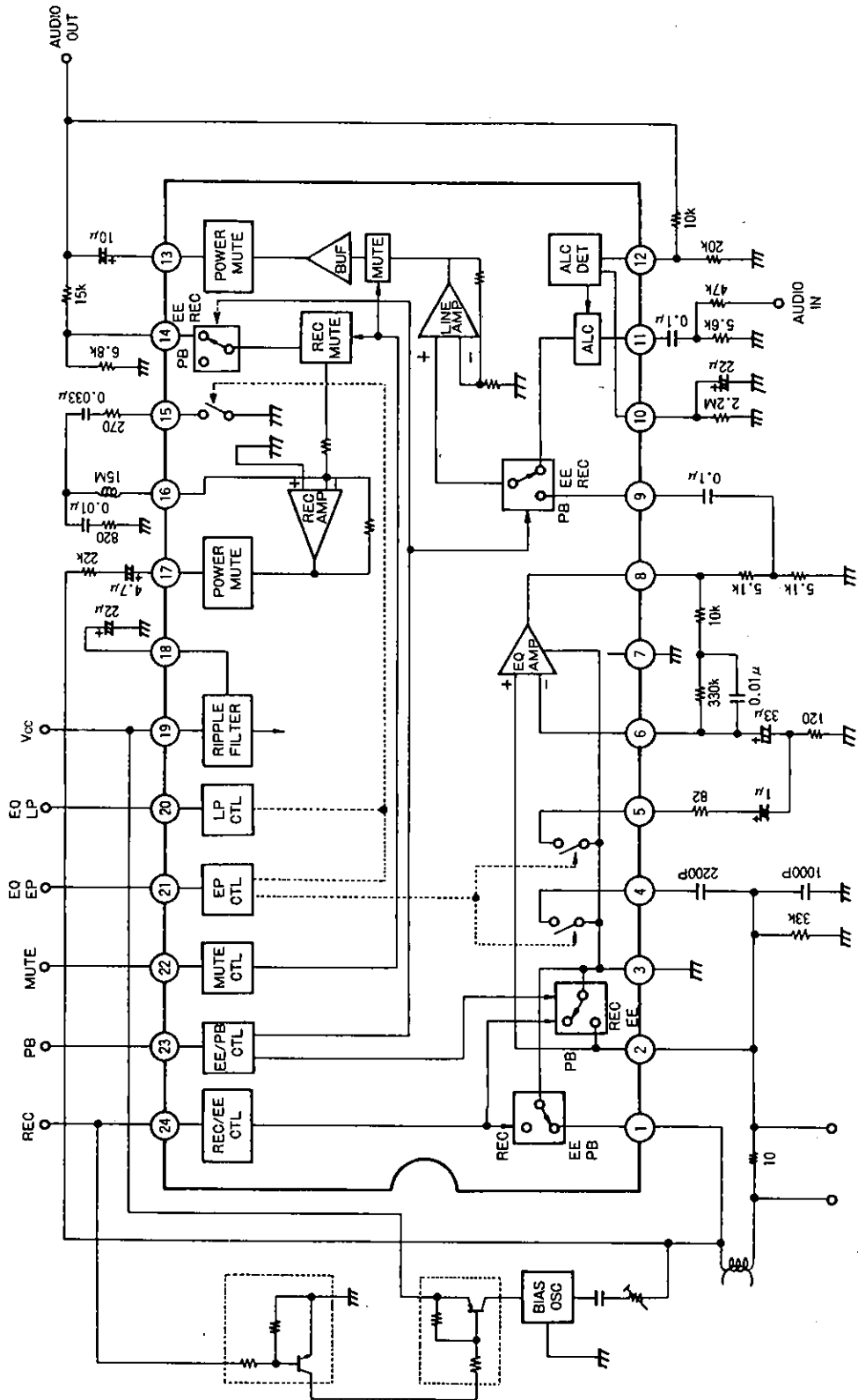
LA7282,7282M

			min	typ	max	unit
[Equalizer Selector Circuit]						
Switch On Voltage	V_{EON}	Pin 20, 21, DC	3.5		6.0	V
Switch Off Voltage	V_{EOFF}	Pin 20, 21, DC	0		0.8	V
[Head Selector Switch]						
Pin 1 On Resistance	R_{ON1}	$I_1 = \pm 1 \text{ mA}$		15	30	Ω
Pin 2 On Resistance	R_{ON2}	$I_2 = \pm 1 \text{ mA}$		5	10	Ω
Pin 1 Input Voltage	V_{IN1}	$T_a = 65^\circ\text{C}, f = 80 \text{ kHz (sin)}, I_{LK} = 10 \mu\text{A}$			± 45	V

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of **December, 1996**. Specifications and information herein are subject to change without notice.

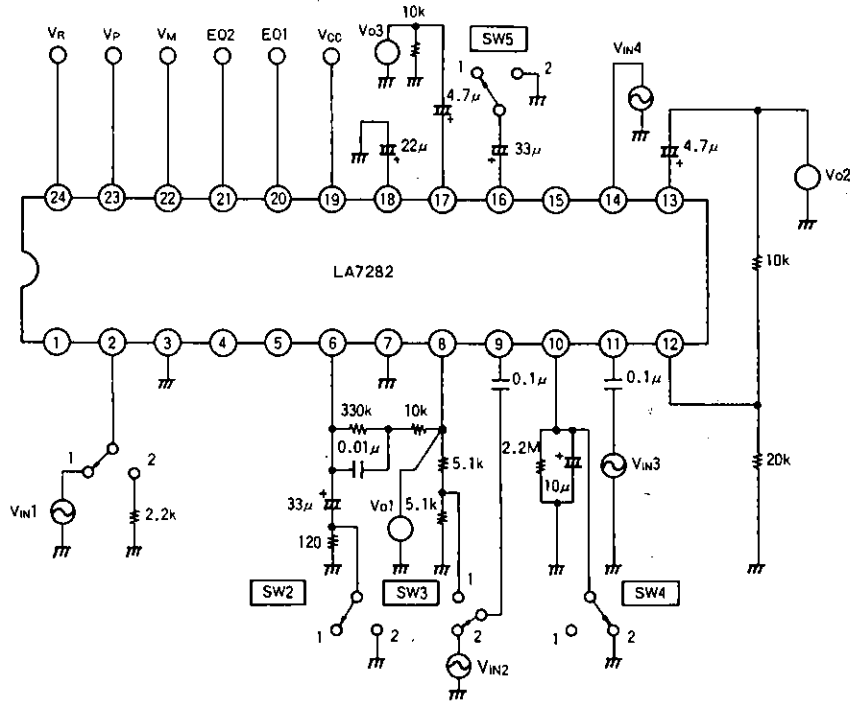
Block Diagram



Unit (resistance : Ω, capacitance : F)

LA7282,7282M

Test Circuit



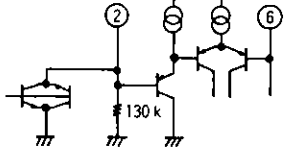
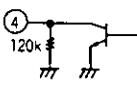
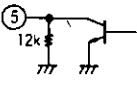
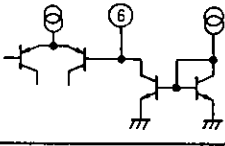
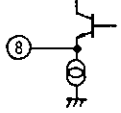
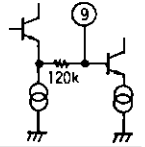
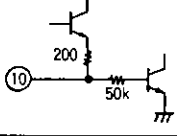
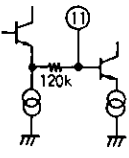
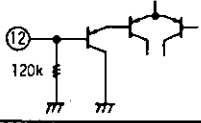
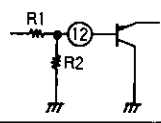
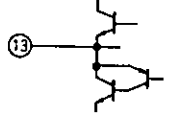
Unit (resistance : Ω, capacitance : F)

<Switch Setting Table>

Parameter (Symbol)	SW1	SW2	SW3	SW4	SW5	V _M	V _P	V _R	Input	Measurement
I _{CCE}	2	1	1	2	1	GND	5V	GND	-	A
I _{CCP}	2	1	1	2	1	GND	GND	GND	-	A
I _{CCR}	2	1	1	2	1	GND	5V	5V	-	A
V _{GPB}	1	1	1	2	1	GND	GND	GND	V _{IN1}	V _{O2}
V _{GOE}	1	2	2	2	1	GND	GND	GND	V _{IN1}	V _{O1}
V _{NIE}	2	1	2	2	1	GND	GND	GND	-	V _{O1}
V _{GLP} , THD _L , V _{OML}	2	1	2	2	1	GND	GND	GND	V _{IN2}	V _{O2}
V _{GLR}	2	1	1	2	1	GND	5V	GND	V _{IN3}	V _{O2}
V _{NOL}	2	1	2	2	1	GND	5V	GND	-	V _{O2}
V _{OA} , ALC, THD _A	2	1	2	1	1	GND	5V	GND	V _{IN3}	V _{O2}
V _{GOR}	2	1	2	2	2	GND	5V	GND	V _{IN4}	V _{O3}
V _{GCR} , THD _R , V _{OMR}	2	1	2	2	1	GND	5V	GND	V _{IN4}	V _{O3}
M _P	1	1	1	2	1	5V	GND	GND	V _{IN1}	V _{O2}
M _R	2	1	1	2	1	5V	5V	GND	V _{IN4}	V _{O3}
M _E	2	1	2	2	1	5V	5V	GND	V _{IN2}	V _{O2}

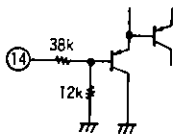
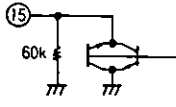
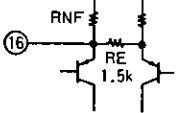
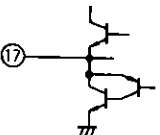
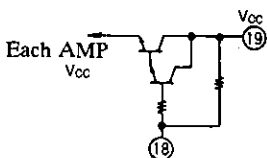
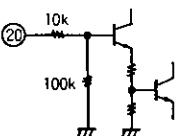
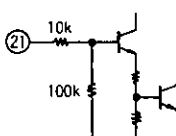
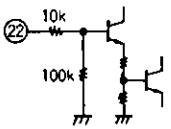
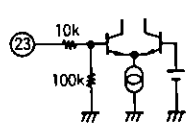
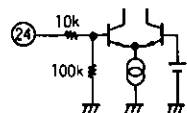
LA7282,7282M

Pin Functions

Pin No.	Function	Terminal Circuit	Description
1	Head Switch 1 (High voltage)		EE, PB: on; REC: off On resistance: 10 Ω, typ. With stand voltage during off: ±45 V (f = 80 kHz)
2	EQ AMP Input and Head Switch 2		Input playback signal to the head. Input impedance: 130 kΩ, typ. EE, REC: on; PB: off Switch on resistance: 5 Ω, typ.
3	GND		An exclusive GND for pin 1 head switch 1, EQ AMP and playback EP switch
4	EP Switch 1		Sets the tape head resonant frequency. On resistance: 15 Ω, typ. Input impedance: 120 kΩ, typ. (playback EP mode)
5	EP Switch 2		Increases the voltage gain at higher frequencies by reducing negative feedback amount of the PB EQ AMP. On resistance: 15 Ω, typ. Input impedance: 12 kΩ, typ. (playback EP mode)
6	EQ AMP NFB		Input of negative feedback of the EQ AMP to establish desired equalizing characteristics.
7	GND		Common return for all circuits except for EQ AMP and head switch 1.
8	EQ AMP Output		
9	LINE AMP PB Input		Input PB signal to the EQ AMP. The input impedance of pin 9 is high (120 kΩ) and requires a small coupling capacitor of 0.1 μF.
10	ALC FILTER		Connecting this pin to GND through a capacitor enables detection. The RC time constant sets attack recovery time.
11	LINE AMP Audio Input		Input EE, REC signal. Select value of R ₁ and R ₂ so that the reference input is at the shoulder of the ALC. The amp gain should be set for 21.5 dB. The input impedance of pin 11 is high (120 kΩ) and requires a small coupling capacitor of 0.1 μF.
12	ALC Detect Input		 Accepts the output signal of LINE amp. The ALC level is determined by the voltage divider consisting of R ₁ and R ₂ .
13	LINE AMP Output		Output impedance: 50 Ω, typ.

Unit (resistance : Ω)

LA7282,7282M

Pin No.	Function	Terminal Circuit	Description																								
14	REC AMP Input		Input recording signal from LINE AMP. Input current is set by the divider consisting of R_1 and R_2 . Pin 14 requires no coupling capacitor since REC AMP is to operate at zero level and as inverting amp.																								
15	LP Switch		Sets the high peaking point to the frequency suitable for LP. On resistance: 15 Ω typ. Input impedance: 60 k Ω typ.																								
16	REC AMP NFB		Connecting an L, C, R network to this pin causes a peaking frequency to rise.																								
17	REC AMP Output		Output impedance: 40 Ω typ.																								
18	Ripple Filter		Connecting an electrolytic capacitor across this pin and GND smooths ripples.																								
19	Supply Voltage (V_{CC})		$V_{CC} = 15$ V max $V_{CC} = 11.25 - 12.75$ V typ.																								
20	LP Control		Applying 3.5 V DC or more (6.0 V max.) to this pin turns on LP switch (pin 15). The switch turns off at 0.8 V or below.																								
21	EP Control		Applying 3.5 V DC or more (6.0 V max.) to this pin turns on EP switch (pin 4,5) and LP switch (pin 15). The switches turn off at 0.8 V or below.																								
22	MUTE Control		Applying 3.8 V DC or more (6.0 V max.) to this pin turns on mute circuit. The mute is disabled at 1.0 V or below. [Control mode]																								
			<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">Mode</th> <th colspan="2">MUTE 'L'</th> <th colspan="2">MUTE 'H'</th> </tr> <tr> <th>LINE AMP</th> <th>REC AMP</th> <th>LINE AMP</th> <th>REC AMP</th> </tr> </thead> <tbody> <tr> <td>PB Mode</td> <td style="text-align: center;">○</td> <td style="text-align: center;">×</td> <td style="text-align: center;">×</td> <td style="text-align: center;">×</td> </tr> <tr> <td>EE Mode</td> <td style="text-align: center;">○</td> <td style="text-align: center;">○</td> <td style="text-align: center;">×</td> <td style="text-align: center;">×</td> </tr> <tr> <td>REC Mode</td> <td style="text-align: center;">○</td> <td style="text-align: center;">○</td> <td style="text-align: center;">○</td> <td style="text-align: center;">×</td> </tr> </tbody> </table> <p style="text-align: center;">[O: Pass signal, x: Block signal]</p>	Mode	MUTE 'L'		MUTE 'H'		LINE AMP	REC AMP	LINE AMP	REC AMP	PB Mode	○	×	×	×	EE Mode	○	○	×	×	REC Mode	○	○	○	×
Mode	MUTE 'L'		MUTE 'H'																								
	LINE AMP	REC AMP	LINE AMP	REC AMP																							
PB Mode	○	×	×	×																							
EE Mode	○	○	×	×																							
REC Mode	○	○	○	×																							
23	PB Control		Applying 3.3 V DC or more (6.0 V max.) to this pin enters EE mode and 1.0 V or below PB mode.																								
24	REC Control		Applying 3.0 V DC or more (up to V_{CC}) to this pin enters REC mode and 1.0 V or below EE mode.																								

Unit (resistance : Ω)