Features

- High-speed (26 ns), low power 16-bit cascadable ALU
- Implements add, subtract, accumulate, 2's complement, pass, and logic operations
- All registers have a bypass path for complete flexibility
- Available in MIL-STD-883 compliant version
- Package styles available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

Description

The L4C381 is a flexible, high-speed, cascadable 16-bit Arithmetic and Logic Unit implemented in CMOS technology. It combines four 381-type 4-bit ALUs, a lookahead-carry generator, and miscellaneous interface logic — all in a single 68-pin package. While containing new features to support high-speed pipelined architectures and single 16-bit bus configurations, the L4C381 retains full performance and functional compatibility with the bipolar '381 designs.

Architecture

The L4C381 operates on two 16-bit operands (A and B) and produces a 16-bit result (F). Three select lines control the ALU and provide 3 arithmetic, 3 logical, and 2 initialization functions. Full ALU status is provided to support cascading to longer word lengths. Registers are provided on both the ALU inputs and the output, but these may be bypassed under user control. An internal feedback path allows the registered ALU output to be routed to one of the ALU inputs, accommodating chain operations and accumulation. Furthermore, the A or B input can be forced to Zero allowing unary functions on either operand.

ALU Operations

The S_0–S_2 lines specify the operation to be performed. The ALU functions and their select codes are shown below.

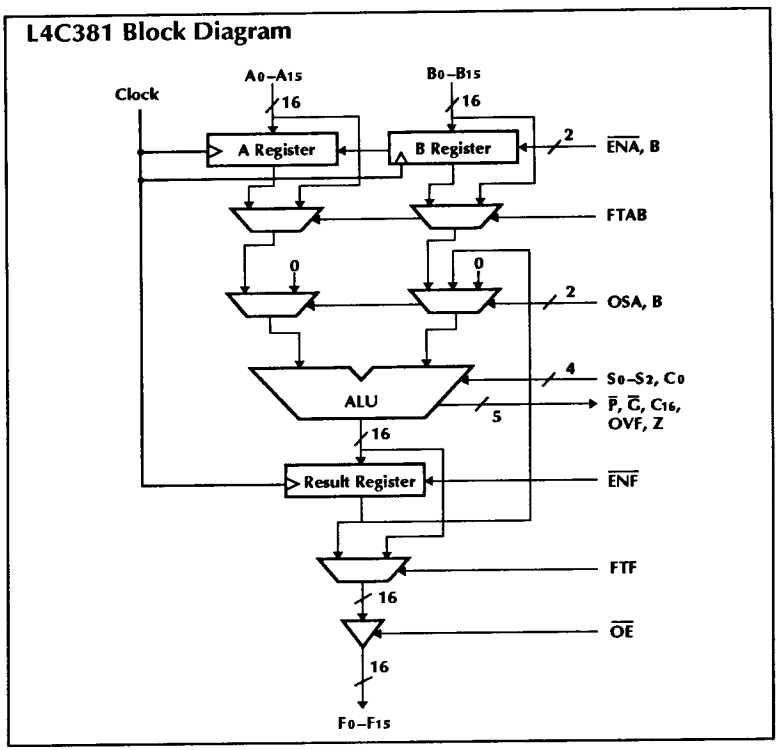
S_2	S_1	S_0	Function
0	0	0	CLEAR (F=00 ... 0)
0	0	1	NOT (A) + B
0	1	0	A + NOT (B)
0	1	1	A + B
1	0	0	A XOR B
1	0	1	A OR B
1	1	0	A AND B
1	1	1	PRESET (F=11 ... 1)

The functions B minus A and A minus B can be achieved by setting the carry input of the least significant slice and selecting codes 001 and 010 respectively.

ALU Status

The ALU provides Overflow and Zero status bits. Carry, Propagate, and Generate outputs are also provided for cascading. These outputs are defined for the three arithmetic functions only. The ALU sets the Zero output when all 16 output bits are

L4C381 Block Diagram



zero. The Generate, Propagate, C_{16}, and OVF flags for the A + B operation are defined in Table 1. The status flags produced for NOT(A) + B and A + NOT(B) can be found by complementing A_i and B_i respectively in Table 1.

Table 1. ALU Status Flags

Bit Carry Generate = $g_i = A_iB_i$,	for i = 0 ... 15
Bit Carry Propagate = $p_i = A_i + B_i$,	for i = 0 ... 15
$P_0 = p_0$	for i = 1 ... 15
$P_i = p_i (P_{i-1})$	for i = 1 ... 15
and	
$G_0 = g_0$	
$G_i = g_i + p_i (G_{i-1})$	for i = 1 ... 15
$C_i = G_{i-1} + P_{i-1} (C_0)$	for i = 1 ... 15
then	
$\overline{G} = \text{NOT}(G_{15})$	
$\overline{P} = \text{NOT}(P_{15})$	
$C_{16} = G_{15} + P_{15}C_0$	
$OVF = C_{15} \text{ XOR } C_{16}$	

Operand Registers

The L4C381 has two 16-bit wide input registers for operands A and B. These registers are rising edge triggered by a common clock. Each register is independently enabled by control signals $\overline{ENA}$ and $\overline{ENB}$.

This architecture allows the L4C381 to accept arguments from a single 16-bit data bus. For those applications that do not require registered inputs, both the A and B operand registers can be bypassed with the FTAB control line. When the FTAB control is asserted, data is routed around the A and B input registers; however, they continue to function normally via the $\overline{ENA}$ and $\overline{ENB}$ controls. The contents of the input registers will again be available to the ALU if the FTAB control is released.

Output Register

The output of the ALU drives the input of a 16-bit register. This rising-edge-triggered register is clocked by the same clock as the input registers. The output register is enabled by the $\overline{ENF}$ control signal. By disabling the output register, intermediate results can be held while loading new input operands. Three-state drivers controlled by the $\overline{OE}$ input allow the L4C381 to be configured in a single bidirectional bus system.

The output register can be bypassed by asserting the FTF control signal. When the FTF control is asserted, output data is routed around the output register, however, it continues to function normally via the $\overline{ENF}$ control.

The contents of the output register will again be available on the output pins if FTF is released. With both FTAB and FTF true (high) the L4C381 is functionally identical to four cascaded 54S381-type devices.

Operand Selection

The two operand select lines OSA and OSB control multiplexers that precede the ALU inputs. These multiplexers provide an operand force-to-zero function as well as F-register feedback to the B input. Table 2 shows the inputs to the ALU as a function of the operand select inputs. Either the A or B operands may be forced to zero.

When both operand select lines are low, the L4C381 is configured as a chain calculation ALU. The registered ALU output is passed back to the B input to the ALU. This allows accumulation operations to be performed by providing new operands via the A input port. The accumulator can be preloaded from the A input by setting OSA true. By forcing the function select lines to the CLEAR state (000), the accumulator may be cleared. Note that this feedback operation is not affected by the state of the FTF control. That is, the F outputs of the L4C381 may be driven directly by the ALU (FTF = true). The output register continues to function, however, and provides the ALU B operand source.

Table 2. Operand Selection Control

OSB, OSA		Operand B	Operand A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_O = Ground, V_{CC} = Max, Note 4, 8			−250	mA
I_{CC1}	V_{CC} Current, Dynamic	Notes 5, 6		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	Note 7			1.0	mA

Switching Characteristics

Over Commercial Operating Range (Notes 9, 10)

***Guaranteed Maximum Combinational Delays** (ns)*

To Output / From Input	L4C381-55				L4C381-40				L4C381-26			
	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}
FTAB = 0, FTF = 0												
Clock	32	38	53	36	26	30	44	32	22	22	26	22
C_0	—	—	34	22	—	—	28	20	—	—	28	18
S_0–S_2, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 0, FTF = 1												
Clock	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_0–S_2, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22
FTAB = 1, FTF = 0												
A_0–A_{15}, B_0–B_{15}	—	36	46	37	—	30	40	32	—	22	22	22
Clock	32	—	—	—	26	—	—	—	22	—	—	—
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_0–S_2, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 1, FTF = 1												
A_0–A_{15}, B_0–B_{15}	55	36	46	37	40	30	40	32	26	22	22	22
Clock (OSA,B=0)	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_0–S_2, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22

***Guaranteed Minimum Setup and Hold Times With Respect to Clock Rising Edge** (ns)*

Input	L4C381-55				L4C381-40				L4C381-26			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_0–A_{15}, B_0–B_{15}	8	0	35	0	6	0	28	0	6	0	16	0
C_0	21	0	21	0	16	0	16	0	8	0	8	0
S_0–S_2, OSA, OSB	44	0	44	0	32	0	32	0	18	0	18	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	8	2	8	2	6	2	6	2	6	2	6	2

***Three State Enable/Disable Times** (ns) (Note 11)*

	L4C381-55	L4C381-40	L4C381-26
t_{EN}	20	18	16
t_{DIS}	20	18	16

***Clock Cycle Time and Pulse Width** (ns)*

	L4C381-55	L4C381-40	L4C381-26
Minimum Cycle Time	43	34	20
Highgoing Pulse	15	10	10
Lowgoing Pulse	15	10	10

Switching Characteristics

Over Military Operating Range (Notes 9, 10)

***Guaranteed Maximum Combinational Delays** (ns)*

From Input \ To Output	L4C381-65				L4C381-45				L4C381-30			
	F0–F15	P,G	OVF,Z	C16	F0–F15	P,G	OVF,Z	C16	F0–F15	P,G	OVF,Z	C16
FTAB = 0, FTF = 0												
Clock	37	44	63	45	28	34	50	34	26	28	34	28
C0	—	—	42	25	—	—	32	23	—	—	22	22
S0–S2, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 0, FTF = 1												
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C0	42	—	42	25	32	—	32	23	26	—	22	22
S0–S2, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28
FTAB = 1, FTF = 0												
A0–A15, B0–B15	—	44	56	44	—	32	46	36	—	28	28	28
Clock	37	—	—	—	28	—	—	—	26	—	—	—
C0	—	—	42	25	—	—	32	23	—	—	22	22
S0–S2, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 1, FTF = 1												
A0–A15, B0–B15	65	44	56	44	45	32	46	36	30	28	28	28
Clock (OSA,B=0)	68	44	63	45	56	34	50	34	34	28	34	28
C0	42	—	42	25	32	—	32	23	26	—	22	22
S0–S2, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28

***Guaranteed Minimum Setup and Hold Times With Respect to Clock Rising Edge** (ns)*

Input	L4C381-60				L4C381-45				L4C381-30			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A0–A15, B0–B15	10	0	43	0	8	0	33	0	8	0	20	0
C0	25	0	25	0	20	0	20	0	12	0	12	0
S0–S2, OSA, OSB	50	0	50	0	36	0	36	0	20	0	20	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	10	2	10	2	8	2	8	2	8	2	8	2

***Three State Enable/Disable Times** (ns) (Note 11)*

	L4C381-60	L4C381-45	L4C381-30
t_{EN}	22	20	18
t_{DIS}	22	20	18

***Clock Cycle Time and Pulse Width** (ns)*

	L4C381-60	L4C381-45	L4C381-30
Minimum Cycle Time	52	38	26
Highgoing Pulse	20	15	12
Lowgoing Pulse	20	15	12

Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

Cascading the L4C381

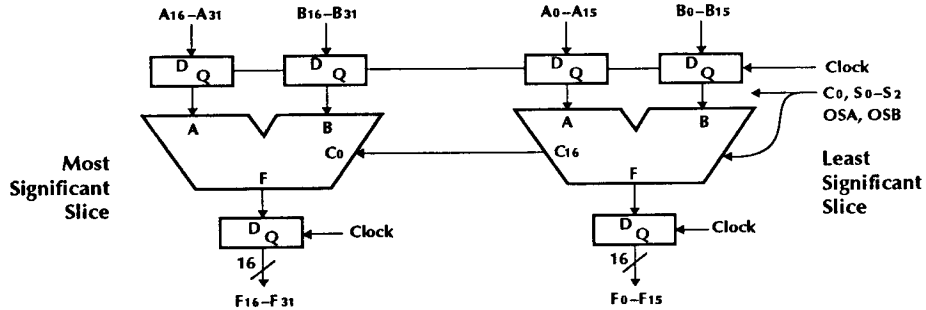
Cascading the L4C381 to 32 bits is accomplished simply by connecting the C_{16} output of the least significant slice to the C_0 input of the most significant slice. The S_0–S_2, OSA, OSB, $\overline{ENA}$, $\overline{ENB}$, and $\overline{ENF}$ lines are common to both devices. The Zero output flags should be logically ANDed to produce the Zero flag for the 32-bit result. The OVF and C_{16} outputs of the most significant slice are valid for the 32-bit result.

Propagation delay calculations for this configuration require two steps: First determine the propagation delay from the input of interest to the C_{16} output of the lower slice. Add this number to the delay from the C_0 input of the upper slice to the output of interest (of the C_0 setup time, if the F register is used). The sum gives the overall input-to-output delay (or setup time) for the 32-bit configuration. This method gives a conservative result, since the C_{16} output is very lightly loaded. Formulas for calculation of all critical delays for a 32-bit system are shown in Figure 4.

Cascading to greater than 32 bits can be accomplished in two ways: The simplest (but slowest) method is to simply connect the C_{16} output of each slice to the C_0 input of the next more significant slice. Propagation delays are calculated as for the 32-bit case, except that the C_0 to C_{16} delays for all intermediate slices must be added to the overall delay for each path. A faster method is to use an external carry-lookahead generator. The $\overline{P}$ and $\overline{G}$ outputs of each slice are connected as inputs to the CLA generator, which in turn produces the C_0 inputs for each slice except the least significant. The C_{16} outputs are not used in this case, except for the most significant one, which is the carry out of the overall system. The carry in to the system is connected to the C_0 input of the least significant slice, and also to the carry lookahead generator. Propagation delays for this configuration are the sum of the time to $\overline{P}$, $\overline{G}$, for the least significant slice, the propagation delay of the carry lookahead generator, and the C_0 to output time of the most significant slice.

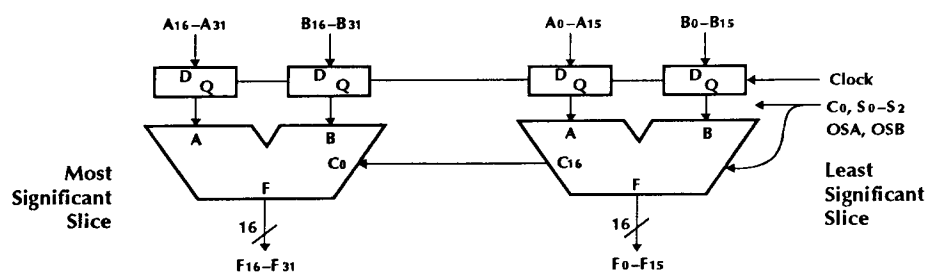
FTAB = 0
FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
Clock	→ Other	=	(Clock → C16) + (C0 → Out)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	Same as 16-bit case
C0	Setup time	=	(C0 → C16) + (C0 Setup time)
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + C0 Setup
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C16) + (C0 Setup time)



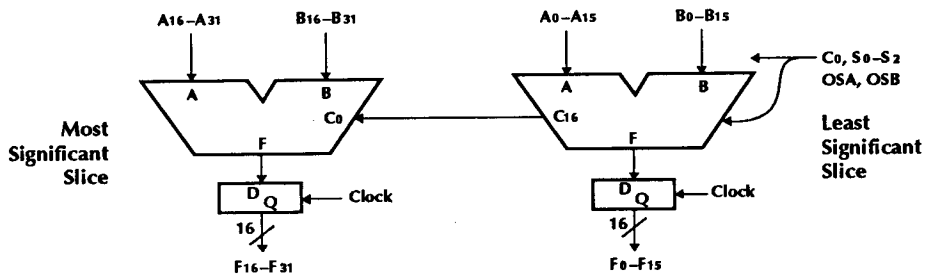
FTAB = 0
FTF = 1

From	To		Calculated Specification Limit
Clock	→ F	=	(Clock → C16) + (C0 → F)
Clock	→ Other	=	(Clock → C16) + (C0 → Out)
C0	→ F	=	(C0 → C16) + (C0 → F)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ F	=	(S0–S2, OSA, OSB → C16) + (C0 → F)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	Same as 16-bit case
C0	Setup time	=	(C0 → C16) + (C0 Setup time)
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + (C0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C16) + (C0 Setup time)



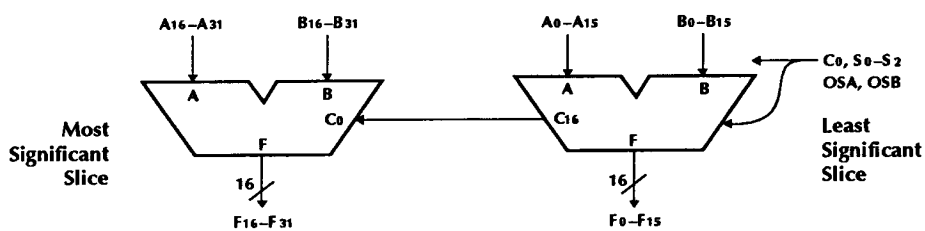
FTAB = 1
FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
A, B	→ Other	=	(A, B → C16) + (C0 → Out)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	(A, B → C16) + (C0 Setup time)
C0	Setup time	=	(C0 → C16) + (C0 Setup time)
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + (C0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C16) + (C0 Setup time)



FTAB = 1
FTF = 1

From	To		Calculated Specification Limit
A, B	→ F	=	(A, B → C16) + (C0 → F)
A, B	→ Other	=	(A, B → C16) + (C0 → Out)
C0	→ F	=	(C0 → C16) + (C0 → F)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ F	=	(S0–S2, OSA, OSB → C16) + (C0 → F)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	(A, B → C16) + (C0 Setup time)
C0	Setup time	=	(C0 → C16) + (C0 Setup time
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + (C0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C16) + (C0 Setup time)



Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance		
	55 ns	40 ns	26 ns
L4C381			
68-pin Plastic LCC, J-Lead — J2	L4C381JC55	L4C381JC40	L4C381JC26
68-pin Pin Grid Array — G1	L4C381GC55	L4C381GC40	L4C381GC26
68-pin Ceramic LCC — K3	L4C381KC55	L4C381KC40	L4C381KC26

Military Operating Range (–55°C to +125°C)

Package Style	Performance		
	65 ns	45 ns	30 ns
L4C381			
68-pin Pin Grid Array — G1	L4C381GM65 L4C381GME65	L4C381GM45 L4C381GME45 L4C381GMB45	L4C381GM30 L4C381GME30 L4C381GMB30
68-pin Ceramic LCC — K3	L4C381KM65 L4C381KME65	L4C381KM45 L4C381KME45 L4C381KMB45	L4C381KM30 L4C381KME30 L4C381KMB30

Pin Assignments

Pin		Function	Pin		Function
J,K	G		J,K	G	
1	F02	A_0	35	F10	F_8
2	F01	A_1	36	F11	F_7
3	E02	A_2	37	G10	F_6
4	E01	A_3	38	G11	F_5
5	D02	A_4	39	H10	F_4
6	D01	A_5	40	H11	F_3
7	C02	A_6	41	J10	F_2
8	C01	A_7	42	J11	F_1
9	B01	A_8	43	K11	F_0
10	B02	A_9	44	K10	C_0
11	A02	A_{10}	45	L10	S_0
12	B03	A_{11}	46	K09	S_1
13	A03	A_{12}	47	L09	S_2
14	B04	A_{13}	48	K08	OSA
15	A04	A_{14}	49	L08	OSB
16	B05	A_{15}	50	K07	FTAB
17	A05	CLK	51	L07	$\overline{ENB}$
18	B06	V_{CC}	52	K06	$\overline{ENA}$
19	A06	GND	53	L06	B_0
20	B07	C_{16}	54	K05	B_1
21	A07	$\overline{P}$	55	L05	B_2
22	B08	$\overline{G}$	56	K04	B_3
23	A08	ZERO	57	L04	B_4
24	B09	OVF	58	K03	B_5
25	A09	$\overline{ENF}$	59	L03	B_6
26	A10	FTF	60	L02	B_7
27	B10	$\overline{OE}$	61	K02	B_8
28	B11	F_{15}	62	K01	B_9
29	C10	F_{14}	63	J02	B_{10}
30	C11	F_{13}	64	J01	B_{11}
31	D10	F_{12}	65	H02	B_{12}
32	D11	F_{11}	66	H01	B_{13}
33	E10	F_{10}	67	G02	B_{14}
34	E11	F_9	68	G01	B_{15}

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