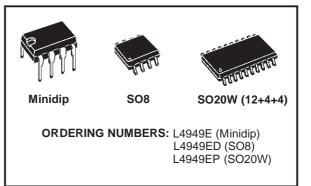


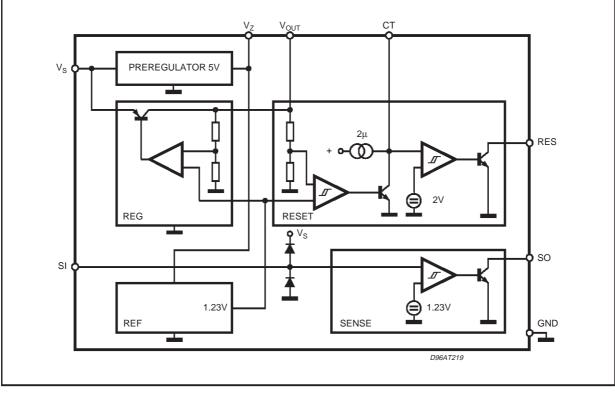
L4949E MULTIFUNCTION VERY LOW DROP VOLTAGE REGULATOR

- OPERATING DC SUPPLY VOLTAGE RANGE 5V - 28V
- TRANSIENT SUPPLY VOLTAGE UP TO 40V
- EXTREMELY LOW QUIESCENT CURRENT IN STANDBY MODE
- HIGH PRECISION STANDBY OUTPUT VOLT-AGE 5V±1%
- OUTPUT CURRENT CAPABILITY UP TO 100mA
- VERY LOW DROPOUT VOLTAGE LESS THAN 0.5V
- RESET CIRCUIT SENSING THE OUTPUT VOLTAGE
- PROGRAMMABLE RESET PULSE DELAY WITH EXTERNAL CAPACITOR
- VOLTAGE SENSE COMPARATOR
- THERMAL SHUTDOWN AND SHORT CIR-CUIT PROTECTIONS



DESCRIPTION

The L4949E is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions as power-on reset and input voltage sense. It is designed for supplying the microcomputer controlled systems especially in automotive applications.



BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

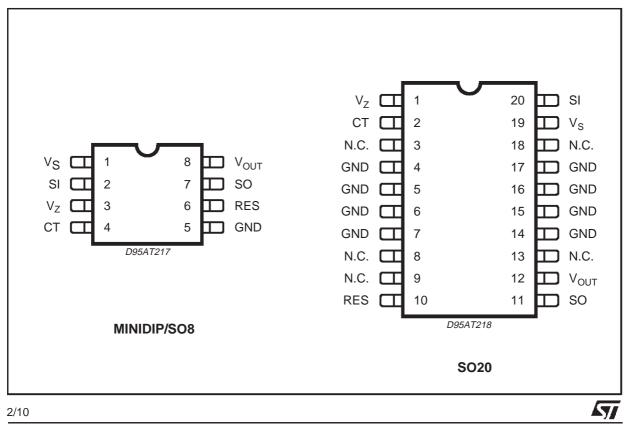
Symbol	Parameter	Value	Unit
V _{SDC}	DC Operating Supply Voltage	28	V
V _{STR}	Transient Supply Voltage (T < 1s)	40	V
lo	Output Current	Internally Limited	
Vo	Output Voltage	20	V
V_{RES}, V_{SO}	Output Voltage	20	V
I _{RES} , I _{SO}	Output Current	5	mA
Vz	Preregulator Output Voltage	7	V
Ι _Ζ	Preregulator Output Current	5	mA
TJ	Junction Temperature	-40 to +150	°C
T _{stg}	Storage Temperature Range	-55 to +150	°C

Note: The circuit is ESD protected according to MIL-STD-883C

THERMAL DATA

Symbol	Description		Minidip	SO-8	SO20L	Unit
R _{th j-amb}	Thermal Resistance Junction-ambient	Max	100	200	50	°C/W
R _{th j-pins}	Thermal Resistance Junction-pins	Max			15	°C/W
TJSD	Thermal Shutdown Junction temperature			165		°C

PIN CONNECTIONS



Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
Vo	Output Voltage	$T_{J} = 25^{\circ}C; I_{O} = 1mA$	4.95	5	5.05	V
Vo	Output Voltage	$6V < V_{IN} < 28V, 1mA < I_O < 50mA$	4.90	5	5.10	V
Vo	Output Voltage	$V_{IN} = 40V;$ T < 1s 5mA < I _O < 100mA	4.75		5.25	V
V _{DP}	Dropout Voltage	$I_{O} = 10mA$ $I_{O} = 50mA$ $I_{O} = 100mA$		0.1 0.2 0.3	0.25 0.4 0.5	V V V
V _{IO}	Input to Output Voltage Difference in Undervoltage Condition	$V_{IN} = 4V, I_O = 35mA$			0.4	V
I _{outh} **	Max Output Leakage	$V_{IN} = 25V, V_O = 5.5V$	20	50	80	μA
V _{OL}	Line Regulation	$6V < V_{IN} < 28V; I_0 = 1mA$			20	mV
V _{OLO}	Load Regulation	1mA < I _O < 100mA			30	mV
I _{LIM}	Current Limit	$V_{O} = 4.5V$ $V_{O} = 4.5V$, $T_{J} = 25^{\circ}C$ $V_{O} = 0V$ (note 1)	105 120	200 100	400 400	mA mA mA
I _{QSE}	Quiescent Current	I _O = 0.3mA; T _J < 100°C		200	300	μA
Ι _Q	Quiescent Current	I _O = 100mA			5	mA

$\textbf{ELECTRICAL CHARACTERISTICS} \hspace{0.1 cm} (V_S = 14V; -40^{\circ}C < T_j < 125^{\circ}C \hspace{0.1 cm} unless \hspace{0.1 cm} otherwise \hspace{0.1 cm} specified)$

** With this test we guarantee that with no output current the output voltage will not exceed 5.5V

RESET

V _{RT}	Reset Thereshold Voltage			V _O -0.5V		V
Vrth	Reset Thereshold Hysteresis		50	100	200	mV
t _{RD}	Reset Pulse Delay	C _T = 100nF; T _R ≥100µs	55	100	180	ms
V _{RL}	Reset Output Low Voltage	R_{RES} = 10K Ω to V_O V _S \ge 1.5V			0.4	V
I _{RH}	Reset Output High Leakage Current	$V_{RES} = 5V$			1	μΑ
V _{CTth}	Delay Comparator Thereshold			2		V
VcTth, hy	Delay Comparator Thereshold Hysteresis			100		mV

SENSE

V _{st}	Sense Low Thereshold		1.16	1.23	1.35	V
V _{sth}	Sense Thereshold Hysteresis		20	100	200	mV
V _{SL}	Sense Output Low Voltage	$\label{eq:VSI} \begin{array}{l} V_{SI} \leq 1.16V; V_S \geq 3V \\ R_{SO} = 10K\Omega \mbox{ to } V_O \end{array}$			0.4	V
I _{SH}	Sense Output Leakage	$V_{SO} = 5V; V_{SI} \ge 1.5V$			1	μA
I _{SI}	Sense Input Current	$V_{SI} = 0$	-20	-8	-3	μA

PREREGULATOR

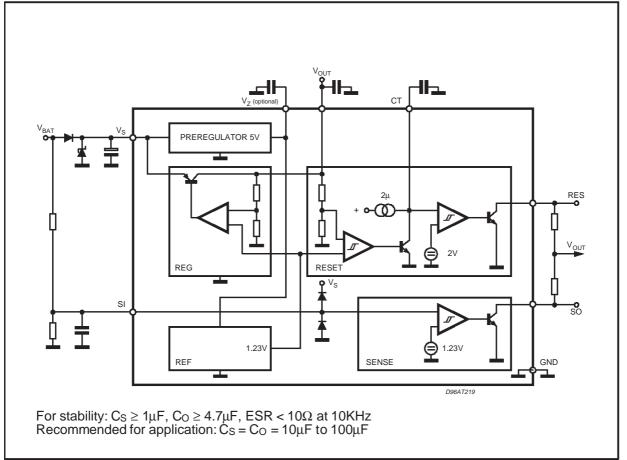
Vz	Preregulator Output Voltage	$I_Z = 10\mu A$	4.5	5	6	V
ا _Z	Preregulator Output Current				10	μA

Note 1: Foldback characteristic

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APPLICATION CIRCUIT



APPLICATION INFORMATION Supply Voltage Transient

High supply voltage transients can cause a reset output signal disturbation.

For supply voltages greater than 8V the circuit shows a high immunity of the reset output against supply transients of more than 100V/ $\mu s.$

For supply voltages less than 8V supply transients of more than $0.4V/\mu s$ can cause a reset signal disturbation.

To improve the transient behaviour for supply voltages less than 8V a capacitor at pin 3 can be used.

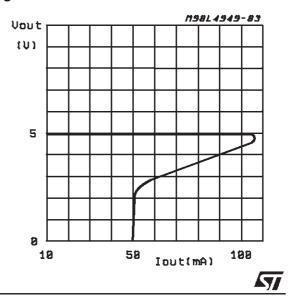
A capacitor at pin 3 (C3 \leq 1µF) reduces also the output noise.

FUNCTIONAL DESCRIPTION

The L4949E is a monolithic integrated voltage regulator, based on the STM modular voltage regulator approch. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

Voltage Regulator

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element. **Figure 1:** Foldback Characteristic of V_O



With this structure very low dropout voltage at currents up to 100mA is obtained. The dropout operation of the standby regulator is maintained down to 3V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. With this feature no functional interruption due to overvoltage pulses is generated. The typical curve showing the standby output voltage as a function of the input supply voltage is shown in Fig. 2. The current consumption of the device (quiescent current) is less than 300µA.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled, the quiescent current as a function of the supply input voltage is shown in Fig. 3.

Figure 2: Output Voltage vs. Input Voltage

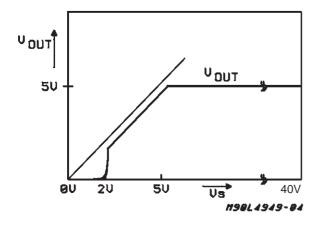
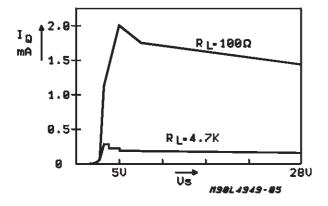


Figure 3: Quiescent Current vs. Supply Voltage



Preregulator

To improve the transient immunity a preregulator stabilized the internal supply voltage to 5V. This internal voltage is present at Pin 3 (Vz). This voltage should not be used as an output because the output capability is very small ($\leq 10\mu A$).

This output may be used as an option when a better transient behaviour for supply voltages less than 8V is required (see also application note).

In this case a capacitor (100nF - 1μ F) must be connected between Pin 3 and GND. If this feature is not used Pin 3 must be left open.

Reset Circuit

The block circuit diagram of the reset circuit is shown in Fig. 4. The reset circuit supervises the output voltage.

The reset thereshold of 4.5V is defined with the internal reference voltage and standby output drivider.

The reset pulse delay time t_{RD} , is defined with the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \bullet 2V}{2\mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T .

The reaction time of the reset circuit increases the noise immunity. Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time will be generated for standby output voltage drops longer than approximately $50\mu s$.

The typical reset output waveforms are shown in Fig. 5.

Sense Comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23V. The use of an external voltage divider makes this comparator very flexible in the application.

It can be used to supervise the input voltage either before or after the protection diode and to give additional informations to the microprocessor like low voltage warnings.

L4949E

Figure 4

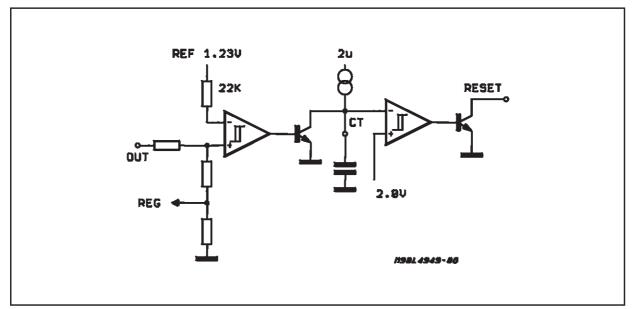
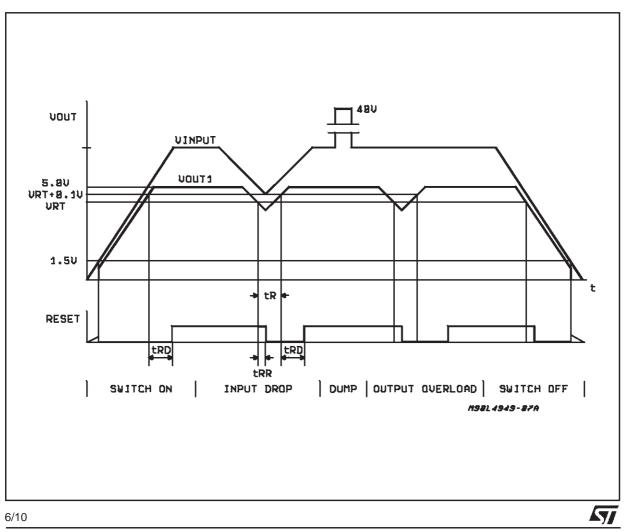
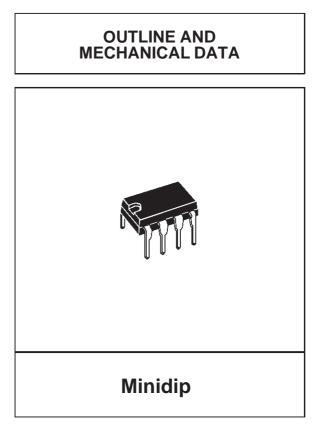


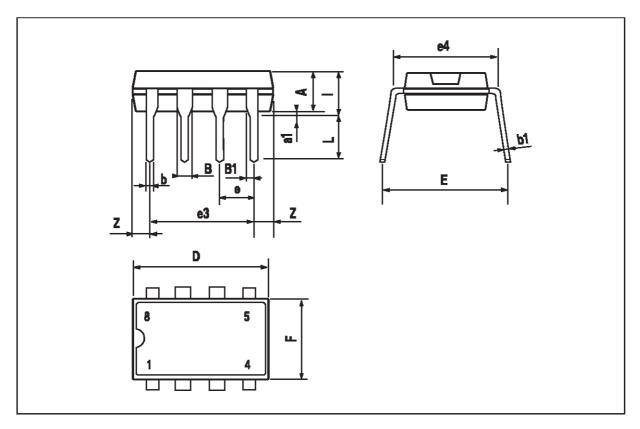
Figure 5



DIM.		mm			inch	
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А		3.32			0.131	
a1	0.51			0.020		
В	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
е		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

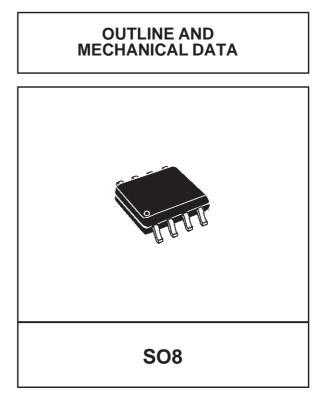
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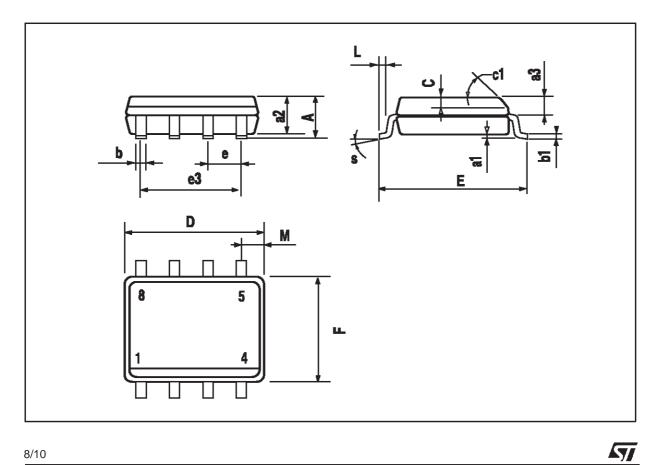


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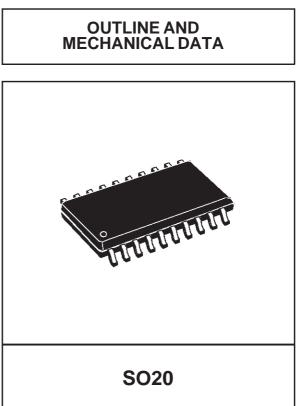
DIM.		mm			inch	
Dini.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.020
c1			45° ((typ.)		
D (1)	4.8		5.0	0.189		0.197
Е	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
М			0.6			0.024
S			8° (n	nax.)		

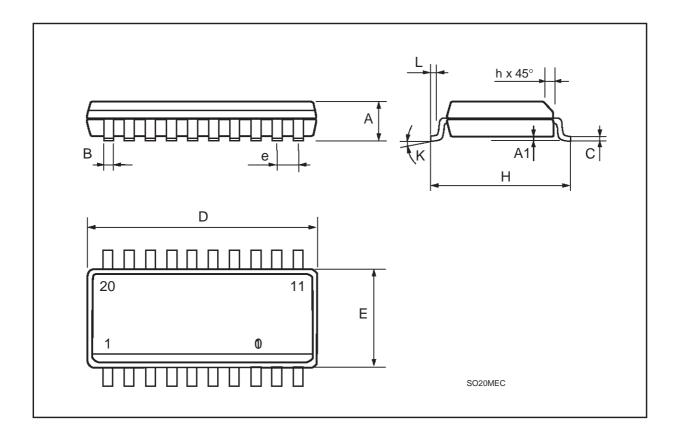


(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006nch).



DIM.		mm		inch			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
А	2.35		2.65	0.093		0.104	
A1	0.1		0.3	0.004		0.012	
В	0.33		0.51	0.013		0.020	
С	0.23		0.32	0.009		0.013	
D	12.6		13	0.496		0.512	
Е	7.4		7.6	0.291		0.299	
е		1.27			0.050		
Н	10		10.65	0.394		0.419	
h	0.25		0.75	0.010		0.030	
L	0.4		1.27	0.016		0.050	
К	0° (min.)8° (max.)						





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