

Data Sheet

FEATURES

- Fastest 64 x 8/9 Cascadeable FIFO
35/25/15 MHz
- Expandable in Word Width & FIFO Depth
- Almost Full/Almost Empty & Half Full Flags
- Fully Independent Asynchronous Inputs & Outputs
- LH5481 Output Enable forces Data Outputs to High-Impedance State
- Pin Compatible & Cascadeable with LH5485/5495 256 x 8/9 FIFOs
- Industry Standard Pinout
- 300-mil 28-pin DIP & 28-pin PLCC Packaging

FUNCTIONAL DESCRIPTION

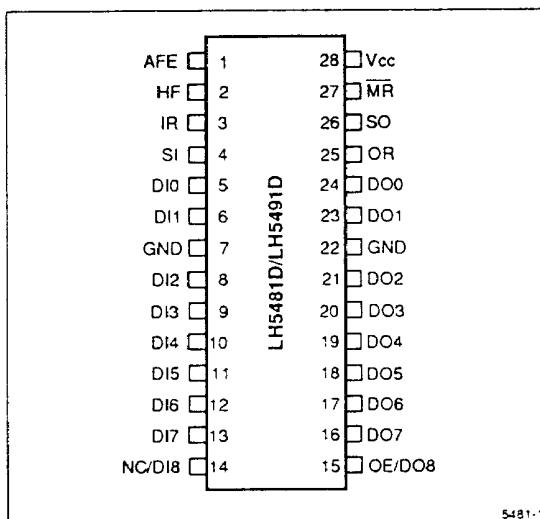
The LH5481 and LH5491 are high performance, asynchronous First-In-First-Out (FIFO) memories organized 64 words deep by 8 or 9-bits wide. The 8-bit LH5481 has an Output Enable (\overline{OE}) function, which can be used to force the 8 data outputs (DO) to a high-impedance state. The LH5491 has 9 data outputs.

These FIFOs accept 8 or 9-bit data at the DI data inputs. A Shift-In (SI) signal writes the DI data into the FIFO. A Shift-Out (SO) signal shifts stored data to the DO outputs. The Output Ready (OR) signal indicates when valid data is present on the DO outputs.

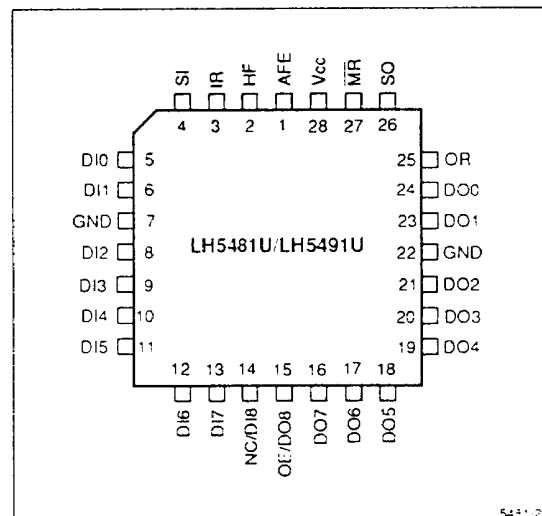
If the FIFO is full and unable to accept more DI data IR will not return high and SI pulses will be ignored. If the FIFO is empty and unable to shift data to the DO outputs, OR will not return high and SO pulses will be ignored. The Almost Full/Almost Empty (AFE) flag is asserted high when the FIFO is almost full (56 words or more) or almost empty (8 words or less). The Half Full (HF) flag is asserted high when the FIFO contains 32 words or more.

Reading and writing operations may be asynchronous, allowing these FIFOs to be used as buffers between digital machines of different operating frequencies. The high speed makes these FIFOs ideal for high performance communication and controller applications.

PINOUT DIAGRAMS

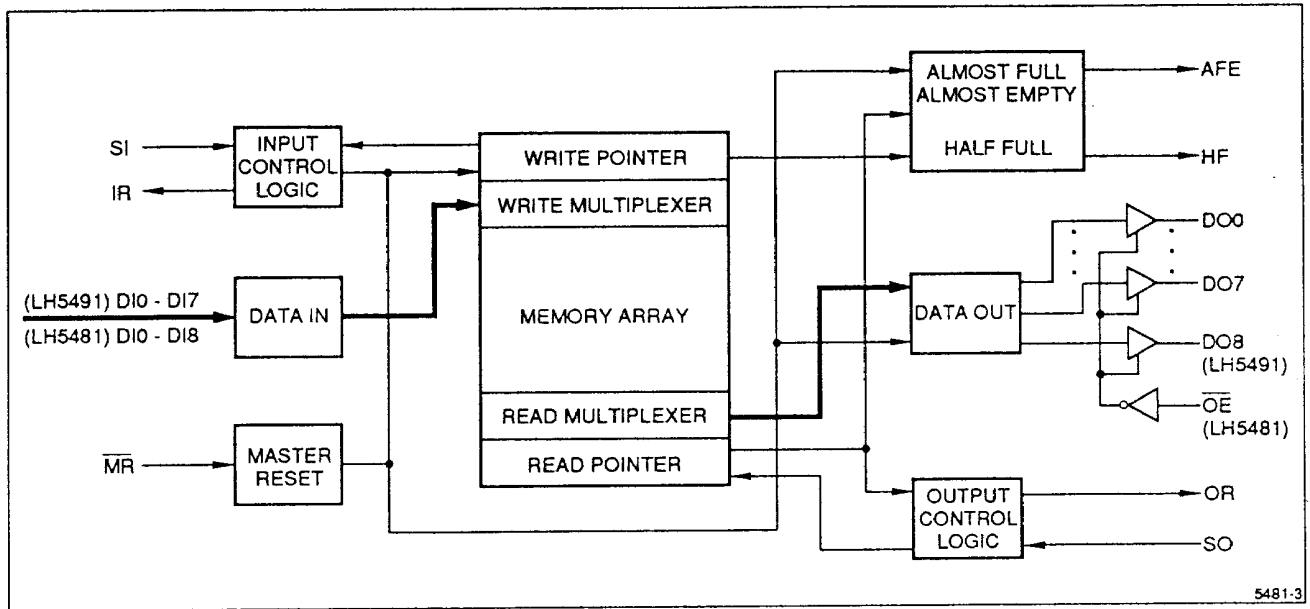


28-Pin DIP (Top View)



28-Pin PLCC (Top View)

BLOCK DIAGRAM



PIN IDENTIFICATION

DI ₀ -DI ₈	Data Inputs	HF	Half Full Flag
DO ₀ -DO ₈	Data Outputs	AFE	Almost Full / Almost Empty
SI	Shift In	$\overline{\text{MR}}$	Master Reset
SO	Shift Out	$\overline{\text{OE}}$	Output Enable (LH5481 only)
IR	Input Ready	V _{CC}	Positive Power Supply
OR	Output Ready	V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS^{1,2}

V _{CC} Range	-0.5V to 7V
Input Voltage Range	-0.5V to V _{CC} +0.5V (not to exceed 7V)
DC Output Current	±40 mA
Storage Temperature	-65°C to 150°C
DC Voltage Applied To Outputs In High-Z state	-0.5V to V _{CC} +0.5V (not to exceed 7V)
Static Discharge Voltage	> 2000V
Power Dissipation (Package Limit)	1.0W

OPERATING RANGE¹

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T _A	Temperature, Ambient	0.0	70	°C
V _{CC}	Supply Voltage	4.5	5.5	V
V _{SS}	Ground	0.0	0.0	V
V _{IL}	Input Low Voltage (Logic "0") ⁵	-0.5	0.8	V
V _{IH}	Input High Voltage (Logic "1")	2.0	V _{CC} +0.5	V

DC ELECTRICAL CHARACTERISTICS¹ (OVER OPERATING RANGE UNLESS OTHERWISE NOTED)¹

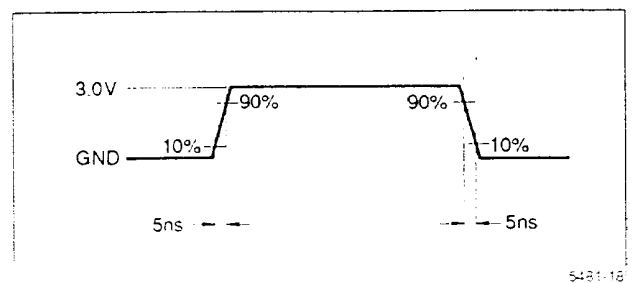
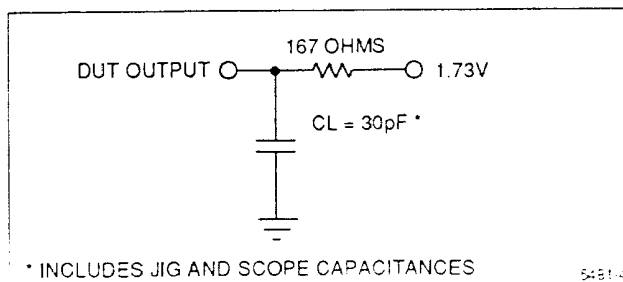
PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
I _{LI}	Input Leakage Current	V _{CC} =5.5V, V _{IN} = 0V to V _{CC}	-10	10	µA
I _{LO}	Output Leakage Current (High-Z)	V _{CC} =5.5V, V _{OUT} = 0V to V _{CC}	-10	10	µA
V _{OH}	Output High Voltage	V _{CC} =4.5V, I _{OH} = -4mA	2.4		V
V _{OL}	Output Low Voltage	V _{CC} =4.5V, I _{OL} = 8.0mA		0.4	V
I _{CCQ}	Power Supply Quiescent Current	V _{CC} =5.5V, I _{OUT} =0mA		25	mA
		V _{IN} <= V _{IL} , V _{IN} >= V _{IH}			
I _{CC}	Power Supply Current ⁶	f _{SI} = 35 MHz, f _{SO} = 35 MHz		45	mA

CAPACITANCE^{1,4}

PARAMETER	DESCRIPTION	TEST CONDITIONS	MAX	UNIT
C _{IN}	Input Capacitance	T _A =25°C, f=1 MHz, V _{CC} =4.5V	5	pF
C _{OUT}	Output Capacitance	T _A =25°C, f=1 MHz, V _{CC} =4.5V	7	pF

AC TEST CONDITIONS¹

Input Pulse Levels	0 to 3V
Input Rise and Fall Times (10% / 90%)	5 ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load for AC Timing Tests	See Figure.



SWITCHING CHARACTERISTICS⁷ (Over Operating Range)

PARAMETERS	DESCRIPTION	15MHz		25MHz		35MHz		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
f _o	Operating Frequency ⁸		15		25		35	MHz
t _{PHSI}	SI HIGH Time ^{9,14}	15		11		9		ns
t _{PLSI}	SI LOW Time ^{9,14}	20		15		13		ns
t _{SSI}	Data Setup to SI ¹⁰	-1		-1		-1		ns
t _{HSI}	Data Hold from SI ¹⁰	14		12		10		ns
t _{DLIR}	Delay, SI HIGH to IR LOW		20		18		16	ns
t _{DHIR}	Delay, SI LOW to IR HIGH		24		20		18	ns
t _{PHSO}	SO HIGH Time ⁹	15		11		9		ns
t _{PLSO}	SO LOW Time ⁹	20		15		13		ns
t _{DLOR}	Delay, SO HIGH to OR LOW		20		18		16	ns
t _{DHOR}	Delay, SO LOW to OR HIGH		24		20		18	ns
t _{SOR}	Data Setup to OR HIGH	-1		-1		-1		ns
t _{HSO}	Data Hold from SO LOW	0		0		0		ns
t _{FT}	Fallthrough Time		36		34		30	ns
t _{BT}	Bubblethrough Time		28		26		25	ns
t _{SIR}	Data Setup to IR ¹¹	5		5		5		ns
t _{HIR}	Data Hold from IR ¹¹	5		5		5		ns
t _{PIR}	Input Ready Pulse HIGH ¹⁴	7		7		7		ns
t _{POR}	Output Ready Pulse HIGH ¹⁴	7		7		7		ns
t _{DLZOE}	OE LOW to LOW Z (LH5481) ^{4,12}		35		30		25	ns
t _{DHZOE}	OE HIGH to HIGH Z (LH5481) ^{4,12}		35		30		25	ns
t _{DHHF}	SI LOW to HF HIGH		40		40		36	ns
t _{DLHF}	SO LOW to HF LOW		40		40		36	ns
t _{DLAFE}	SO or SI LOW to AFE LOW		40		40		36	ns
t _{DHAFE}	SO or SI LOW to AFE HIGH		40		40		36	ns
t _{PMR}	\overline{MR} Pulse Width	35		35		35		ns
t _{D\overline{MR}SI}	\overline{MR} HIGH to SI HIGH		25		25		22	ns
t _{D\overline{MR}OR}	\overline{MR} LOW to OR LOW ¹³		25		25		20	ns
t _{D\overline{MR}IR}	\overline{MR} LOW to IR HIGH ¹³		25		25		20	ns
t _{L\overline{MR}}	\overline{MR} LOW to Output LOW ¹³		25		25		20	ns
t _{A\overline{MR}}	\overline{MR} LOW to AFE HIGH		30		30		30	ns
t _{HF}	\overline{MR} LOW to HF LOW		30		30		30	ns

NOTES:

- All voltages are measured with respect to V_{ss}.
- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
- Sample tested only.
- FIFO inputs are able to withstand a -1.5V undershoot for less than 10ns per cycle.
- I_{cc} is dependent upon actual output loading and cycle rates. Specified values are with outputs open.
- All time measurements performed at "AC Test Conditions".
- f_o = f_{SI} = f_{SO}.
- t_{PHSI} + t_{PLSI} = t_{PHSO} + t_{PLSO} = 1/f_o.
- t_{SSI} and t_{HSI} apply when memory is not full.
- t_{SIR} and t_{HIR} apply when memory is full and SI is HIGH.
- High-Z transitions are referenced to the steady-state V_{OH} - 500mV and V_{OL} + 500mV levels on the output.
- After reset goes LOW, all Data outputs will be at LOW level, IR goes HIGH and OR goes LOW.
- Common dash number devices are guaranteed by design to function properly in a cascaded configuration.

OPERATIONAL DESCRIPTION

Unlike earlier versions of FIFOs, the LH5481 and LH5491 use dual-port Random-Access-Memory, write and read pointers, and special control logic. The write pointer is incremented by the falling edge of the Shift-In (SI) signal, while the read pointer is incremented by the falling edge of the Shift-Out (SO) signal. The Input Ready (IR) signal enables data writing to the FIFO. Output Ready (OR) indicates valid read information is available on the Data Output (DO) pins.

Resetting The FIFO

The FIFO Must Be Reset, upon Power-Up, using the Master Reset (MR) signal. This causes the FIFO to enter an empty state, indicated by the Output Ready (OR) being LOW and Input Ready (IR) being HIGH. All Data Output (DO) pins will be LOW in this state. The AFE flag will be HIGH and the HF flag will be LOW.

If Shift In (SI) is HIGH, when the Master Reset ($\overline{\text{MR}}$) signal is ended, then the data on the Data Input (DI) pins will be written into the FIFO and Input Ready (IR) will return LOW until Shift In (SI) is brought LOW.

If Shift In (SI) is LOW when the Master Reset ($\overline{\text{MR}}$) is ended, then Input Ready (IR) will go HIGH, but the data on the Data Input (DI) pins will not enter the FIFO until Shift In (SI) goes HIGH.

Shifting Data In

Data Input (DI) is shifted into the FIFO on the rising edge of Shift In (SI). This loads input data into the FIFO and causes Input Ready (IR) to go LOW. When a falling edge of Shift In (SI) occurs, the write pointer increments to the next word position and Input Ready (IR) goes HIGH, indicating that the FIFO is ready to accept new data. When the FIFO is full, Input Ready (IR) remains LOW after the negative edge of Shift In (SI) signal; Shift Out (SO) action is required to unload a word of data and bring Input Ready (IR) HIGH - see Bubblethrough description, below.

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of Shift Out (SO). The read pointer increments to the next word

location and FIFO data, if present, will appear on the Data Output (DO) pins and the Output Ready (OR) signal will go HIGH. If FIFO data is not present, Output Ready (OR) will stay LOW, indicating the FIFO is empty; in this case, the last valid data read from the FIFO will remain on the Data Output (DO) pins. When the FIFO is not empty, Output Ready (OR) will go LOW after the rising edge of Shift Out (SO). The previous data remains on the Data Output (DO) pins until a falling edge of Shift Out (SO).

Fallthrough Condition

When the FIFO is empty, a data word entering through the Shift In (SI) action will follow one of two sequences.

If Shift Out (SO) is LOW, the data will propagate to the Data Output (DO) pins and Output Ready (OR) will go HIGH and stay HIGH until the next rising edge of Shift Out (SO).

If Shift Out (SO) is held HIGH while data is shifted into an empty FIFO (as occurs in depth cascading of FIFOs), data will propagate to the Data Output (DO) pins and Output Ready (OR) will pulse HIGH for a minimum time duration specified by t_{POR} and then go back LOW again. The stored word will remain on the Data Output (DO) pins. If more words are written into the FIFO, they will line up behind the first word and not appear on the Data Output (DO) pins until Shift Out (SO) has returned LOW.

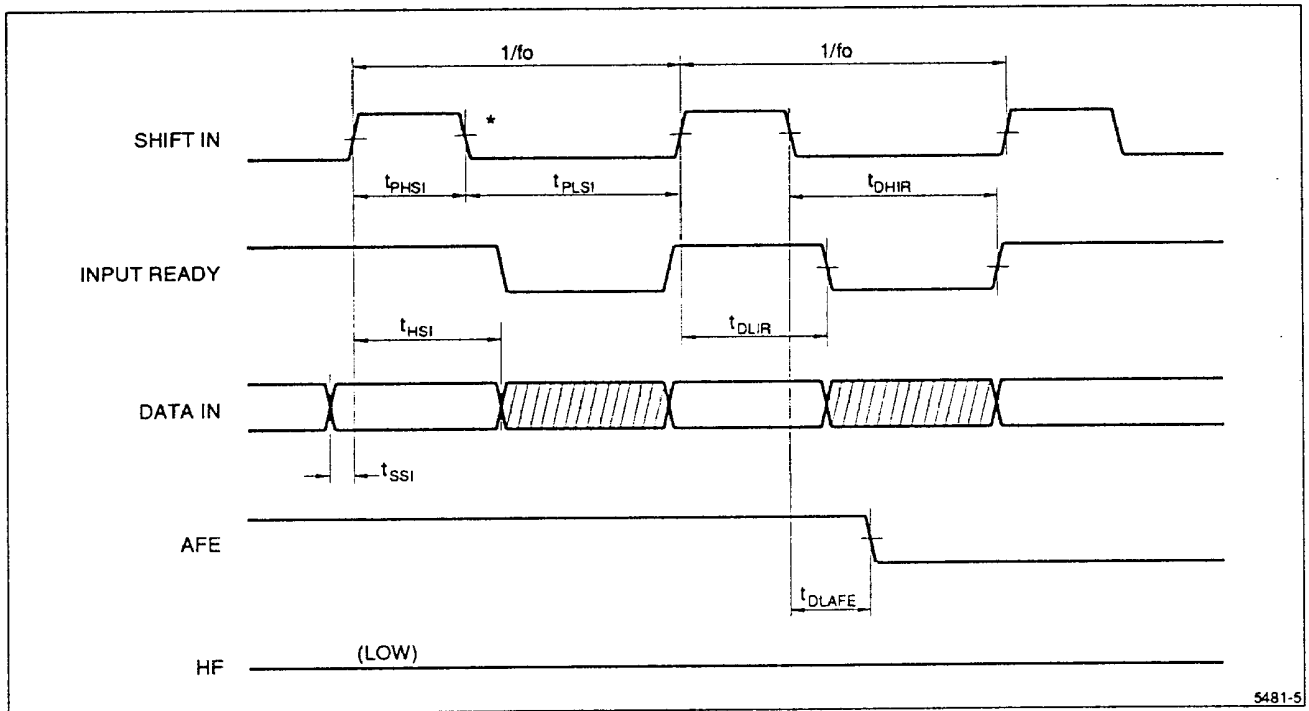
Bubblethrough Condition

When the FIFO is full, Shift Out (SO) action will initiate one of the following two sequences.

If Shift In (SI) is LOW, Input Ready (IR) will go HIGH and stay HIGH until the next rising edge of Shift In (SI).

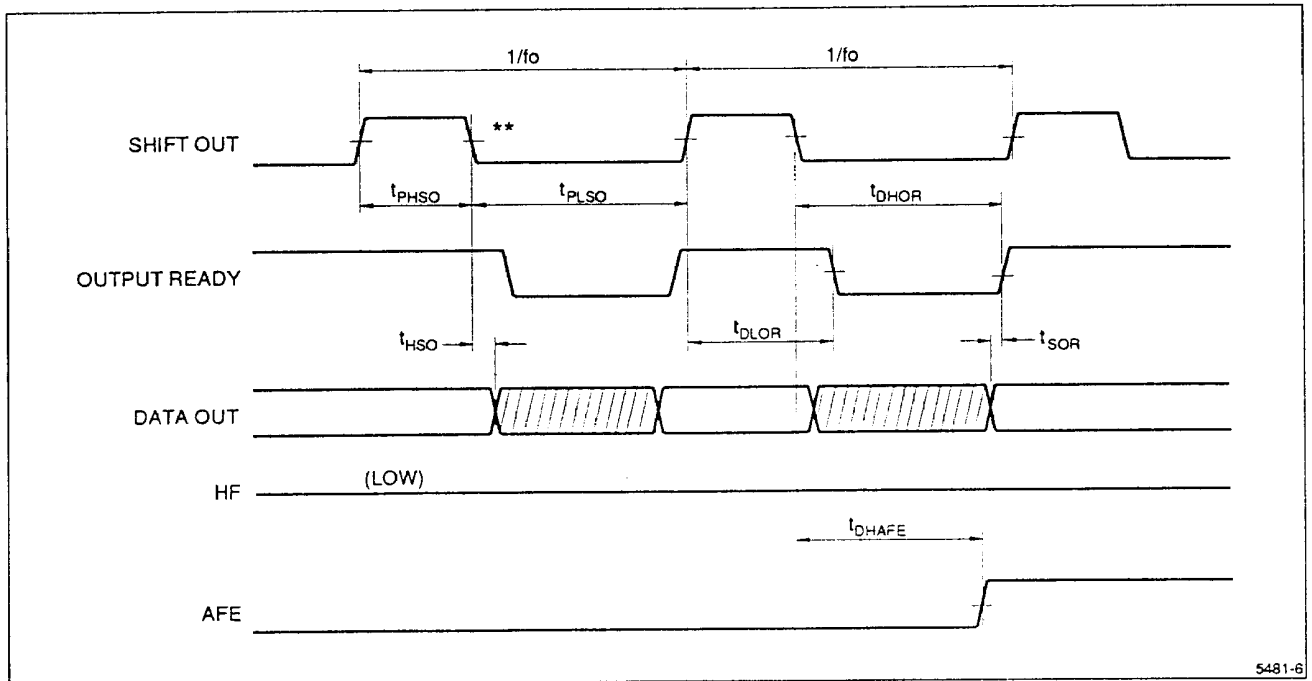
If Shift In (SI) is held HIGH while data is shifted out of a full FIFO (as occurs in depth cascading of FIFOs), Input Ready (IR) will pulse HIGH for a minimum time duration specified by t_{PIR} and then go back LOW again. Special Data Input (DI) setup and hold times (t_{SIIR} and t_{HIIR} , respectively) are defined for this condition.

SWITCHING WAVEFORMS



* NOTE: FIFO Contains 8 Words

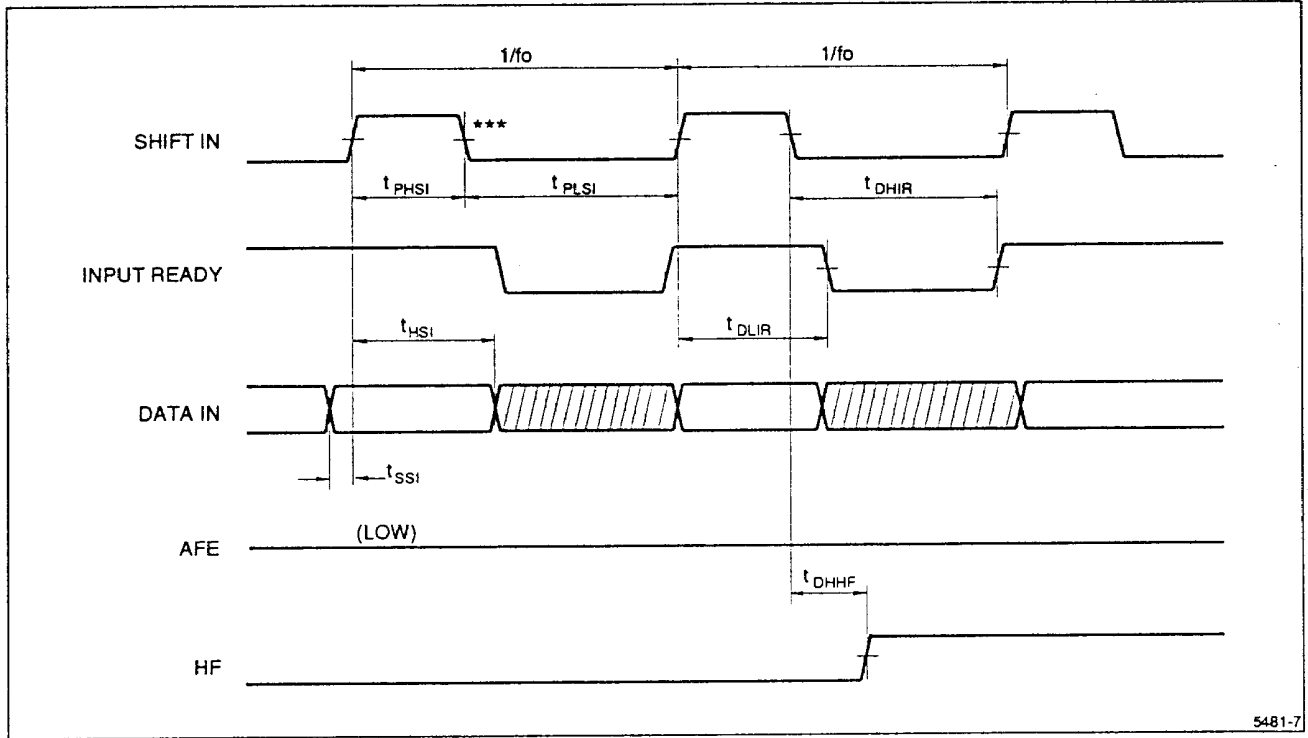
Figure 1. Data In Timing



** NOTE: FIFO Contains 9 Words

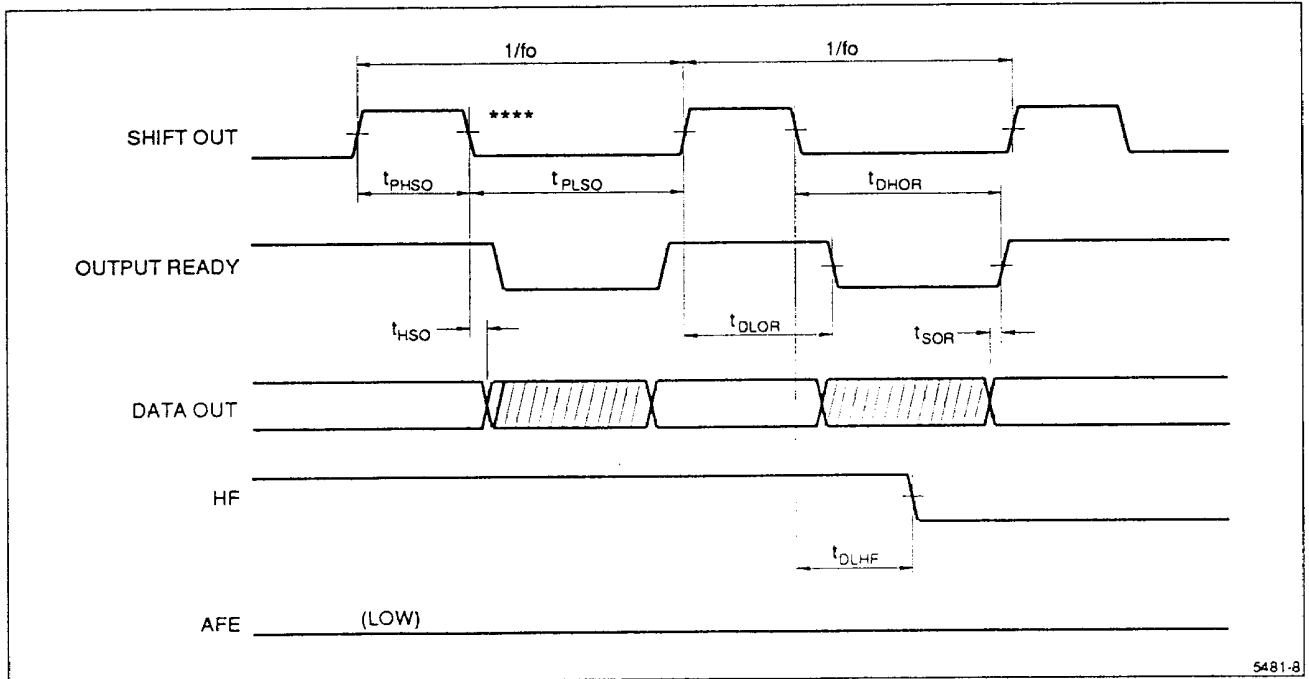
Figure 2. Data Out Timing

SWITCHING WAVEFORMS (cont'd)



*** NOTE: FIFO Contains 31 Words

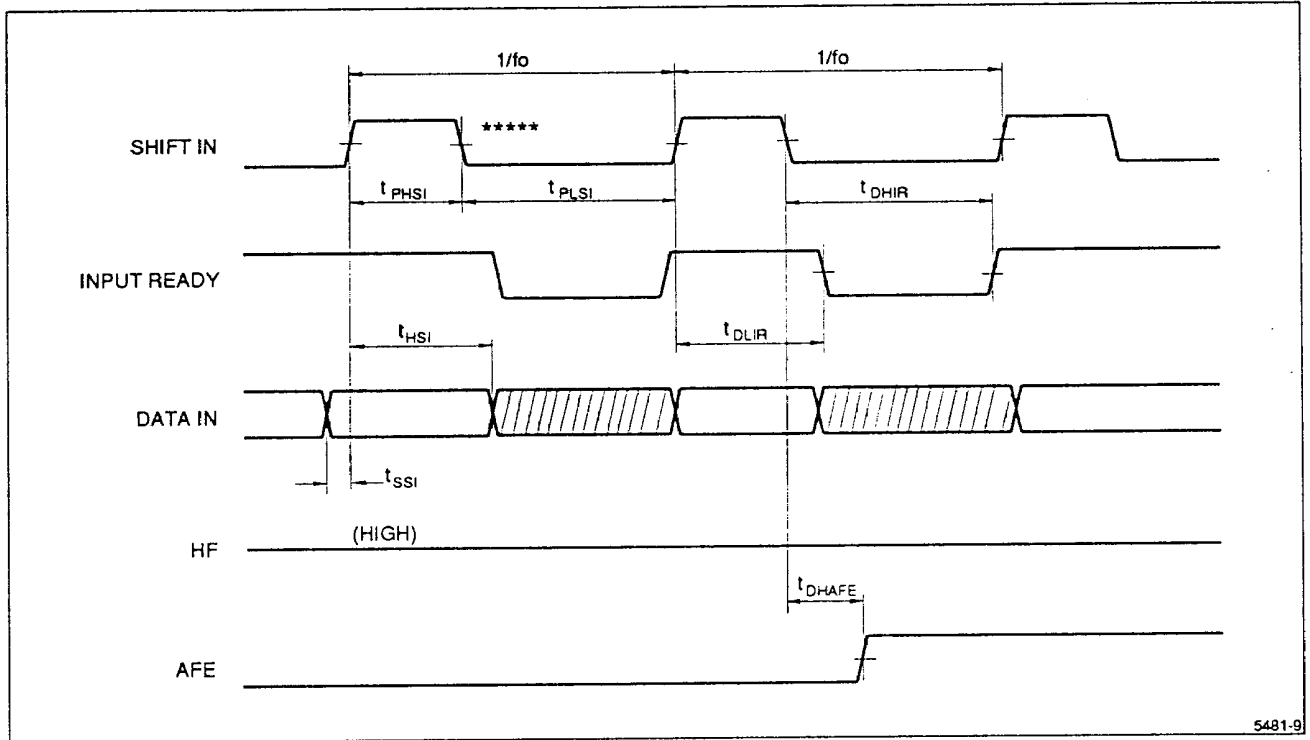
Figure 3. Data In Timing



**** NOTE: FIFO Contains 32 Words

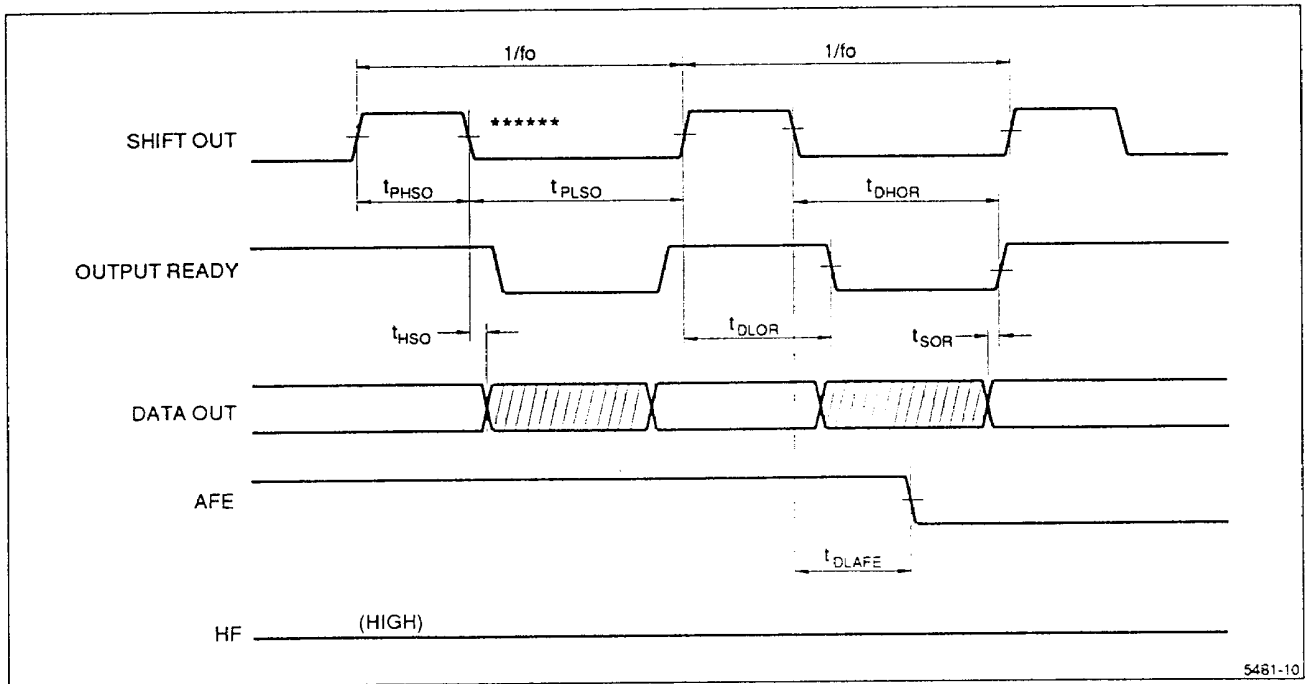
Figure 4. Data Out Timing

SWITCHING WAVEFORMS (cont'd)



***** NOTE: FIFO Contains 55 Words

Figure 5. Data In Timing



***** NOTE: FIFO Contains 56 Words

Figure 6. Data Out Timing

SWITCHING WAVEFORMS (cont'd)

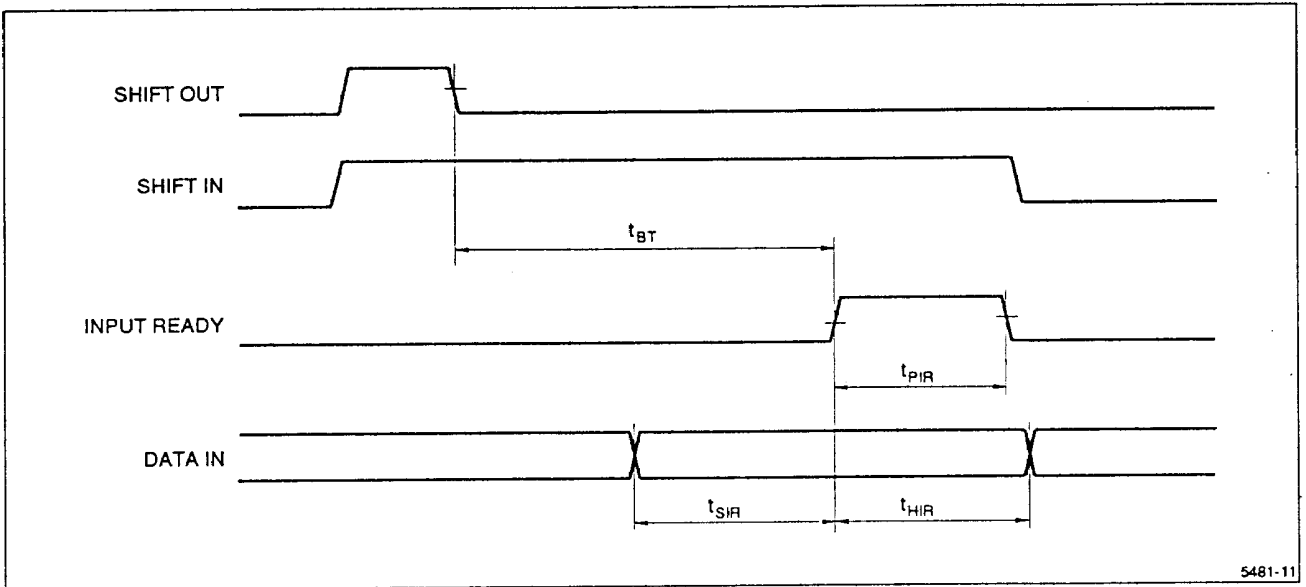


Figure 7. Bubblethrough Timing (Reading a Full FIFO)

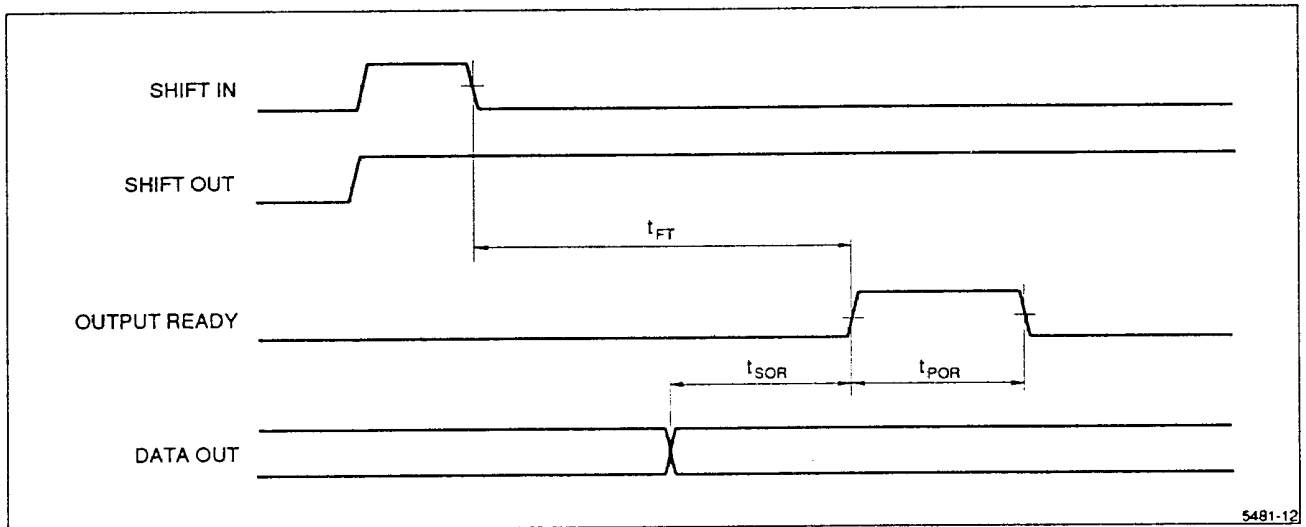
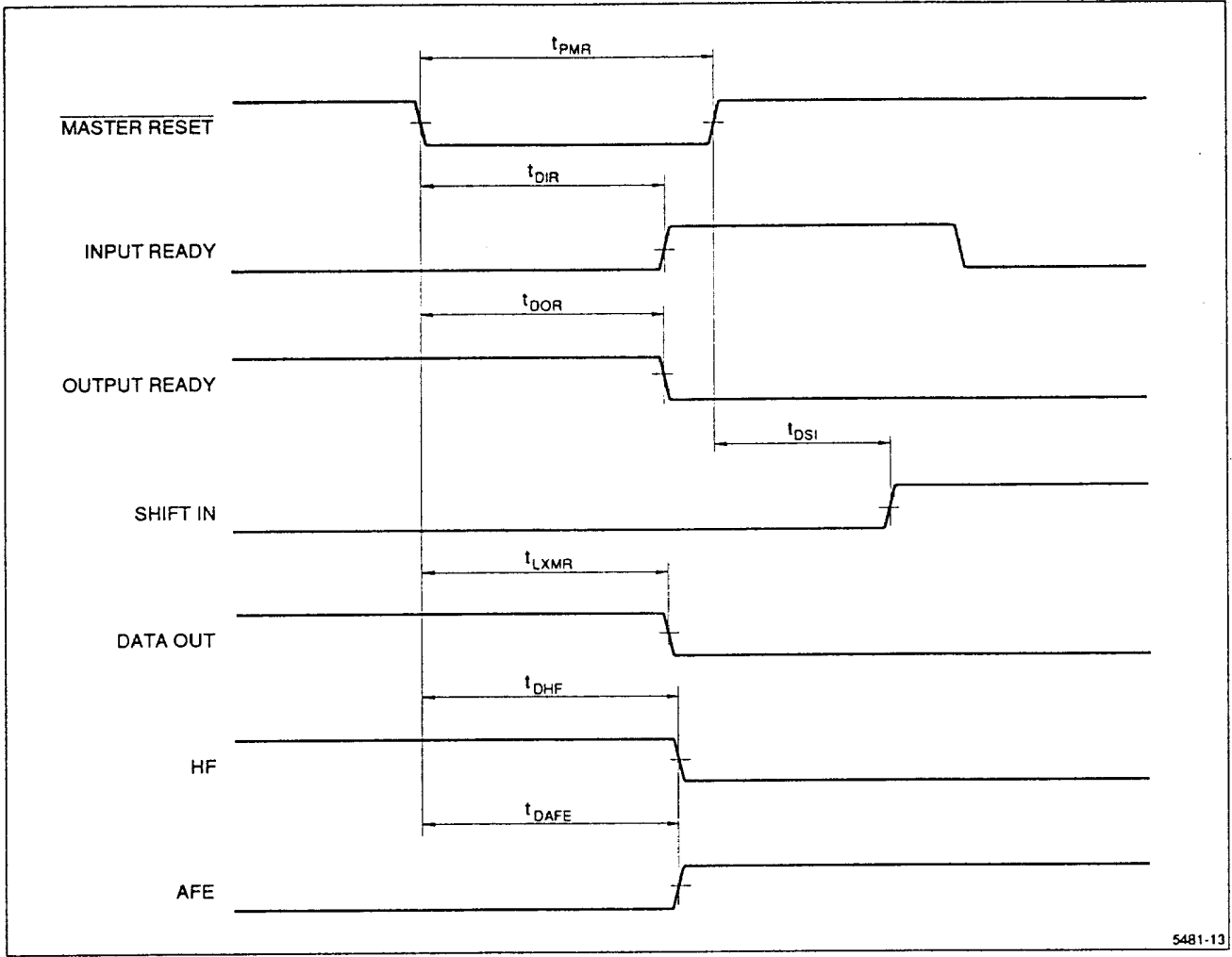


Figure 8. Fallthrough Timing (Writing an Empty FIFO)

SWITCHING WAVEFORMS (cont'd)



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Figure 9. Master Reset Timing

SWITCHING WAVEFORMS (cont'd)

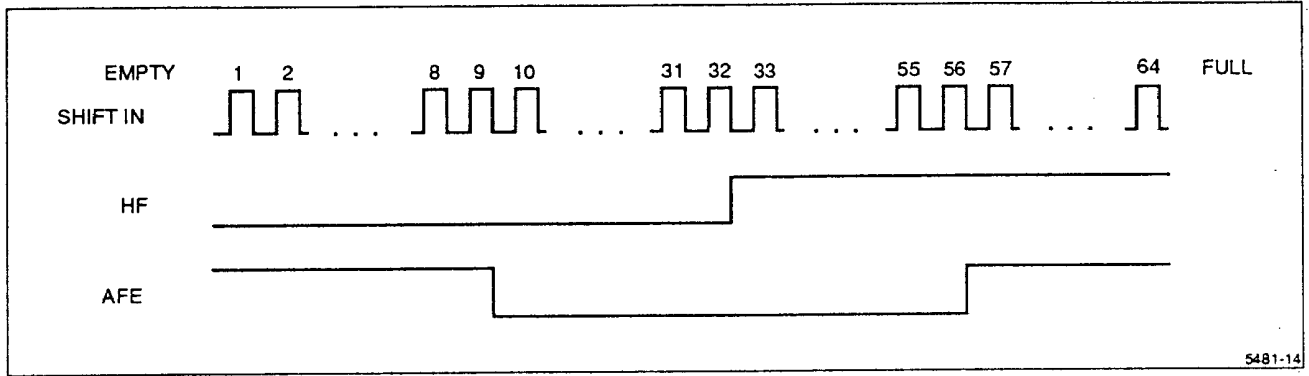


Figure 10. Shifting Words In

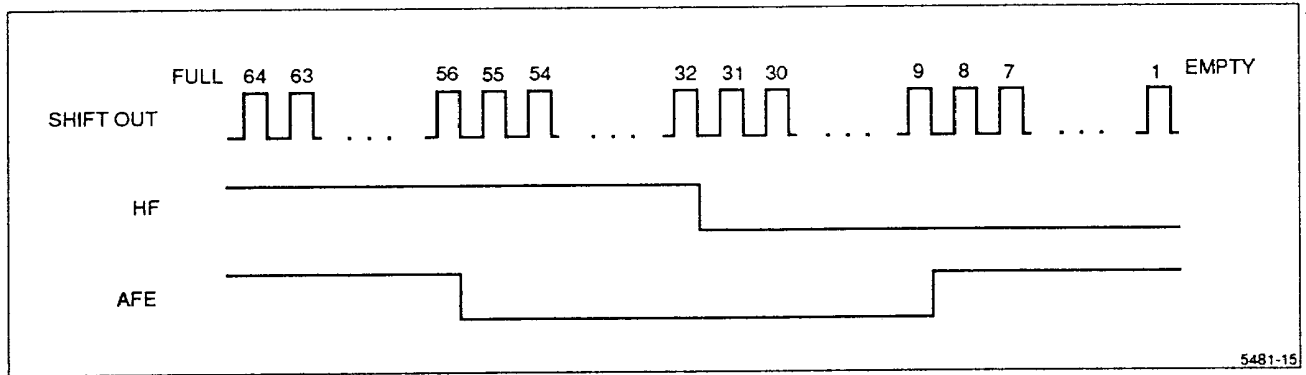


Figure 11. Shifting Words Out

FIFO Expansion

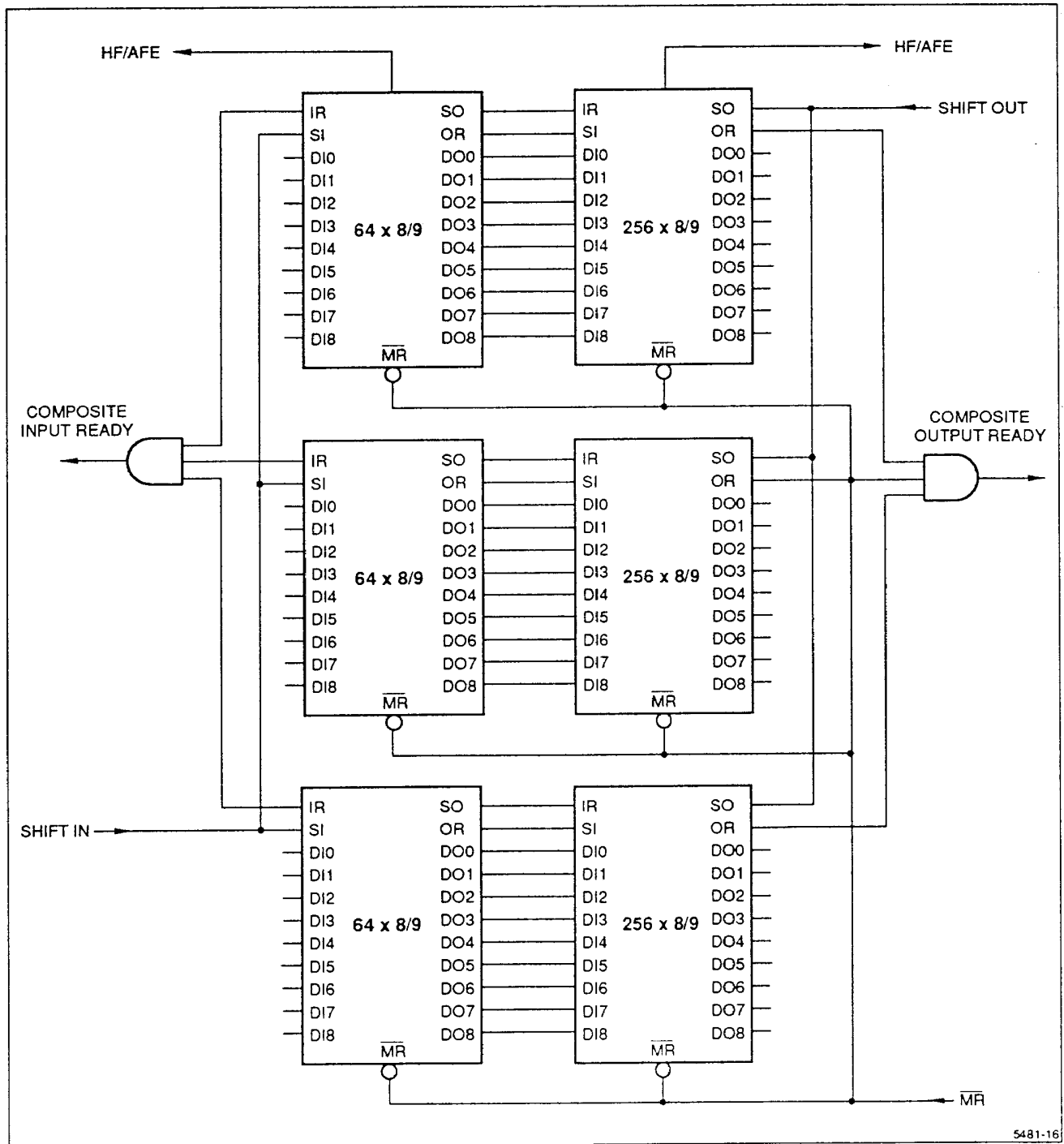


Figure 12. 320 x 24/27 Configuration
Using 64 x 8/9 (LH5481/91) & 256 x 8/9 (LH5485/95) FIFOs.

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FIFO Expansion (cont'd)

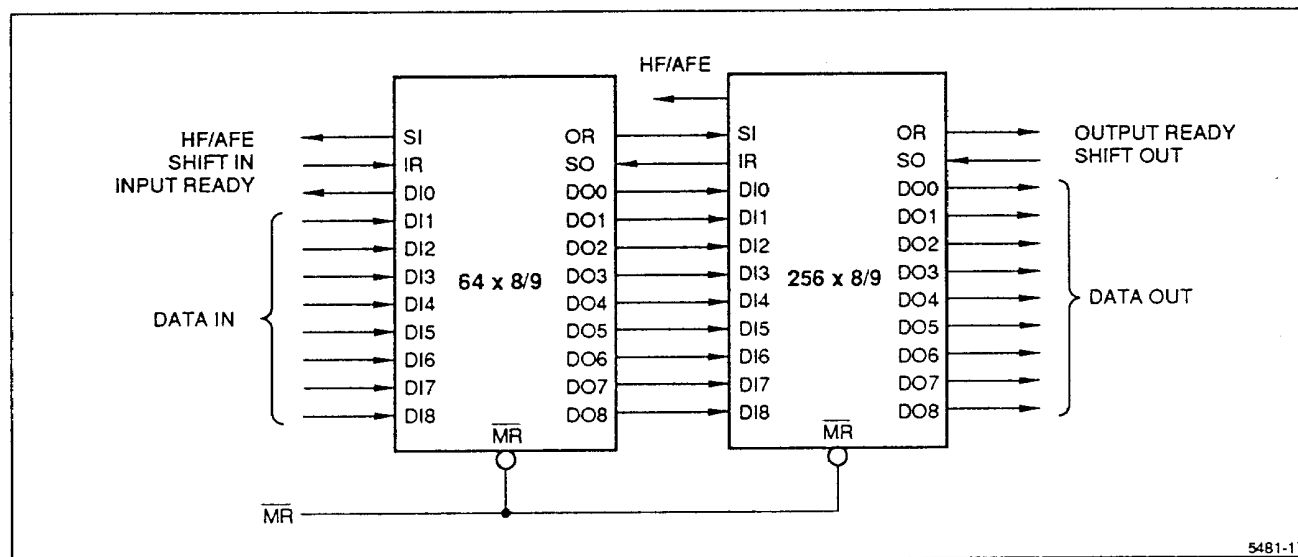


Figure 13. 128 x 8/9 Configuration

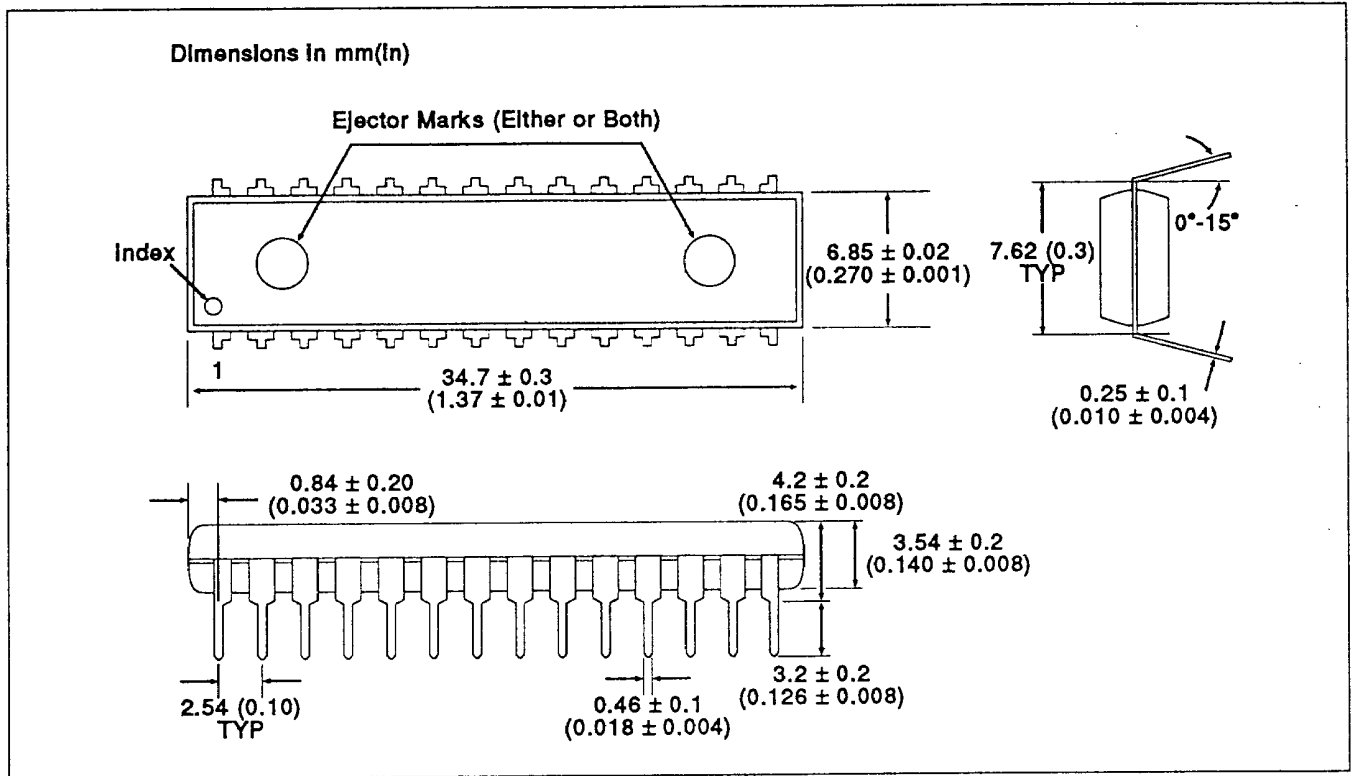
FIFOs are expandable in depth and width. However, in forming wider words, external logic is required to generate composite Input and Output Ready flags. This is due to the variation of delays of the FIFOs. The example circuit above uses simple AND gates as the external IR and OR generators. More complex logic may be required if fallthrough and bubblethrough pulses are needed by the external system.

FIFOs can easily be cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

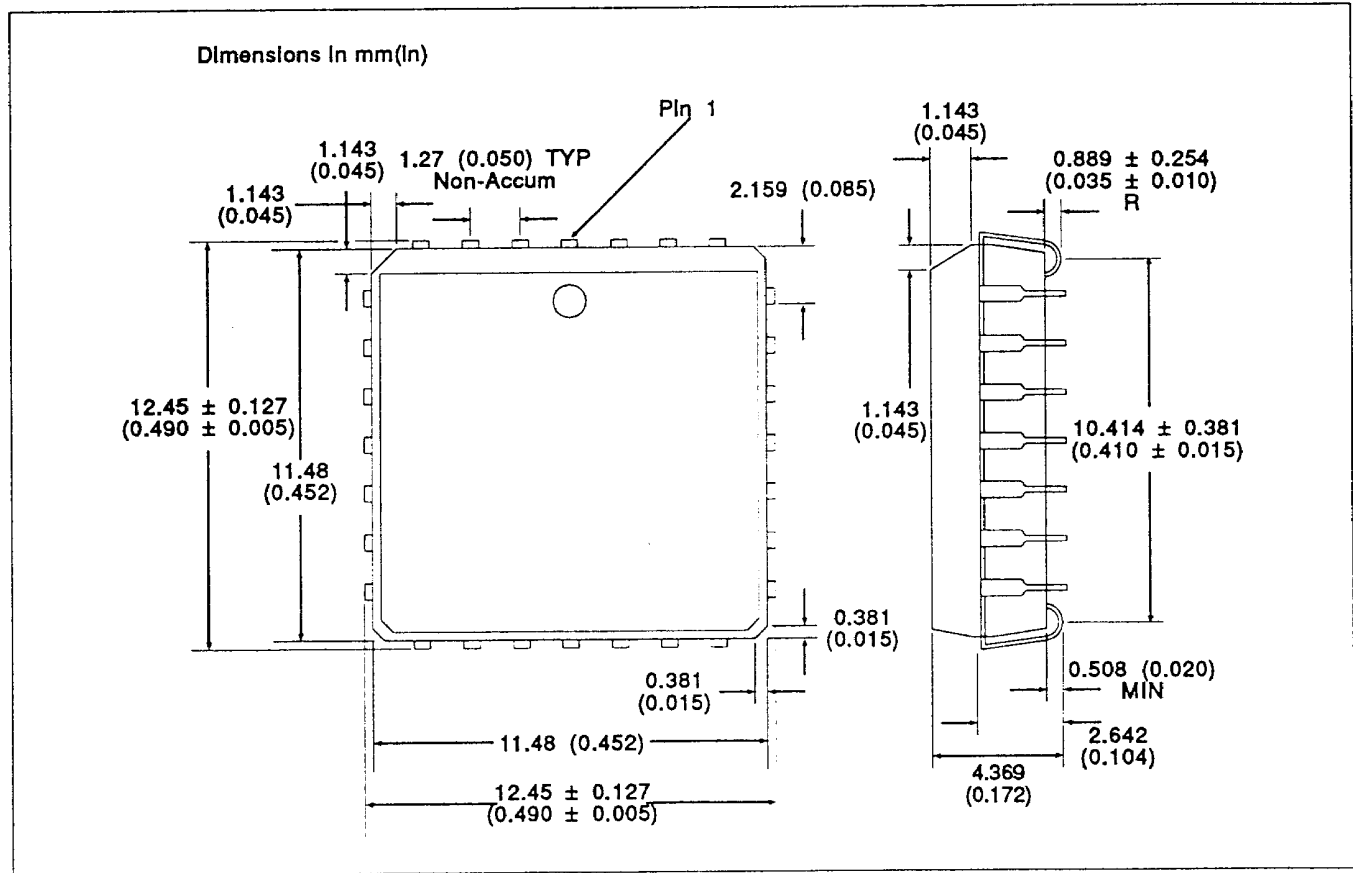
NOTES:

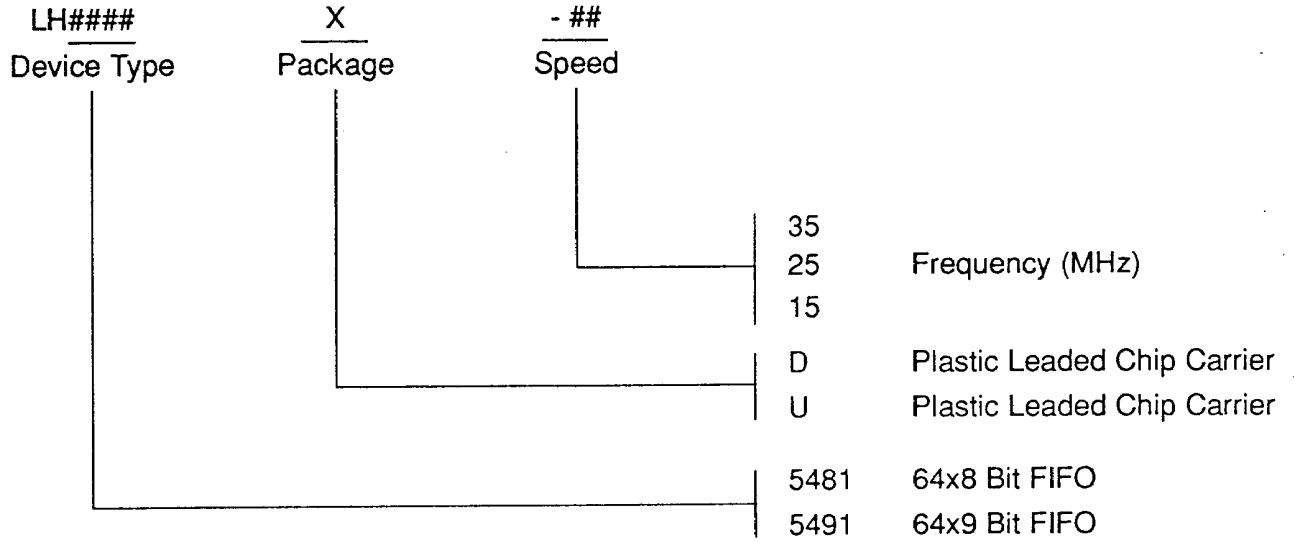
1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. All SHARP FIFOs will cascade with other SHARP FIFOs of the same architecture (i.e., 64x8/9 with 64x8/9 or 64x8/9 with 256x8/9). However, they may not cascade with FIFOs from other manufacturers.

PACKAGE DIAGRAM: 28-PIN 300-MIL DUAL IN-LINE PACKAGE



PACKAGE DIAGRAM: 28-PIN PLASTIC LEADED CHIP CARRIER





Examples: LH5481D-25 (64 x 8, 300 mil PDIP, 25 MHz)
 LH5491U-35 (64 x 9, PLCC, 35 MHz)

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