T-46-23-13

LH52256LL

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time:
  90 ns (MAX.)
- Low power consumption:
  Operating: 385 mW (MAX.)
  Standby: 220 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH52256LL is an ultra-low power CMOS-periphery static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

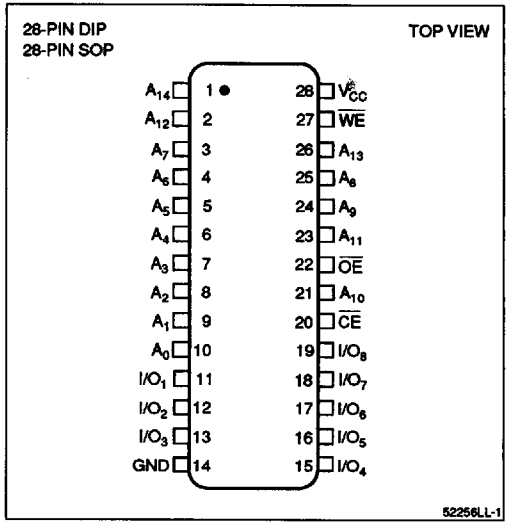


Figure 1. Pin Connections for DIP and SOP Packages

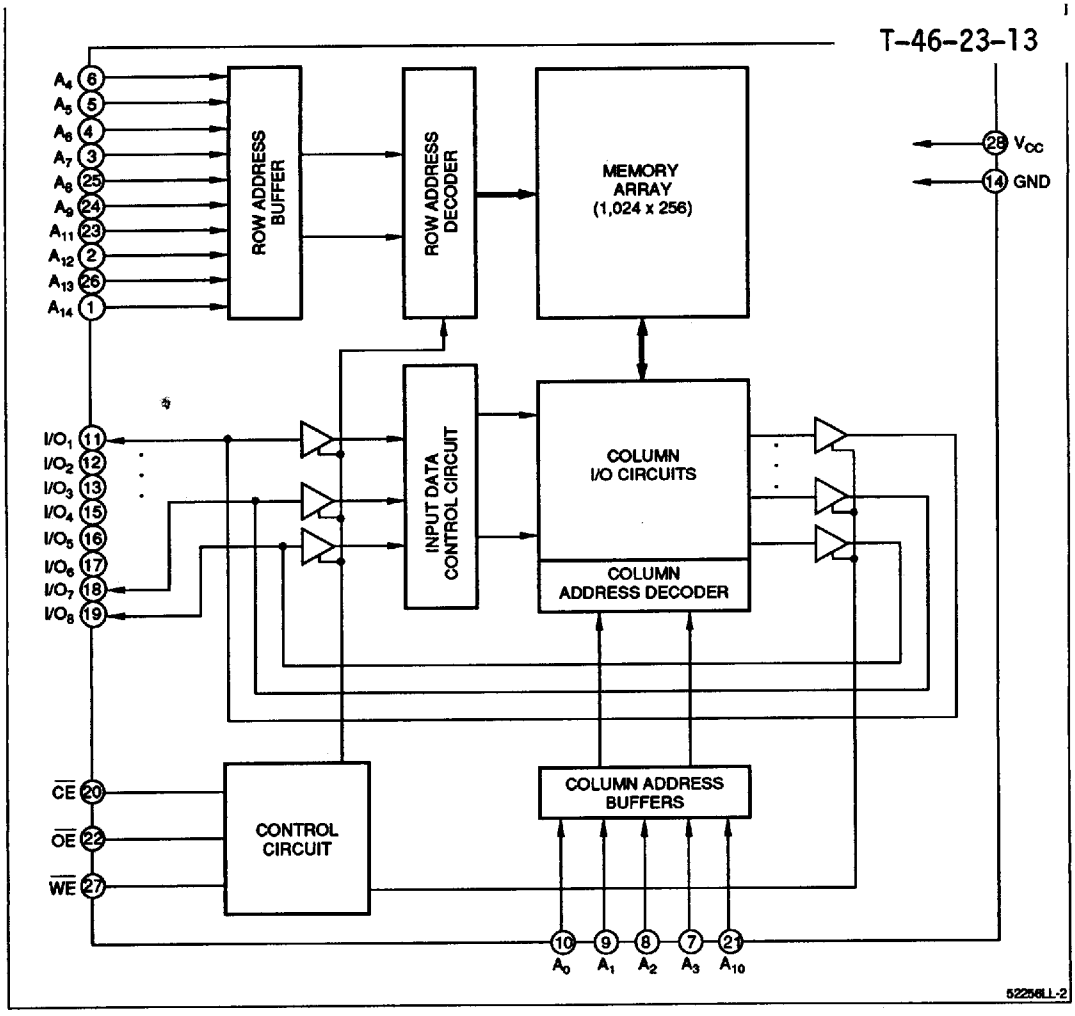


Figure 2. LH52256LL Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address inputs
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	
L	L	X	Write	D_{IN}	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	3.5	V_{CC} + 0.3	V
	V_{IL}	-0.3		+0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5 V_{IN} = 0 to V_{CC}			1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			70	mA
	I_{CC1}	V_{IH} = 3.5 V, V_{IL} = 0.6 V Outputs open			65	mA
	I_{CC2}	V_{IH} = 2.2 V, V_{IL} = 0.8 V Outputs open			70	mA
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V		2	40	µA
Output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	90		ns	
Address access time	t_{AA}		90	ns	
Chip enable access time	t_{ACE}		90	ns	
Output enable access time	t_{OE}		50	ns	
Output hold from address change	t_{OH}	10		ns	
Chip enable Low to output in Low-Z	t_{LZ}	5		ns	1
Output enable Low to output in Low-Z	t_{OLZ}	5		ns	1
Chip disable to output in High-Z	t_{HZ}	0	40	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	40	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	90		ns	
Chip enable to end of write	t_{CW}	55		ns	
Address valid to end of write	t_{AW}	80		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	55		ns	
Write recovery time	t_{WR}	5		ns	
Data valid to end of write	t_{DW}	30		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	5		ns	1
Write Low to output in High-Z	t_{WZ}	0	40	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	1.0 ns
Timing reference level	1.5 V
Output load conditions	1TTL gate, C_L = 100 pF (Includes scope and jig capacitance)

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V		2.0			V
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V, V_{CCDR} = 3.0 V	T_A = 25°C			1	µA
			T_A = 0 to 40°C			3	
			T_A = 0 to 70°C			20	
Chip disable to data retention	t_{CDR}			0			ns
Recovery time	t_R			t_{RC}*			ns

* t_{RC} = Read cycle time

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		8	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V		10	pF

NOTE:

1. This parameter is sampled and not production tested.

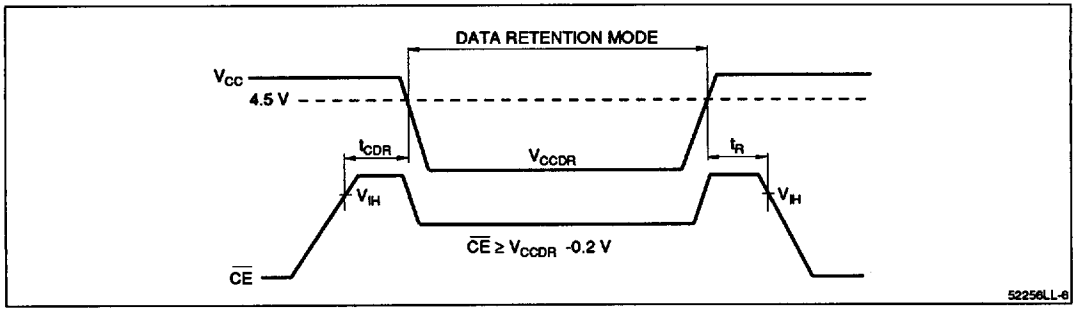


Figure 3. Low Voltage Data Retention

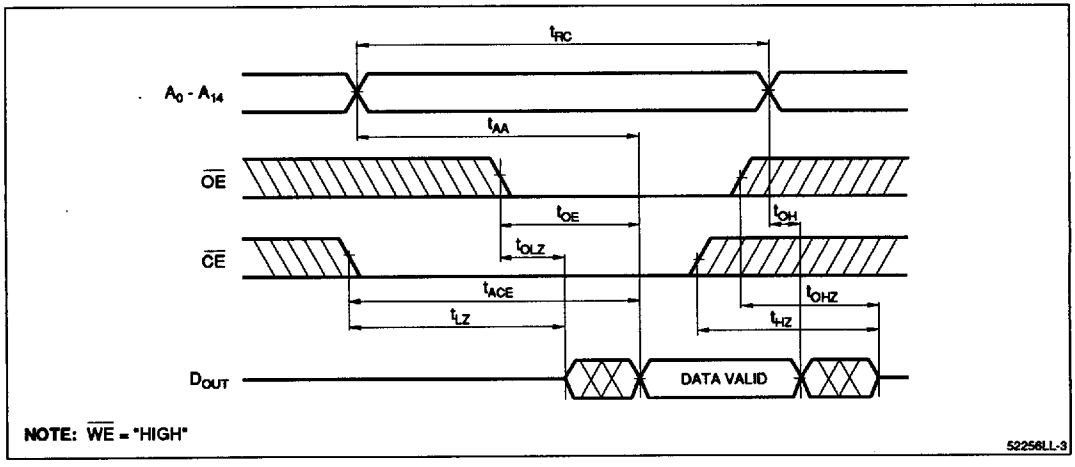
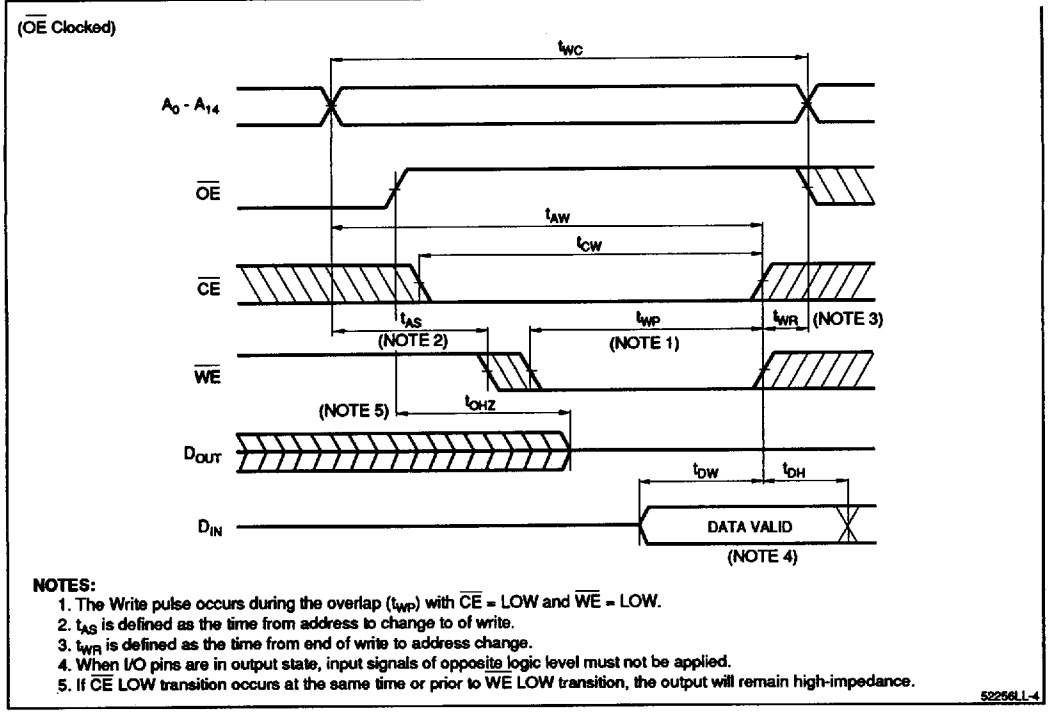


Figure 4. Read Cycle



NOTES:
1. The Write pulse occurs during the overlap (t_{WP}) with $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{AS} is defined as the time from address to change to of write.
3. t_{WR} is defined as the time from end of write to address change.
4. When I/O pins are in output state, input signals of opposite logic level must not be applied.
5. If $\overline{CE}$ LOW transition occurs at the same time or prior to $\overline{WE}$ LOW transition, the output will remain high-impedance.

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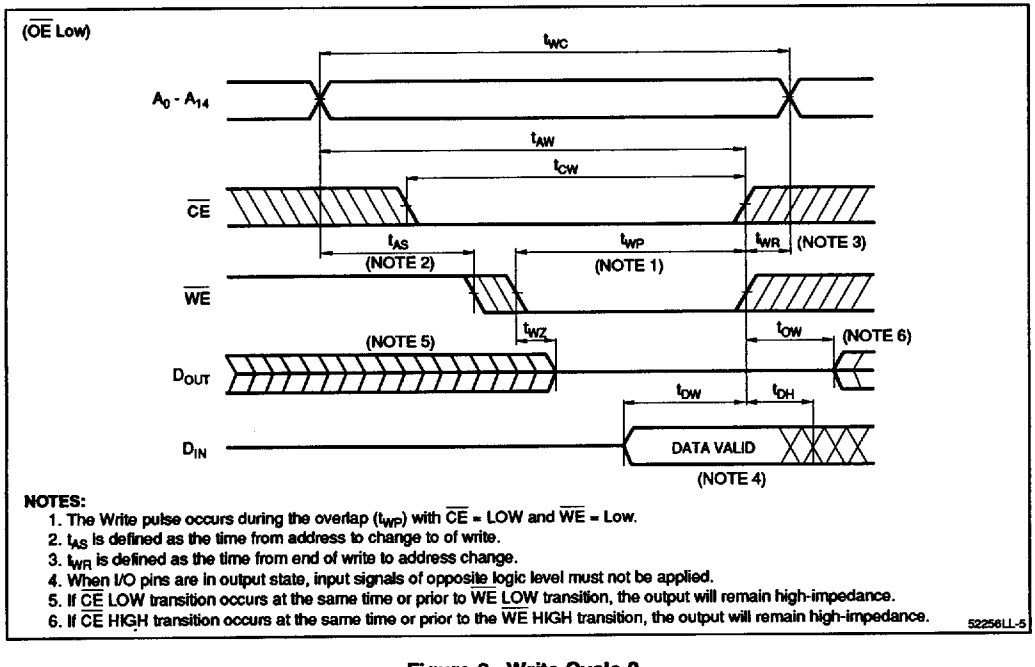
Figure 5. Write Cycle 1



NOTES:
1. The Write pulse occurs during the overlap (t_{WP}) with $\overline{CE}$ = LOW and $\overline{WE}$ = Low.
2. t_{AS} is defined as the time from address to change to of write.
3. t_{WR} is defined as the time from end of write to address change.
4. When I/O pins are in output state, input signals of opposite logic level must not be applied.
5. If $\overline{CE}$ LOW transition occurs at the same time or prior to $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

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Figure 6. Write Cycle 2

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ORDERING INFORMATION