LH5911/LH5912/LH5914

Preliminary Data Sheet

2K x 8 CMOS Dual Port RAM

Functional Description

The LH5911, LH5912 and LH5914 are dual port static RAMs that use true dual port memory cells to allow each port to independently access any location in memory. The LH5911 and LH5912 are "Master" devices which may be used alone in a single width configuration, or with one or more LH5914 "Slave" devices in wide word applications.

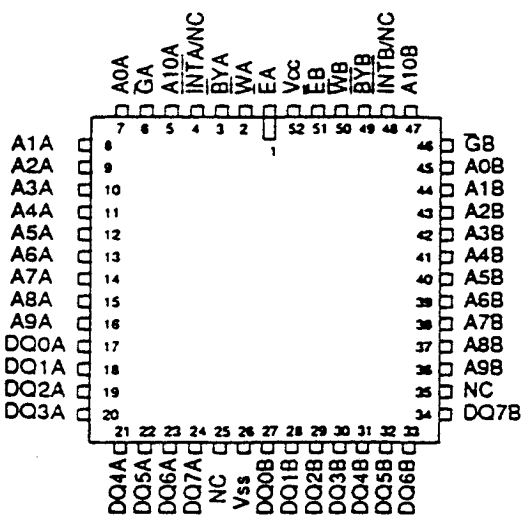
Each port provides a conventional byte wide interface to the system. Chip Enable ($\overline{E}$), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$) inputs independently control the function of each port. Additionally, Busy ($\overline{BY}$) and Interrupt ($\overline{INT}$) flags provide communication between the ports. An asserted $\overline{BY}$ output indicates that the internal arbitration logic has granted the opposite port access to the desired address. An asserted $\overline{INT}$ flag indicates the opposite port has requested attention by writing to a specific location. $\overline{BY}$ and $\overline{INT}$ are open drain outputs, allowing for wire or-ing of either function. $\overline{BY}$ is an output on Master type devices and an input on Slave type devices.

Power reduction circuitry has been designed into each port, controlled by $\overline{E}$. Battery backup is possible with data retention at voltages down to 2.0V in the Data Retention mode.

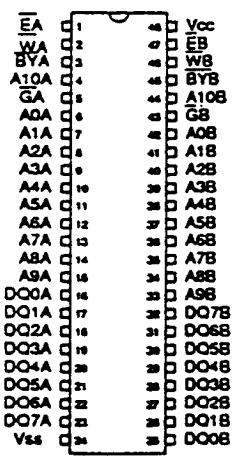
Features

- Fast Access Times - 35/45/55 ns
- True Dual Port Memory Array
- Fully Asynchronous
- LH5911: Master
  LH5912: Master with $\overline{INT}$
  LH5914: Slave
- Busy Output on Master
  Busy Input on Slave
- Data Retention Mode for Battery Backup
- 48-Pin DIP, 52-Pin DIP or 52-Pin PLCC
- $\overline{INT}$ Flag for Inter Port Communication (LH5912 Only)
- $\overline{E}$ Power Down
- "Transparent" Write
- TTL Compatible I/O

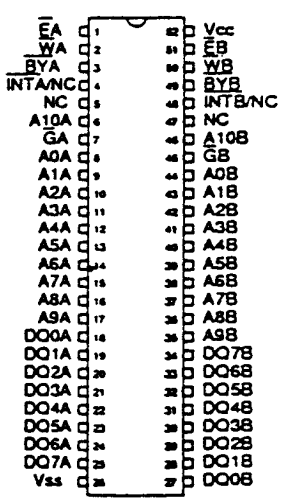
Pinout Diagrams



52 Pin PLCC - Top View

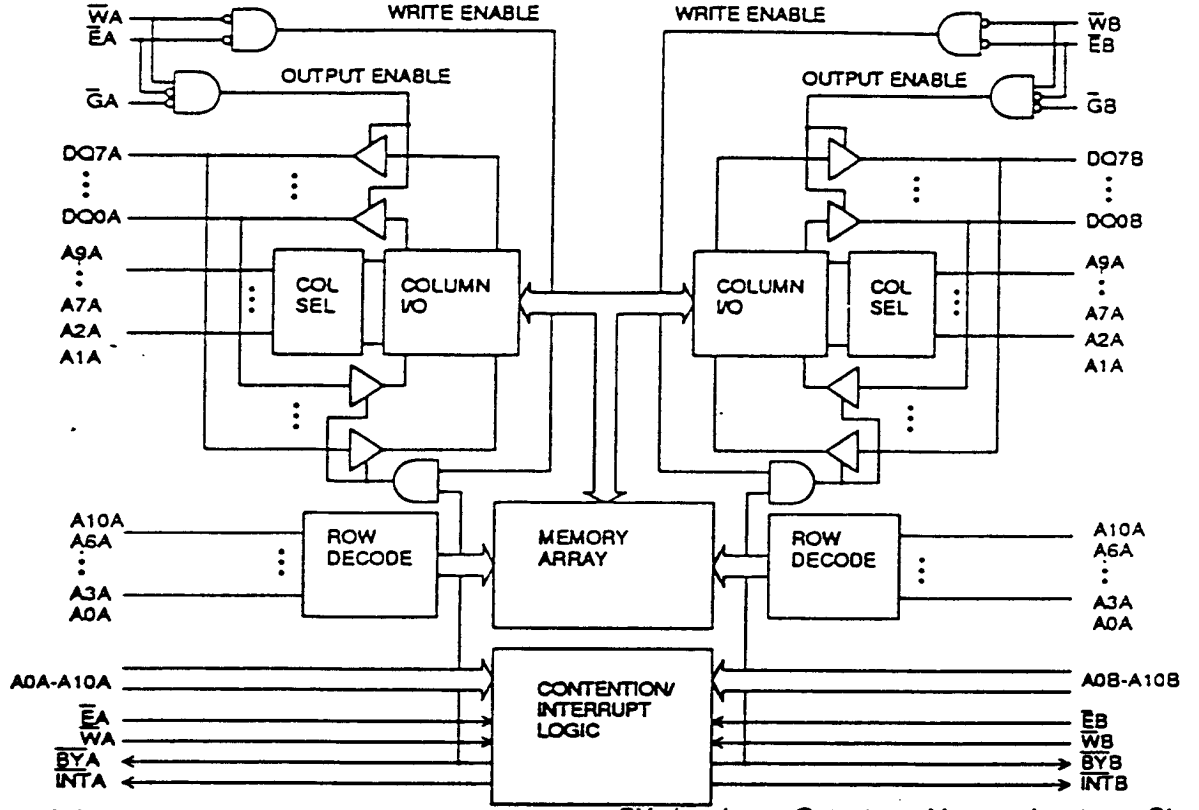


48 Pin DIP - Top View



52 Pin DIP - Top View

Block Diagram



BY signals are Outputs on Masters, Inputs on Slaves

Pin Identification

A_0-A_{10} . . . . . Address Inputs
DQ_0-DQ_7 . . . . . Data Inputs/Outputs
$\overline{E}$ . . . . . Chip Enable Input
$\overline{W}$ . . . . . Write Enable Input
$\overline{G}$ . . . . . Output Enable Input
$\overline{BY}$ . . . . . Busy Output (Input)
$\overline{INT}$/NC . . . . . Interrupt Output
V_{CC} . . . . . Positive Power Supply
V_{SS} . . . . . Ground

Notes:
Functions apply equally to Port A and Port B
V_{CC} and V_{SS} are common to both ports.
$\overline{BY}_A$ and $\overline{BY}_B$ are outputs on LH5911 and LH5912. $\overline{BY}_A$ and $\overline{BY}_B$ are inputs on LH5914.
$\overline{INT}_A$/NC and $\overline{INT}_B$/NC are $\overline{INT}_A$ and $\overline{INT}_B$ on LH5912, and NC on LH5914

Configuration Table

Part Number	Package	# of Pins	$\overline{BY}$	$\overline{INT}$/NC	Type
LH5911	DIP	48	Output	N/A	Master
LH5912	DIP	52	Open Drain Output	Open Drain Output	Master
LH5912	PLCC	52	Open Drain Output	N/A	Master
LH5914	DIP	48	Input	NC	Slave
LH5914	PLCC	52	Input	N/A	Slave

Absolute Maximum Ratings [1]

Supply Voltage to Ground Potential ..... -0.5V to 7V
Signal Pin Voltage Range ..... -0.5V to V_{CC}+0.5V
DC Output Current [2] ..... ± 40 mA
Storage Temperature Range ..... -65°C to 150°C
Power Dissipation (Package Limit) 1.0W

Operating Range

Symbol	Parameter	Min	Max	Unit
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic "0" Input Voltage [3]	-0.5	0.8	V
V_{IH}	Logic "1" Input Voltage	2.2	V_{CC}+0.5	V

DC Electrical Characteristics - Over Operating Range

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{CC1}	Operating Current [4]				150	mA
I_{SB1}	Standby Current	$\overline{E}_A$ and $\overline{E}_B \geq V_{IH}$			30	mA
I_{SB2}	Standby Current [4]	$\overline{E}_A$ or $\overline{E}_B \geq V_{IH}$			75	mA
I_{SB3}	Standby Current	$\overline{E}_A$ and $\overline{E}_B \geq V_{CC}$-0.2V			5	mA
I_{SB4}	Standby Current [4]	$\overline{E}_A$ or $\overline{E}_B \geq V_{CC}$-0.2V			65	mA
I_{LI}	Input Leakage Current	V_{CC}=5.5V, V_{in} = 0V to V_{CC}			2	µA
I_{LO}	I/O Leakage Current	V_{CC}=5.5V, V_{in} = 0V to V_{CC}			2	µA
V_{OH}	Output High Voltage	I_{OH} = -4.0mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA			0.4	V
V_{OL}	Output Low Voltage [5]	I_{OL} = 16.0mA			0.5	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC}$-0.2V	2.0			V
I_{DR}	Data Retention Current	V_{DR} = 3.0V			100	uA

AC Test Conditions

Input Pulse Levels ..... Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Ref. Levels 1.5V
Output Load, Timing Tests ..... See Figure, Page 5

Capacitance [6,7]

C_{IN} (Input Capacitance) 7pF
C_{DQ} (Output, Input/Output Capacitance) 7pF

See notes following "Switching Characteristics"

Switching Characteristics - Over Operating Range [8]

See Notes on Page 5

Symbol	Description	-35 Min	-35 Max	-45 Min	-45 Max	-55 Min	-55 Max	Units
Read Cycle								
t_{RC}	Read Cycle Timing	35		45		55		ns
t_{AA}	Address Access Time		35		45		55	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		35		45		55	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [6,9]	5		5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High Z [6,9]	3	15	3	20	3	25	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [6,9,10]	3	15	3	20	3	25	ns
t_{GHZ}	$\overline{G}$ High to Output High Z [6,9]	3	15	3	20	3	25	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [6]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [6]		20		25		30	ns
Write Cycle								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{EW}	$\overline{E}$ Low to End of Write	30		35		40		ns
t_{AW}	Address Valid to End of Write	30		35		40		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	30		35		40		ns
t_{DW}	Input Data Setup Time	15		20		25		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High Z [6,9]		15		20		25	ns
t_{WLZ}	$\overline{W}$ High to Output Active [6,9]	3		3		3		ns
Contention Timing								
t_{BL}	Contention Exists to $\overline{BY}$ Low	0	20	0	25	0	30	ns
t_{BH}	Contention Ends to $\overline{BY}$ High	0	20	0	25	0	30	ns
t_{WI}	$\overline{W}$ High Prior to $\overline{BY}$ High to Inhibit Write	15		15		15		ns
t_{DDD}	Data Flow Through Time (Transparent Write)		40		45		55	ns
t_{WDD}	Write LOW to Data Valid (Opposite Port)		50		55		65	ns
t_{APS}	Arbitration Priority Setup Time	10		10		10		ns
t_{WRD}	$\overline{W}$ Low to Read Data Invalid	5		5		5		ns
t_{BW}	$\overline{BY}$ Low to $\overline{W}$ Low for Slave	0		0		0		ns
t_{WV}	$\overline{BY}$ High to $\overline{W}$ High for Valid Write	15		20		25		ns
t_{BDD}	$\overline{BY}$ High to Valid Data		Note 11		Note 11		Note 11	ns
Interrupt Timing								
t_{INS}	Write Cycle begin to $\overline{INT}$ Low		25		30		35	ns
t_{WINS}	$\overline{W}$ Low to $\overline{INT}$ Low		25		30		35	ns
t_{INR}	Read Cycle Begin to $\overline{INT}$ High		25		30		35	ns
t_{GINR}	$\overline{G}$ Low to $\overline{INT}$ High		25		30		35	ns

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

3. Negative undershoots of up to 3.0V are permitted once per cycle.

4. I_{CC} and I_{SB} are dependent upon actual output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

5. Open Drain outputs only ($\overline{INT}$ and $\overline{BY}$).

6. Sample tested only.

7. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{in}=0V and V_{CC}=5.0V.

8. Switching Characteristics measurements performed at "AC Test Condition" levels.

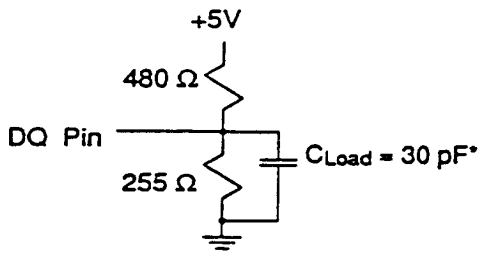
9. Active output to High-Z and High-Z to active output tests specified for a 500mV transition from steady state levels into the test load. C_{Load} is 5 pF for these tests.

10. t_{GLZ} (max) will result in Valid Data Out given that both t_{AA} and t_{EA} have been met.

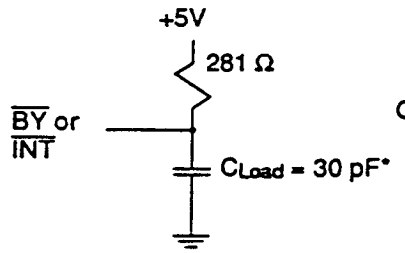
11. t_{BDD} is determined by the greater of 0, t_{WDD} - t_{WP}(actual) or t_{DDD} - t_{DW}(actual).

Equivalent Test Load

DQ Outputs

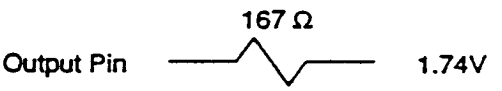


Open Drain Outputs



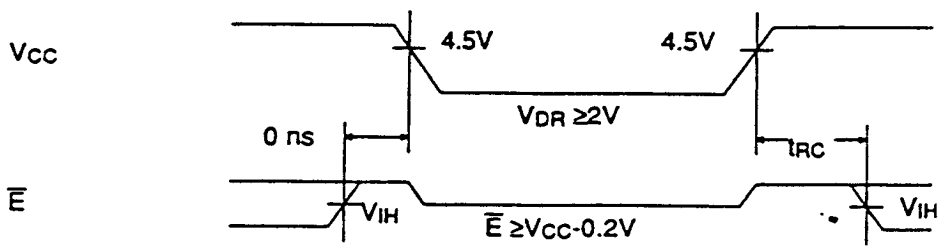
* Includes scope and jig capacitance.

Actual Test Load



Test fixture has an intrinsic 30 pF (min) capacitance

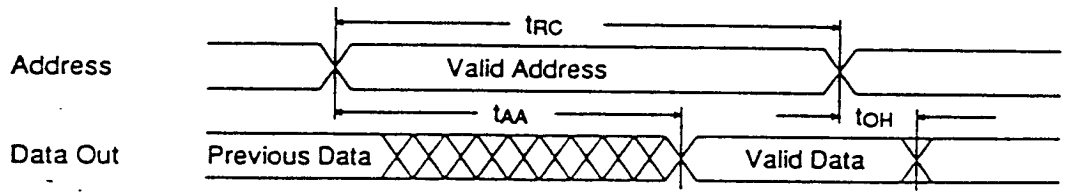
Data Retention Timing



Switching Waveforms - Read Cycle

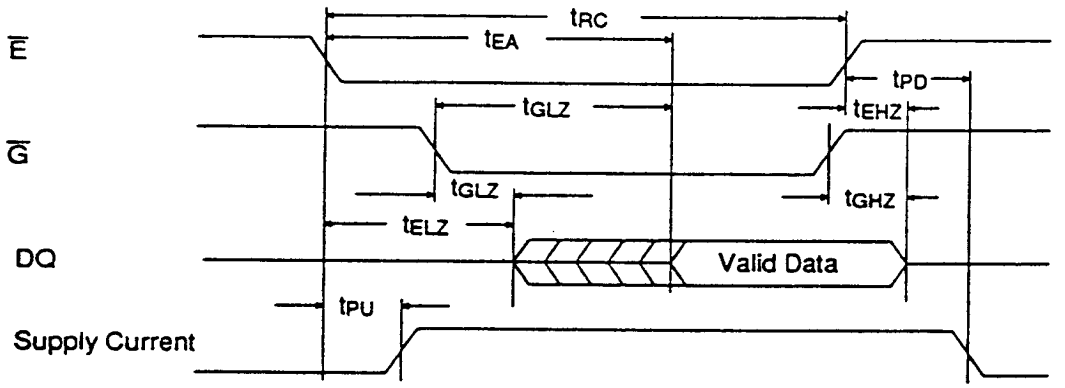
Read Cycle No. 1 - Either Port

Chip is in Read mode: $\overline{W}$ is HIGH and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of I/O implies that data lines are in the Low-Z state and that Data-out may not be valid.



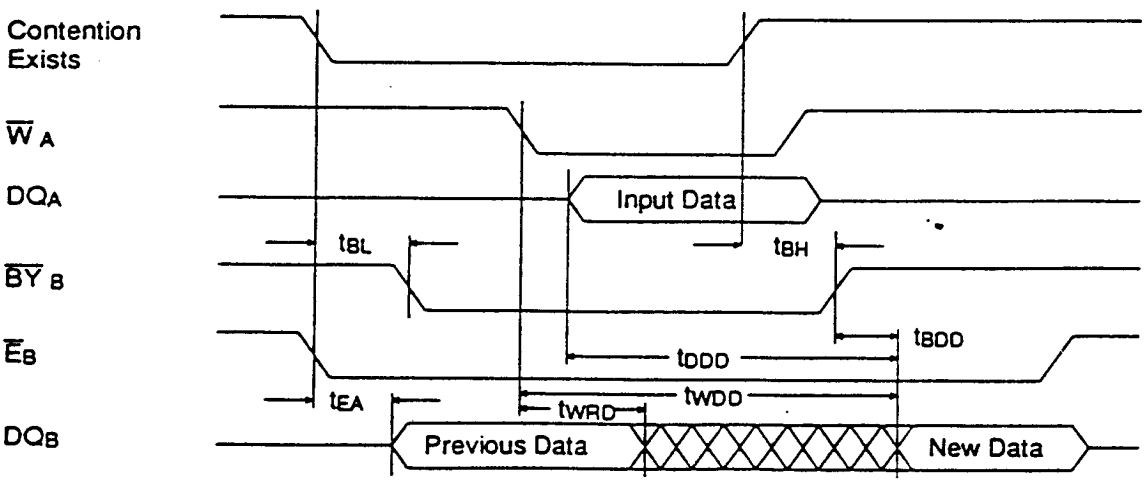
Read Cycle No. 2 - Either Port

Chip is in Read mode: $\overline{W}$ is HIGH. Timing illustrated for the case where addresses are valid before $\overline{E}$ goes LOW. Data-out is not specified to be valid until the latter of t_{EA} or t_{GLZ}(min), but may become valid as soon as t_{ELZ} or t_{GLZ}(max). Outputs will transition from high-Z to valid Data-out.



Read Cycle No. 3 - Read While $\overline{BY}$ (Transparent Write)

Contention occurs with Port A winning. Port A performs a Write (which is shown as a delayed Write in this example for illustration purposes). Port B performs a Read. Port B's DQ lines will follow the contents of the memory location, even as Port A changes it. DQ_B becomes indeterminate t_{WRD} after $\overline{W}_A$ goes low. DQ_B will reflect the new data t_{DDD} after it is presented to DQ_A. The new data on DQ_B will be guaranteed to be valid t_{BDD} after $\overline{BY}_B$ returns HIGH.

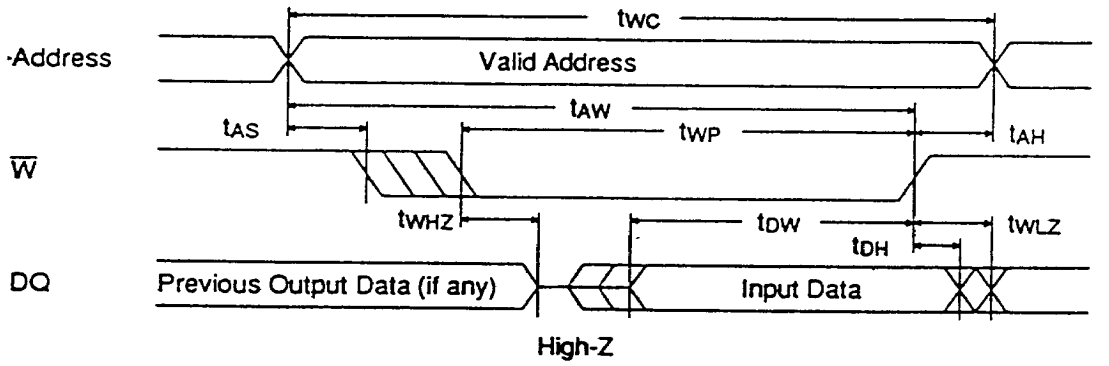


Switching Waveforms - Write Cycle

Addresses must be stable during Write Cycles. The outputs will remain in the high Z state if $\overline{W}$ is low when $\overline{E}$ goes low. If $\overline{G}$ is high, the outputs will remain in the high Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held high for all write cycles. This will prevent the outputs from becoming active during write cycles, preventing bus contention, thereby reducing system noise.

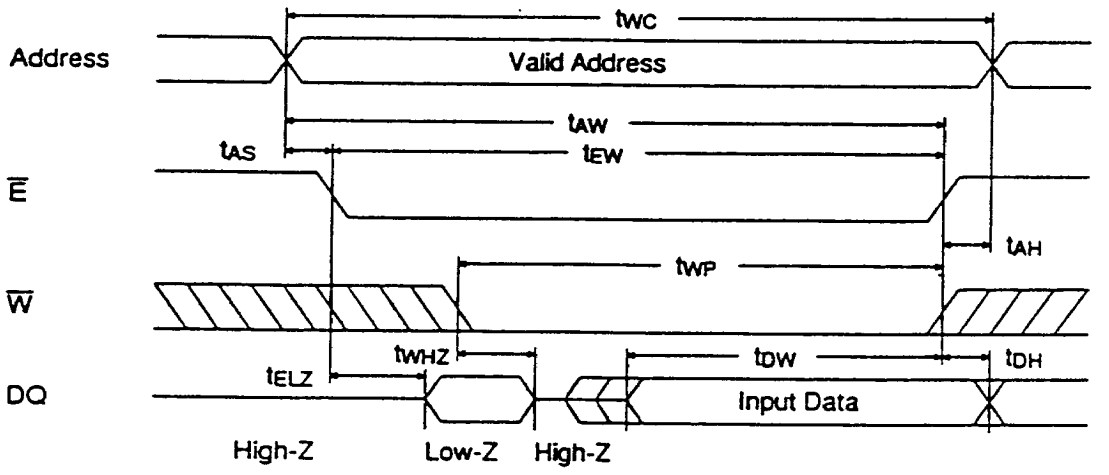
Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is low. The data bus may become driven t_{WLZ} after the rising edge of $\overline{W}$. Given that the addresses have not changed, the output data will be identical to the data previously written into the same location.



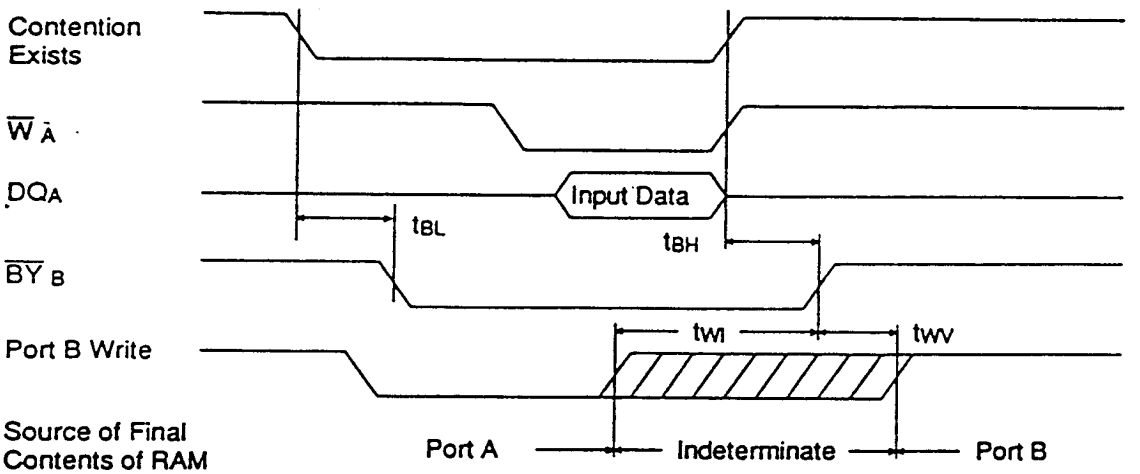
Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to low Z if the falling edge of $\overline{W}$ occurs after t_{ELZ} from the falling edge of $\overline{E}$.



Write Cycle No. 3 - Write While Busy

This cycle demonstrates contention occurring with Port A winning. Port A performs a Write. Port B performs a Write. The Write on Port A will occur normally. The Write on Port B will be inhibited while $\overline{BY}_B$ is LOW. If the Write on Port B is terminated prior to t_{WI}, it will have been completely inhibited. If the Write on Port B ends later than t_{WV} after $\overline{BY}_B$ returns HIGH, the data on DQ_B will have been written into the location. If the Write on Port B ends after t_{WI} but before t_{WV}, the data left in the addressed location may be indeterminate.



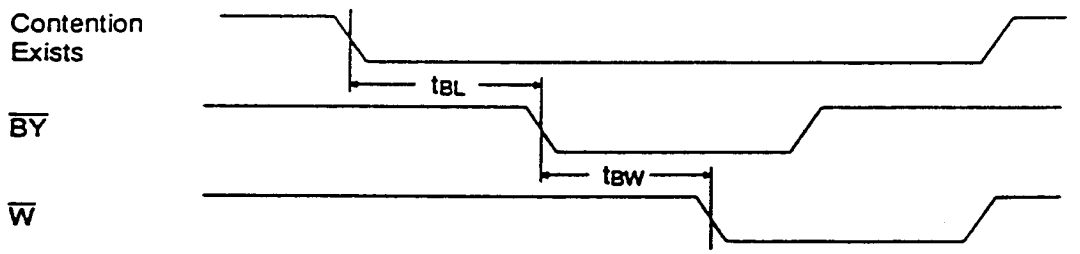
Width Expansion - Use of the Slave LH5914

Systems wider than 8 bits will need to use dual port RAMs in parallel. Slave LH5914 chips should be used for word width expansion to prevent the multiple dual port RAMs from resolving contention situations in favor of different ports. Systems which have the potential for contention to exist should use LH5912 52-pin Masters with $\overline{BY}$ outputs instead of LH5911 48-pin Standalone devices, which do not have $\overline{BY}$ outputs.

Slave device's $\overline{BY}$ pins are Inputs. Systems should connect the Master's $\overline{BY}$ open drain outputs to every Slave's $\overline{BY}$ inputs, with a pull up resistor to V_{CC}.

Slaves depend upon the Master to determine which port should be the winner in the event of contention. Read cycle timing is not effected, however special considerations must be made in Write cycle timing. To assure that the Slave has sufficient time to inhibit Write cycles on the losing port, the falling edge of $\overline{W}$ must occur at least t_{BW} after $\overline{BY}$ for that port goes low. Delaying the falling edge of $\overline{W}$ by $t_{BL}+t_{BW}$ from the falling edge of $\overline{E}$ will meet this constraint.

The same constraints apply with respect to properly ending Write cycles in Slaves as it does in Masters. Refer to the next section.



Contention Operation

Contention occurs when both ports attempt to address the same location at the same time. Proper system operation can be insured if each port's Busy output is used to generate wait states, stretching the cycle for the duration of the Busy condition.

In these examples, assume that Port A arrives first, so $\overline{BY}_B$ is asserted. All cycles on Port A will occur normally. Read cycles on Port B will occur normally, but Write cycles on Port B will be inhibited until its $\overline{BY}$ flag returns HIGH.

Port A Read; Port B Read. Reads to the same location will yield valid data on both ports.

Port A Write; Port B Read. The Write cycle on Port A will be successfully completed. The Read on Port B will follow the changing contents of the RAM location. Read Cycle 3 illustrates this operation. The assertion of $\overline{BY}_B$ during Port B's Read cycle signals that the data may be changing, and that Port B must wait for t_{BDD} for that data to be assured of being valid.

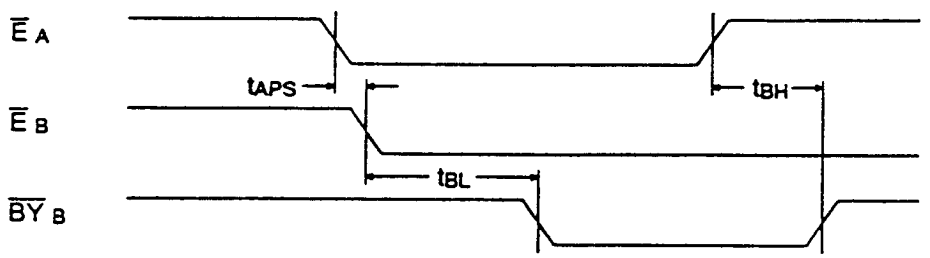
Port A Write; Port B Write. The winning port will successfully complete its Write, however the final contents of the location will depend upon the timing of the losing port. Port B's Write will be inhibited for the duration of the contention. If Port B's Write ends prior to t_{WI} of the rising edge of $\overline{BY}_B$, Port B's write will have been inhibited and Port A's data will remain in the RAM. If Port B extends its Write past t_{WV} after the rising edge of $\overline{BY}_B$, Port B's Write will be complete, and Port B's data will be left in the RAM. If Port B terminates its Write after t_{WI} but before t_{WV}, an incomplete Write may occur, leaving indeterminate data at the addressed byte.

Port A Read; Port B Write. The Read on Port A will inhibit the Write on Port B for the duration of the contention. The outcome of the inhibited Write on Port B will be determined in the same way as the case of "Port A Write; Port B Write", described above.

Switching Waveforms - Contention

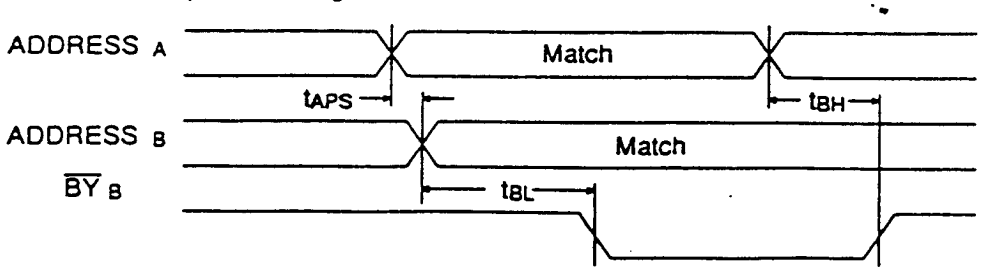
Addresses Match; $\overline{E}$ Arbitration

Both port's addresses match prior to $\overline{E}$ being asserted. If the falling edges of the $\overline{E}$s are within t_{APS}, the contention logic will determine which port's $\overline{BY}$ flag is asserted.



Both Ports Enabled; Address Arbitration

Both ports are enabled prior to the addresses matching. If the addresses are valid within t_{APS}, the contention logic will determine which port's $\overline{BY}$ flag is asserted.



Interrupt Operation - LH5912

LH5912s are 52 pin Masters that provide an interport communication scheme through the use of interrupt latches. Each port is assigned a unique "mailbox" within the memory address space. When a port writes to its own mailbox, the opposite port's latch is set, and its $\overline{INT}$ output goes LOW.

When Port A wants to send Port B a message, Port A writes to its own mailbox at memory location 7FF (A0-A10 = HIGH). This will cause $\overline{INT}_B$ to be set. Port B can then reset that interrupt by reading Port A's mailbox at location 7FF. $\overline{G}_B$ must be active during Port B's Read cycle for $\overline{INT}_B$ to be reset.

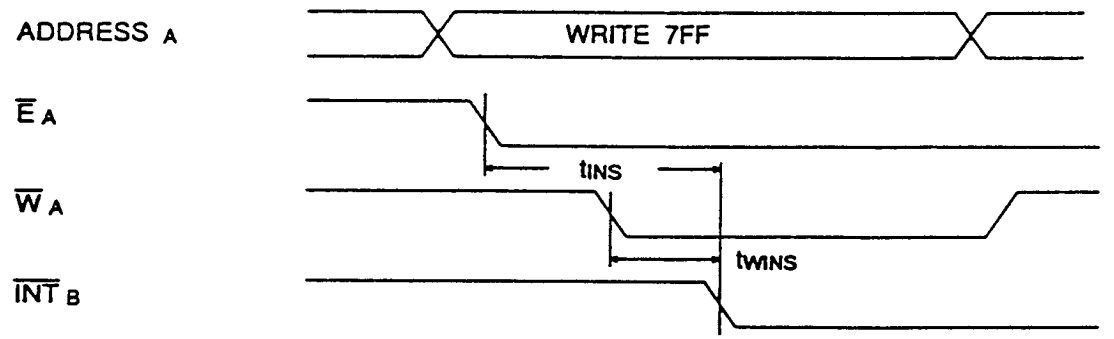
Port B's mailbox is at memory location 7FE (A0 = LOW, A1-A10 = HIGH). Port B sends a message to Port A by writing to its own mailbox, which sets $\overline{INT}_A$. Port A resets $\overline{INT}_A$ by reading Port B's mailbox. $\overline{G}_A$ must be active during Port A's Read cycle for $\overline{INT}_A$ to be reset.

The mailboxes are normal memory locations. Contention effects Read and Write operations to the mailbox locations in the same way it effects any other memory address.

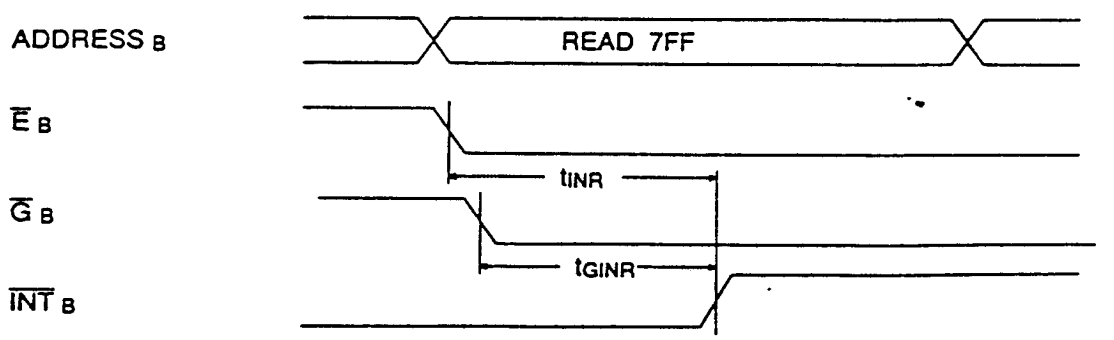
The $\overline{INT}$ outputs are active LOW open drain outputs. They should be pulled up to Vcc with a resistor, and may be wire ORed together. Systems not using the $\overline{INT}$ functions may leave the $\overline{INT}$ pins open. The $\overline{INT}$ latches should be reset upon power-up to assure they were not set during power-up.

Switching Waveforms - Interrupt

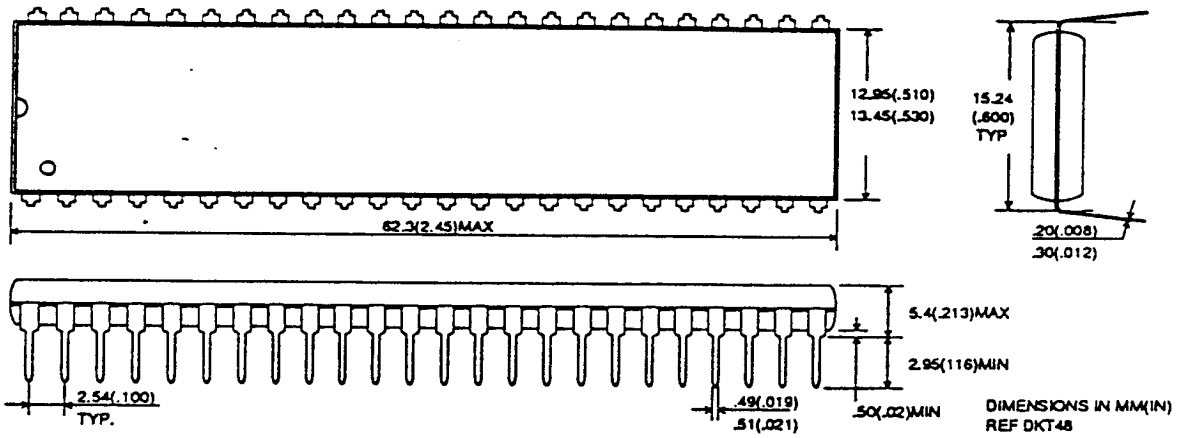
Port A Sets $\overline{INT}_B$



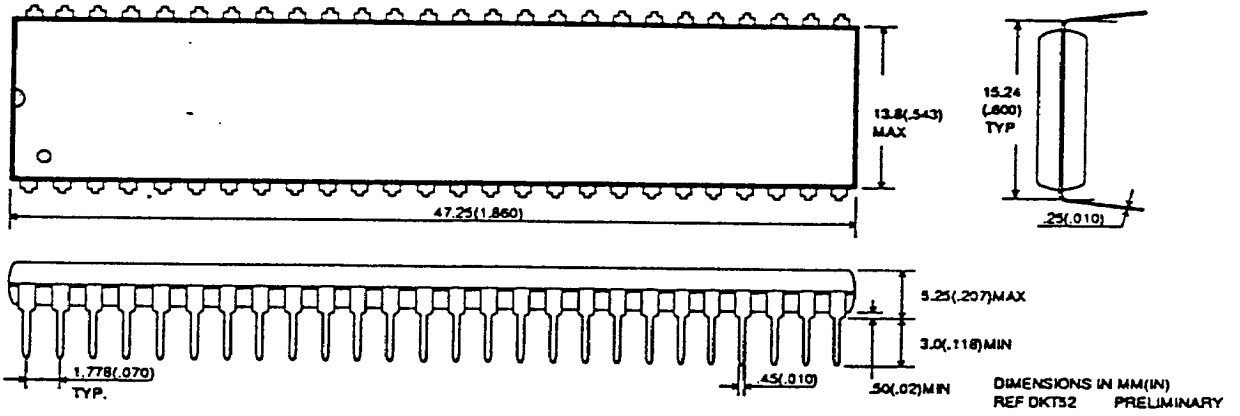
Port B Resets $\overline{INT}_B$



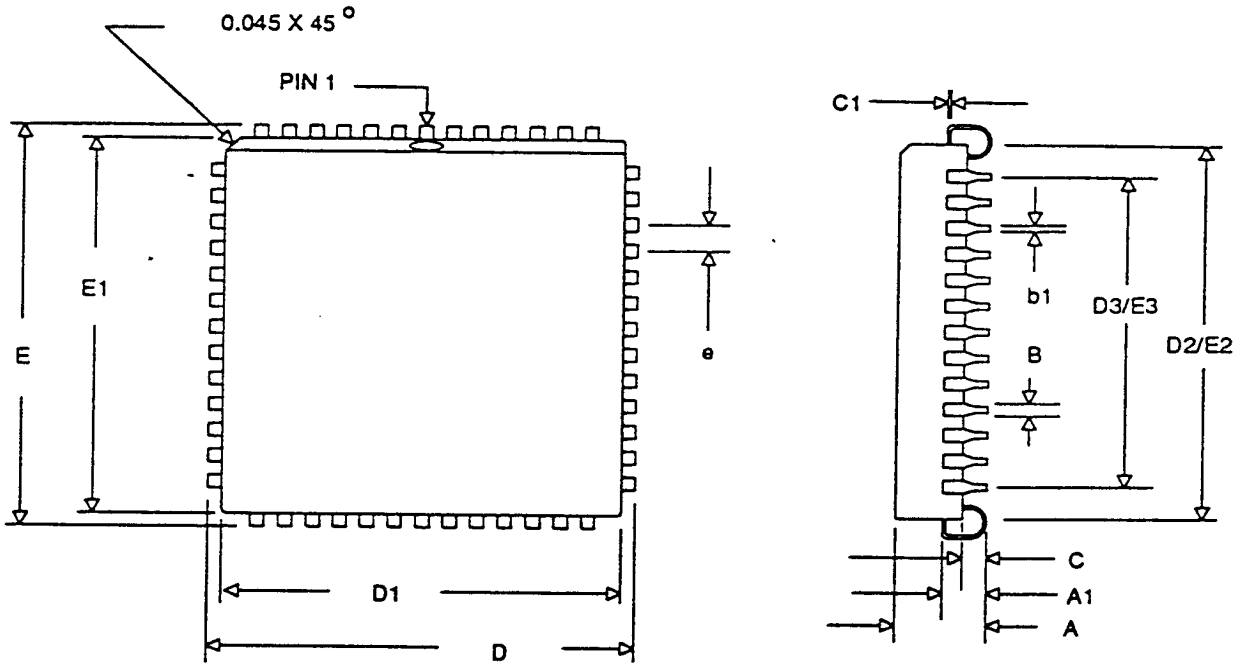
Package Diagram - 48-Pin Plastic DIP



Package Diagram - 52-Pin Plastic DIP



Package Diagram - 52-Pin PLCC



Symbol	inches		millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
B	0.026	0.032	0.66	0.82
b1	0.013	0.021	0.33	0.53
C	0.020	0.040	0.51	1.02
C1	0.008	0.012	0.20	0.30
D	0.785	0.795	19.94	20.19
D1	0.750	0.756	19.05	19.20
D2/E2	0.690	0.756	17.53	19.20
D3/E3	0.600 REF		15.24 REF	
E	0.785	0.795	19.94	20.19
E1	0.750	0.756	19.05	19.20
e	0.050 BSC		1.27 BSC	

Ordering Information

Ordering Code	Type	Speed	# Pins	Package Type
LH5911-35	Master	35ns	48	600-Mil Plastic DIP
LH5911-45	Master	45ns	48	600-Mil Plastic DIP
LH5911-55	Master	55ns	48	600-Mil Plastic DIP
LH5912-35	Master	35ns	52	600-Mil Plastic DIP
LH5912-45	Master	45ns	52	600-Mil Plastic DIP
LH5912-55	Master	55ns	52	600-Mil Plastic DIP
LH5912U-35	Master	35ns	52	PLCC
LH5912U-45	Master	45ns	52	PLCC
LH5912U-55	Master	55ns	52	PLCC
LH5914-35	Slave	35ns	48	600-Mil Plastic DIP
LH5914-45	Slave	45ns	48	600-Mil Plastic DIP
LH5914-55	Slave	55ns	48	600-Mil Plastic DIP
LH5914U-35	Slave	35ns	52	PLCC
LH5914U-45	Slave	45ns	52	PLCC
LH5914U-55	Slave	55ns	52	PLCC

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Organizational Structure	*SHARP Part Number*	*Access Time*	*Standby Current*	*Package Options*	*Sample Avail*	*Prod Avail*	*Data Sheet*	*Notes and Features*
Slow Static RAMs								
Low-Low Power Full CMOS								
256x4 (3.5 um CMOS)	LH5101	300/450 ns	10 uA	0.4" DIP	now	now	yes	
1Kx4 (3.5 um CMOS)	LH5114H	150 ns	5 uA	0.3" DIP	now	now	yes	
2Kx8 w/ CE, OE, WE (1.2um CMOS)	LH5115	55/70 ns	10 uA	0.6" DIP	call	call	yes	
	LH5115D	55/70 ns	10 uA	0.3" SDIP	call	call	pending	
	LH5115N	55/70 ns	10 uA	0.45" SOP	call	call	yes	
2Kx8 w/ CE, OE, WE (1.2um CMOS)	LH5116	100 ns	1 uA	0.6" DIP	now	now	yes	
	LH5116D	100 ns	1 uA	0.3" SDIP	now	now	yes	
	LH5116H	100 ns	1 uA	0.6" DIP	Aug '90	Sep '90	yes	*industrial temperature*
	LH5116N	100 ns	1 uA	0.45" SOP	now	now	yes	
2Kx8 w/ CE, CS, WE (1.2um CMOS)	LH5117	100 ns	1 uA	0.6" DIP	call	call	yes	
	LH5117D	100 ns	1 uA	0.3" SDIP	call	call	yes	
	LH5117H	100 ns	1 uA	0.6" DIP	call	call	yes	*industrial temperature*
	LH5117N	100 ns	1 uA	0.45" SOP	call	call	yes	
2Kx8 w/ WE, CE1, CE2 (1.2um CMOS)	LH5118	100 ns	1 uA	0.6" DIP	call	call	yes	
	LH5118D	100 ns	1 uA	0.3" SDIP	call	call	yes	
	LH5118H	100 ns	1 uA	0.6" DIP	call	call	yes	*industrial temperature*
	LH5118N	100 ns	1 uA	0.45" SOP	call	call	yes	
16Kx1 (1.2um CMOS)	LH5167	55/70 ns	1 uA	0.3" DIP	call	call	yes	
8Kx8 (1.2 um CMOS)	LH5160	100 ns	1 uA	0.6" DIP	now	now	yes	
	LH5160D	100 ns	1 uA	0.3" SDIP	now	call	yes	*industrial temperature*
	LH5160H	100 ns	1 uA	0.6" DIP	now	now	yes	
	LH5160HD	100 ns	1 uA	0.3" SDIP	now	call	yes	*industrial temperature*
	LH5160N	100 ns	1 uA	0.45" SOP	now	now	yes	
	LH5160HN	100 ns	1 uA	0.45" SOP	now	now	yes	*industrial temperature*
Slow 32Kx8 (1.0 um CMOS)	LH51256	100/120 ns	1 uA	0.6" DIP	Nov '90	Jan '91	yes	*industrial temperature*
	LH51256N	100/120 ns	1 uA	0.45"SOP	Oct '90	Dec '90	yes	*industrial temperature*
Slow 128Kx8 (0.8 um CMOS TFT)	LH511000	100/120 ns	1 uA	0.6" DIP	Jan '91	Apr '91	pending	*utilizes TFT technology*
	LH511000N	100/120 ns	1 uA	0.525" SOP	Jan '91	Apr '91	pending	*utilizes TFT technology*
	LH511000T	100/120 ns	1 uA	TSOP	Apr '91	Jul '91	pending	*utilizes TFT technology*
	LH511000TR	100/120 ns	1 uA	reverse TSOP	Apr '91	Jul '91	pending	*utilizes TFT technology*

Organizational Structure	SHARP Part Number	Access Time	Standby Current	Package Options	Sample Avail	Prod Avail	Data Sheet	Notes and Features
Slow Static RAMs								
Mixed MOS								
Slow 32Kx8 (1.2 um CMOS)	LH52256	120 ns	2 mA	0.6" DIP	now	now	yes	
	LH52256L	70/90/120 ns	100 uA	0.6" DIP	now	now	yes	
	LH52256NL	70/90 ns	100 uA	0.45" SOP	now	now	yes	
Slow 32Kx8 (1.0 um CMOS)	LH52250D	55/70/100 ns	1 mA	0.3" SDIP	now	now	yes	
Slow 128Kx8 (0.8 um CMOS)	LH521000E	55/70/100 ns	1 mA	0.4" DIP	1991	1991	yes	
	LH521000N	55/70/100 ns	1 mA	0.525" SOP	1991	1991	yes	
	LH521000	55/70/100 ns	1 mA	0.6" DIP	1991	1991	yes	
Fast Static RAMs								
64Kx1 (1.2 um CMOS)	LH5261	25/35 ns	1 mA	0.3" SDIP	now	now	yes	
256Kx1 (1.2 um CMOS)	LH52251	35/45 ns	1 mA	0.3" SDIP	now	now	yes	
256Kx1 (1.0 um CMOS)	LH52251AD	25/35 ns	1 mA	0.3" SDIP	now	now	yes	
	LH52251AK	25/35 ns	1 mA	0.3" SOJ	now	now	yes	
64Kx4 (1.2 um CMOS)	LH52252	35/45 ns	1 mA	0.3" SDIP	now	now	yes	*Chip Enable version*
64Kx4 (1.0 um CMOS)	LH52252AD	25/35 ns	1 mA	0.3" SDIP	now	now	yes	*Chip Enable version*
	LH52252AK	25/35 ns	1 mA	0.3" SOJ	now	now	yes	*Chip Enable version*
64Kx4 (0.8 um CMOS)	LH52252BD	15/20 ns	1 mA	0.3" SDIP	1991	1991	pending	*Chip Enable version*
	LH52252BK	15/20 ns	1 mA	0.3" SOJ	1991	1991	pending	*Chip Enable version*
64Kx4 (1.2 um CMOS)	LH52255	35/45 ns	n/a	0.3" SDIP	now	now	yes	*Chip Select version*
64Kx4 (0.8 um CMOS)	LH52253D	15/20 ns	1 mA	0.3" SDIP	Apr '91	May '91	pending	*Output Enable version*
	LH52253K	15/20 ns	1 mA	0.3" SOJ	Apr '91	May '91	pending	*Output Enable version*
32Kx8 (1.0 um CMOS)	LH52258D	35/45 ns	1 mA	0.3" SDIP	now	now	yes	
	LH52258K	35/45 ns	1 mA	0.3" SOJ	now	Jul '90	yes	
	LH52258N	45 ns	1 mA	0.45" SOP	Jun '90	Sep '90	pending	
32Kx8 (0.8 um CMOS)	LH52258AD	15/20/25 ns	1 mA	0.3" SDIP	1991	1991	pending	
	LH52258AK	15/20/25 ns	1 mA	0.3" SOJ	1991	1991	pending	
256Kx4 (0.8 um CMOS)	LH521002E	20/25/35 ns	1 mA	0.4" DIP	Feb '91	May '91	yes	
	LH521002K	20/25/35 ns	1 mA	0.4" SOJ	Aug '90	Aug '90	yes	*limited volume til October*
128Kx8 (0.8 um CMOS)	LH521008E	20/25/35 ns	1 mA	0.4" DIP	Mar '91	May '91	yes	
	LH521008K	20/25/35 ns	1 mA	0.4" SOJ	Sep '90	Jan '91	yes	

Organizational Structure	SHARP Part Number	Access Time	Standby Current	Package Options	Sample Avail	Prod Avail	Data Sheet	Notes and Features
Dual Port Static RAMs								
2Kx8 Dual Port, Master	LH5911	35/45/55 ns	5 mA *	48-pin DIP	Call	Jul '90	yes	*Compatible w/ IDT7132*
2Kx8 Dual Port, Master w/ Int	LH5912U	35/45/55 ns	5 mA *	52-pin PLCC	Dec '90	Feb '91	yes	*Compatible w/ IDT71321*
2Kx8 Dual Port, Slave	LH5914	35/45/55 ns	5 mA *	48-pin DIP	Jul '90	Aug '90	yes	*Compatible w/ IDT7142*
	LH5914U	35/45/55 ns	5 mA *	52-pin PLCC	Dec '90	Feb '91	yes	*Compatible w/ IDT7142*
4Kx8 Dual Port	LH5920	35/45/55 ns	5 mA *	48-pin DIP	Nov '90	Jan '91	yes	*Compatible w/ IDT7134*
	LH5920U	35/45/55 ns	5 mA *	52-pin PLCC	Nov '90	Jan '91	yes	*Compatible w/ IDT7134*
4Kx8 Dual Port, Master w/ Int	LH5926U	35/45/55 ns	5 mA *	52-pin PLCC	Sep '90	Oct '90	yes	*w/ Arbitration*
4Kx8 Dual Port, Slave	LH5924U	35/45/55 ns	5 mA *	52-pin PLCC	Oct '90	Nov '90	yes	*w/ Arbitration*
8Kx8 Dual Port w/ Semaphore	LH5933U	25/35/45 ns	TBD	52-pin PLCC	Feb '91	Apr '91	pending	
		* *Dual Port SRAM Standby Current with both Enable inputs => Vcc - 0.2 V across the full operating temperature range*						
Wide-Word Static RAMs								
Slow 16Kx18 (0.8 um CMOS)	LH52270	45/55 ns	TBD	48-pin DIP	May-91	Jul-91	pending	
	LH52270U	45/55 ns	TBD	52-pin PLCC	May-91	Jul-91	pending	
Fast 16Kx18 (0.8 um CMOS)	LH52278	20/25/30 ns	TBD	48-pin DIP	May-91	Jul-91	pending	
	LH52278U	20/25/30 ns	TBD	52-pin PLCC	May-91	Jul-91	pending	
Slow 64Kx18 (0.8 um CMOS)	LH521020	45/55 ns	TBD	48-pin DIP	Apr-91	Jun-91	pending	
	LH521020U	45/55 ns	TBD	52-pin PLCC	Apr-91	Jun-91	pending	
Fast 64Kx18 (0.8 um CMOS)	LH521028	20/25/30 ns	TBD	48-pin DIP	Mar-91	May-91	yes	
	LH521028U	20/25/30 ns	TBD	52-pin PLCC	Mar-91	May-91	yes	