

# KM68BV4002

# BiCMOS SRAM

## 512K x 8 Bit High Speed BiCMOS Static RAM(3.3V Operating)

### FEATURES

- Fast Access Time 12,15,20 ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60 mA(Max.)
  - (CMOS): 30 mA(Max.)
  - Operating KM68BV4002J-12 : 170 mA(Max.)
  - KM68BV4002J-15 : 160 mA(Max.)
  - KM68BV4002J-20 : 150 mA(Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM68BV4002J: 36-SOJ-400

### GENERAL DESCRIPTION

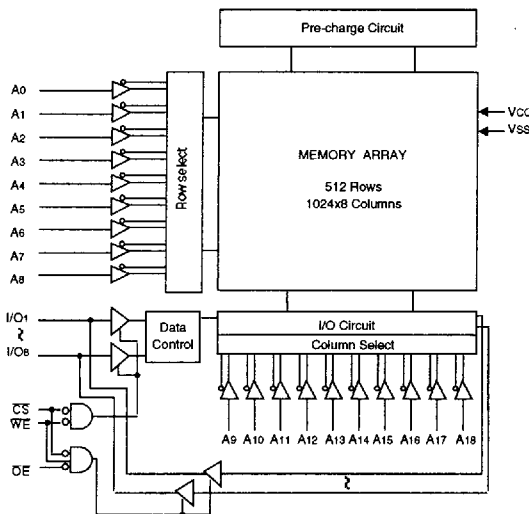
The KM68BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits.

The KM68BV4002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

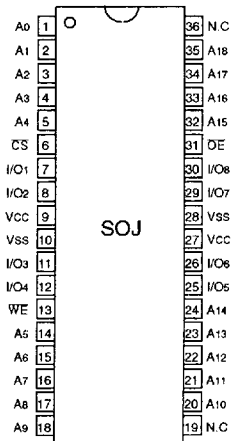
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM68BV4002 is packaged in a 400 mil 36-pin plastic SOJ.

### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATION(TOP VIEW)



Pin Name	Pin Function
A0-A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power (+3.3V)
Vss	Ground
N.C	No Connection

**ABSOLUTE MAXIMUM RATINGS \***

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN,OUT</sub>	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V <sub>CC</sub>	-0.5 to 4.6	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage Temperature	T <sub>stg</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	0 to 70	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS (T<sub>A</sub>=0 to 70 °C)**

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3**	V
Input Low Voltage	V <sub>IL</sub>	-0.5 *	-	0.8	V

\* V<sub>IL</sub>(Min.)= -2.0V ac (Pulse Width≤10 ns) for I<sub>S</sub>≤20 mA

\*\* V<sub>IH</sub>(Min.)= V<sub>CC</sub>+2.0V ac (Pulse Width≤10 ns) for I<sub>S</sub>≤20 mA

**DC AND OPERATING CHARACTERISTICS**

(T<sub>A</sub>=0 to 70 °C, V<sub>CC</sub>=3.3±0.3V, unless otherwise specified)

Item	Symbol	Test Condition	Min.	Max.	Unit	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-2	2	μA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>OUT</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-10	10	μA	
Average Operating Current	I <sub>CC</sub>	Min. Cycle, 100% Duty $\overline{CS}=V_{IL}$ , I <sub>OUT</sub> =0 mA $\overline{WE}=V_{IL}$ or $\overline{WE}=\overline{OE}=V_{IH}$	12 ns	-	170	mA
			15 ns	-	160	
			20 ns	-	150	
Standby Power Supply Current	I <sub>SB</sub>	$\overline{CS}=V_{IH}$ , Min. Cycle	-	60	mA	
	I <sub>SB1</sub>	$\overline{CS} \geq V_{CC}-0.2V$ , f=0 MHz V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	-	30	mA	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =8 mA	-	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-4 mA	2.4	-	V	

**CAPACITANCE \*** (f=1MHz, T<sub>A</sub>=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	7	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	8	pF

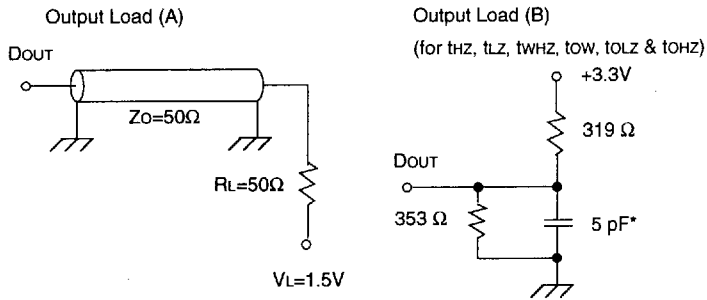
\* Note: Capacitance is sampled and not 100% tested.

## AC CHARACTERISTICS

## TEST CONDITIONS

(TA=0 to 70 °C, VCC=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3 ns
Input and Output Timing	1.5V
Reference Levels	
Output Load	See below



\* Including Scope and Jig Capacitance

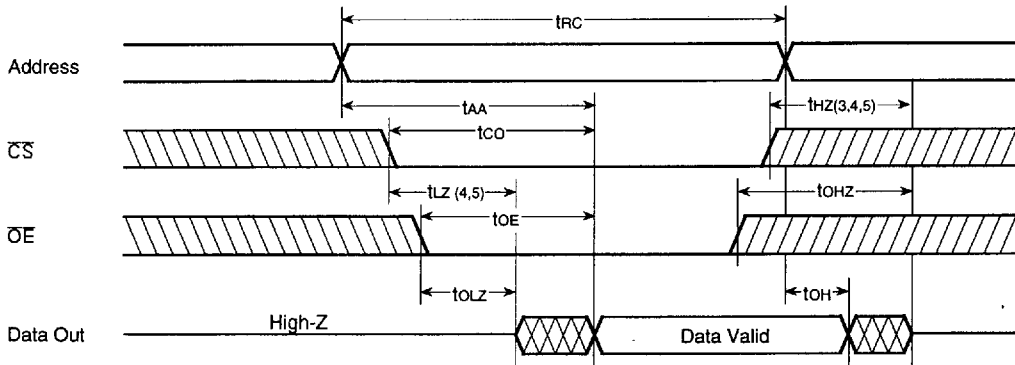
## READ CYCLE

Parameter	Symbol	KM68BV4002J-12		KM68BV4002J-15		KM68BV4002J-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t <sub>RC</sub>	12	-	15	-	20	-	ns
Address Access Time	t <sub>AA</sub>	-	12	-	15	-	20	ns
Chip Select to Output	t <sub>CO</sub>	-	12	-	15	-	20	ns
Output Enable to Valid Output	t <sub>OE</sub>	-	6	-	7	-	8	ns
Chip Select to Low-Z Output	t <sub>LZ</sub>	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	-	6	-	7	-	8	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	-	6	-	7	-	8	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	ns

## WRITE CYCLE

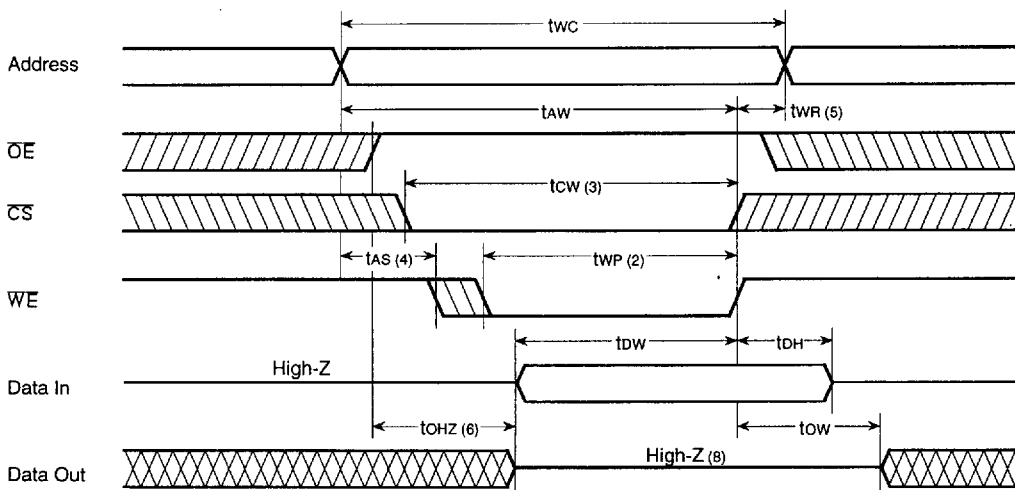
Parameter	Symbol	KM68BV4002J-12		KM68BV4002J-15		KM68BV4002J-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t <sub>wc</sub>	12	-	15	-	20	-	ns
Chip Select to End of Write	t <sub>cw</sub>	8	-	10	-	12	-	ns
Address Set-up Time	t <sub>as</sub>	0	-	0	-	0	-	ns
Address Valid to End of Write	t <sub>aw</sub>	8	-	10	-	12	-	ns
Write Pulse Width(OE High)	t <sub>wp</sub>	8	-	10	-	12	-	ns
Write Pulse Width(OE Low)	t <sub>wp</sub>	10	-	12	-	15	-	ns
Write Recovery Time	t <sub>wr</sub>	0	-	0	-	0	-	ns
Write to Output High-Z	t <sub>whz</sub>	-	6.5	-	7.5	-	8	ns
Data to Write Time Overlap	t <sub>dw</sub>	6	-	7	-	8	-	ns
Data Hold from Write Time	t <sub>dh</sub>	0	-	0	-	0	-	ns
End Write to Output Low-Z	t <sub>ow</sub>	3	-	3	-	3	-	ns

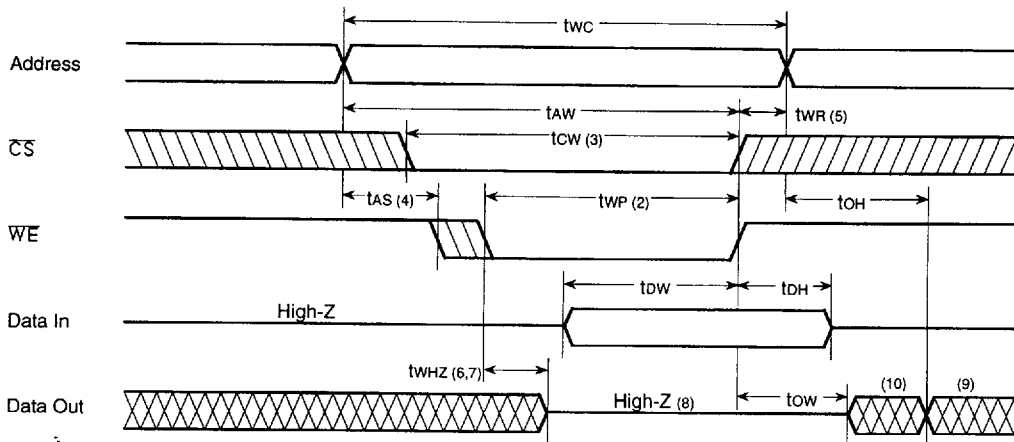
## TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE ( $\overline{WE}=V_{IH}$ )

## NOTES (READ CYCLE)

1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ}(\max.)$  is less than  $t_{LZ}(\min.)$  both for a given device and from device to device.
5. Transition is measured  $\pm 200$  mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CS} = V_{iL}$ .
7. Address valid prior to coincident with  $\overline{CS}$  transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}$  Clock)

TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{OE}$  Low Fixed)

## NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going low and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS}$  going high and  $\overline{WE}$  going high.  $tWP$  is measured from the beginning of write to the end of write.
3.  $tCW$  is measured from the later of  $\overline{CS}$  going low to end of write.
4.  $tAS$  is measured from the address valid to the beginning of write.
5.  $tWR$  is measured from the end of write to the address change.  $tWR$  applied in case a write ends as  $\overline{CS}$ , or  $\overline{WE}$  going high.
6. If  $\overline{OE}$ ,  $\overline{CS}$  and  $\overline{WE}$  are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If  $\overline{CS}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain high impedance state.
9.  $Dout$  is the read data of the new address.
10. When  $\overline{CS}$  is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

## FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	$I_{SB}$ , $I_{SB1}$
L	H	H	Output Disable	High-Z	$I_{CC}$
L	H	L	Read	$D_{OUT}$	$I_{CC}$
L	L	X	Write	$D_{IN}$	$I_{CC}$

Note : X means Don't Care.