

1M x 4Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 4bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5V or +3.3V), access time (-5, -6 or -7), power consumption(Normal or Low power), and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in 3.3V Low power version.

This 1Mx4 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory for main frames and mini computers, personal computer and high performance microprocessor systems.

FEATURES

• Part Identification

- KM44C1000D/D-L(5V, 1K Ref.)
- KM44V1000D/D-L(3.3V, 1K Ref.)

• Active Power Dissipation

Unit : mW

Speed	3.3V	5V
-5	-	470
-6	220	415
-7	200	360

• Refresh Cycles

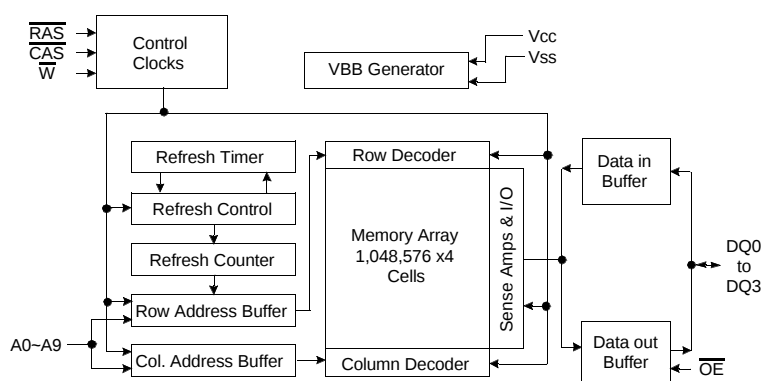
Part NO.	Refresh cycle	Refresh Period	
		Normal	L-ver
KM44C1000D	1K	16ms	128ms
KM44V1000D			

• Performance Range

Speed	t _{rac}	t _{cac}	t _{rc}	t _{pc}	Remark
-5	50ns	15ns	90ns	35ns	5V only
-6	60ns	15ns	110n	40ns	5V/3.3V
-7	70ns	20ns	130n	45ns	5V/3.3V

- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (3.3V, L-ver only)
- Fast parallel test mode capability
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early write or output enable controlled write
- JEDEC Standard pinout
- Available in 26(20)-pin SOJ 300mil and TSOP(II) 300mil packages
- Single +5V±10% power supply(5V product)
- Single +3.3V±0.3V power supply(3.3V product)

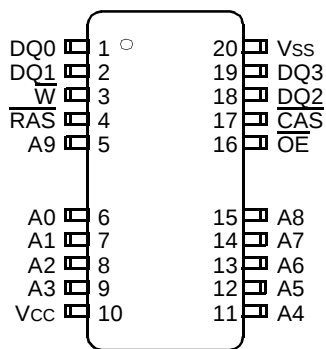
FUNCTIONAL BLOCK DIAGRAM



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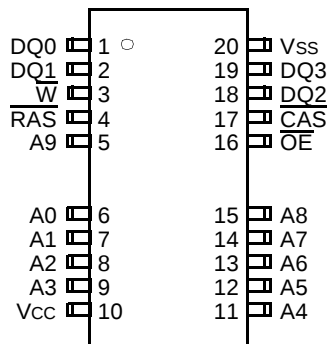
PIN CONFIGURATION (Top Views)

•KM44C/V1000DJ



(SOJ)

•KM44C/V1000DT



(TSOP-II)

Pin Name	Pin function
A0 - A9	Address Inputs
DQ0 - 3	Data In/out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5V)
	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	600	600	mW
Short Circuit Output Current	I _{os}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	2.4	-	V _{CC} +1.0 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	-0.1 ^{*2}	-	0.8	V

*1 : V_{CC} +1.3V/15ns(3.3V), V_{CC} +2.0V/20ns(5V), Pulse width is measured at V_{CC}

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.3V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	μA
	Output High Voltage Level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.5V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	μA
	Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommend operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM44V1000D	KM44C1000D	
I _{CC1}	Don't Care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
I _{CC2}	Don't Care	Don't Care	1	2	mA
I _{CC3}	Don't Care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
I _{CC4}	Don't Care	-5	-	65	mA
		-6	45	55	mA
		-7	40	45	mA
I _{CC5}	Normal L	Don't Care	0.5	1	mA
			100	200	uA
I _{CC6}	Don't Care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
I _{CC7}	L	Don't Care	200	300	uA
I _{CCS}	L	Don't Care	150	-	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @ $t_{RC}=\min$.)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3}* : $\overline{RAS}$ -only Refresh Current ($\overline{CAS}=V_{IH}$, $\overline{RAS}$, Address cycling @ $t_{RC}=\min$.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}=V_{IL}$, $\overline{CAS}$, Address cycling @ $t_{PC}=\min$.)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @ $t_{RC}=\min$)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})= $V_{CC}-0.2V$, Input low voltage(V_{IL})= $0.2V$, $\overline{CAS}=0.2V$,

DQ=Don't Care, $T_{RC}=125\mu s$ (L-ver.), $T_{RAS}=T_{RASmin}\sim 300ns$

I_{CCS} : Self refresh current

$\overline{RAS}=\overline{CAS}=V_{IL}$, $\overline{W}=\overline{OE}=A_0 \sim A_9=V_{CC}-0.2V$ or $0.2V$

DQ0 ~ DQ3= $V_{CC}-0.2V$, $0.2V$ or OPEN

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} I_{CC6} and I_{CC7}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC} .

KM44C1000D, KM44V1000D

CMOS DRAM

CAPACITANCE (TA=25°C, VCC=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A9]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ3]	CDQ	-	7	pF

AC CHARACTERISTICS (0°C≤T≤70°C, See note 1,2)

Test condition (5V device) : VCC=5.0V±10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.4/0.4V

Test condition (3.3V device) : VCC=3.3V±0.3V, VIH/VIL=2.2/0.7V, VOH/VOL=2.0/0.8V

Parameter	Symbol	-5*1		-6		7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	132		152		177		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		15		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	12	0	12	0	17	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		50		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	15		15		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		70		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	15	10K	15	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	35	20	45	20	50	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		15		ns	

Note) *1 : 5V only

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, See note 2)

Parameter	Symbol	-5 ^{*1}		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	t _{DS}	0		0		0		ns	9
Data hold time	t _{DH}	10		10		15		ns	9
Refresh period (Normal)	t _{REF}		16		16		16	ms	
Refresh period (L-ver)	t _{REF}		128		128		128	ms	
Write command set-up time	t _{WCS}	0		0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	37		37		47		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	72		82		97		ns	7
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	47		52		62		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t _{CPWD}	52		57		67		ns	7
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		10		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C-B-R}}$ counter test cycle)	t _{CPT}	20		20		25		ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		30		35		40	ns	3
Fast Page mode cycle time	t _{PC}	35		40		45		ns	
Fast Page read-modify-write cycle time	t _{PRWC}	77		82		97		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t _{RASP}	50	200K	60	200K	70	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	30		35		40		ns	
$\overline{\text{OE}}$ access time	t _{OEA}		15		15		20	ns	
$\overline{\text{OE}}$ to data delay	t _{OED}	12		12		17		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	t _{OEZ}	0	12	0	12	0	17	ns	6
$\overline{\text{OE}}$ command hold time	t _{OEH}	15		15		20		ns	
Write command set-up time (Test mode in)	t _{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t _{WTH}	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{C-B-R}}$ refresh)	t _{WRP}	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ($\overline{\text{C-B-R}}$ refresh)	t _{WRH}	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C-B-R}}$ self refresh)	t _{RASS}	100		100		100		us	14,15,16
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C-B-R}}$ self refresh)	t _{RPS}	90		110		130		ns	14,15,16
$\overline{\text{CAS}}$ Hold time ($\overline{\text{C-B-R}}$ self refresh)	t _{CHS}	-50		-50		-50		ns	14,15,16

Note) *1 : 5V only

TEST MODE CYCLE

(Note 11)

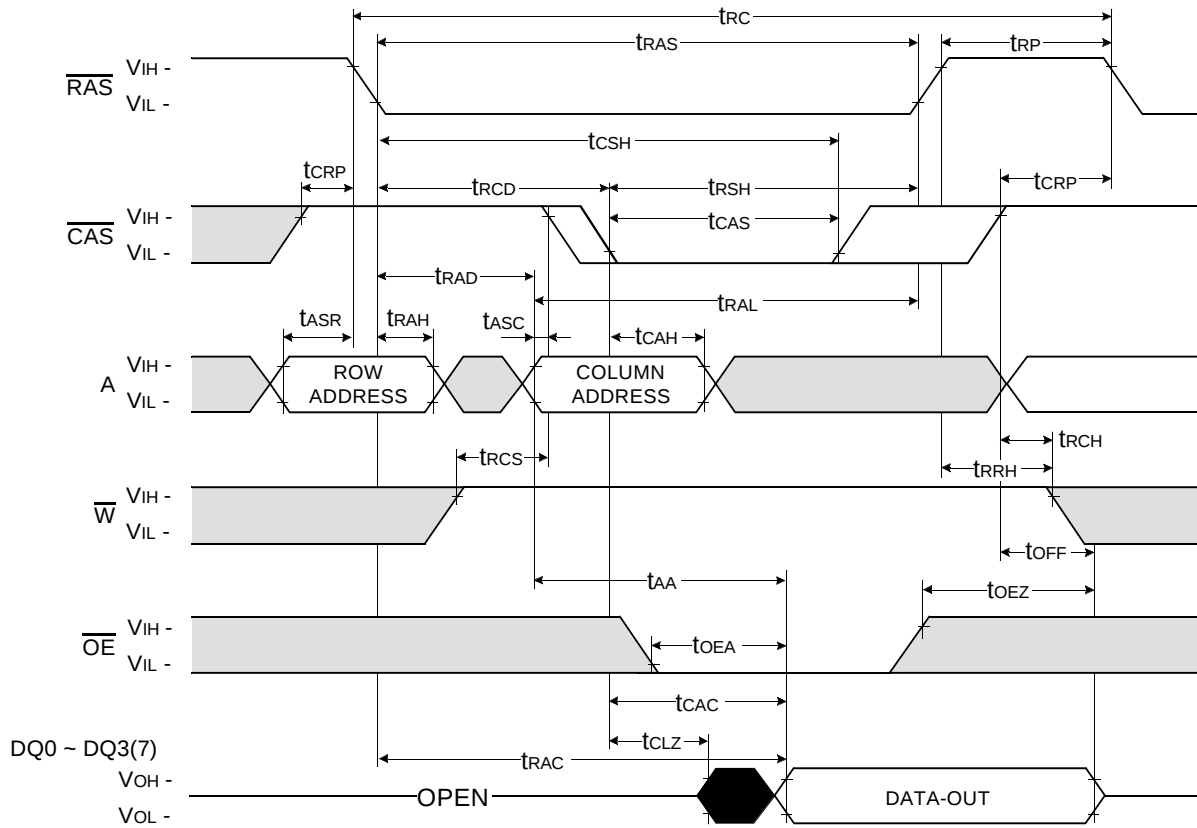
Parameter	Symbol	-5*1		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	95		115		135		ns	
Read-modify-write cycle time	t _{RWC}	138		160		190		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		55		65		75	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t _{CAC}		18		20		25	ns	3,4,5
Access time from column address	t _{AA}		30		35		40	ns	3,10
$\overline{\text{RAS}}$ pulse width	t _{RAS}	55	10K	65	10K	75	10K	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	18	10K	20	10K	25	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	18		20		25		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	55		65		75		ns	
Column Address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		40		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	41		45		55		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	78		90		105		ns	7
Column Address to $\overline{\text{W}}$ delay time	t _{AWD}	53		60		70		ns	7
Fast Page mode cycle time	t _{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle	t _{PRWC}	81		90		105		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t _{RASP}	55	200K	65	200K	75	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40		45	ns	3
$\overline{\text{OE}}$ access time	t _{OEa}		20		20		25	ns	
$\overline{\text{OE}}$ to data delay	t _{OEa}	18		20		25		ns	
$\overline{\text{OE}}$ command hold time	t _{OEh}	18		20		25		ns	

Note) *1 : 5V only

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$ then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. $t_{\text{OFF}}(\text{MAX})$ defines the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. If $t_{\text{RAS}} \geq 100\mu\text{s}$, then $\overline{\text{RAS}}$ precharge time must use t_{RPS} instead of t_{RP} .
15. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 1024(1K) cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6 μs interval, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh should be executed with in 15.6 μs immediately before and after self refresh in order to meet refresh specification.

READ CYCLE

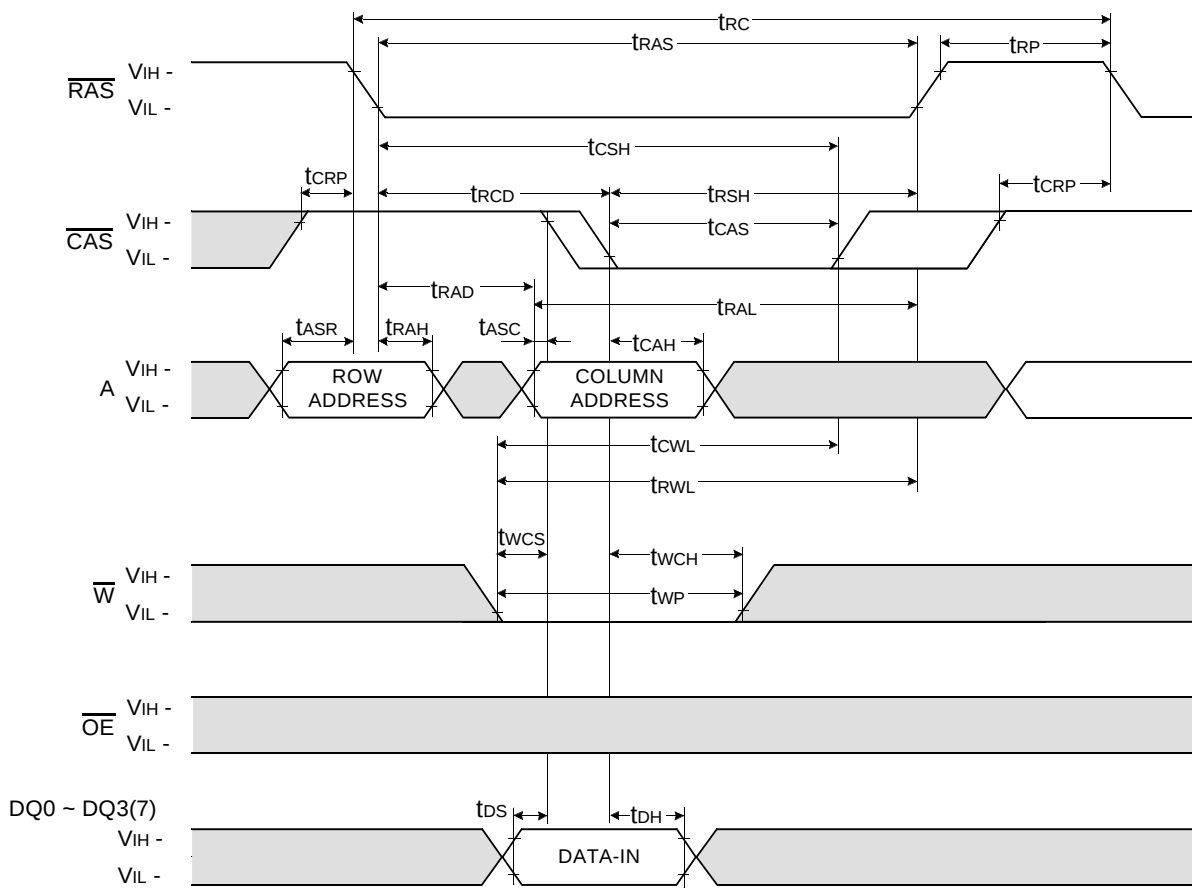


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WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

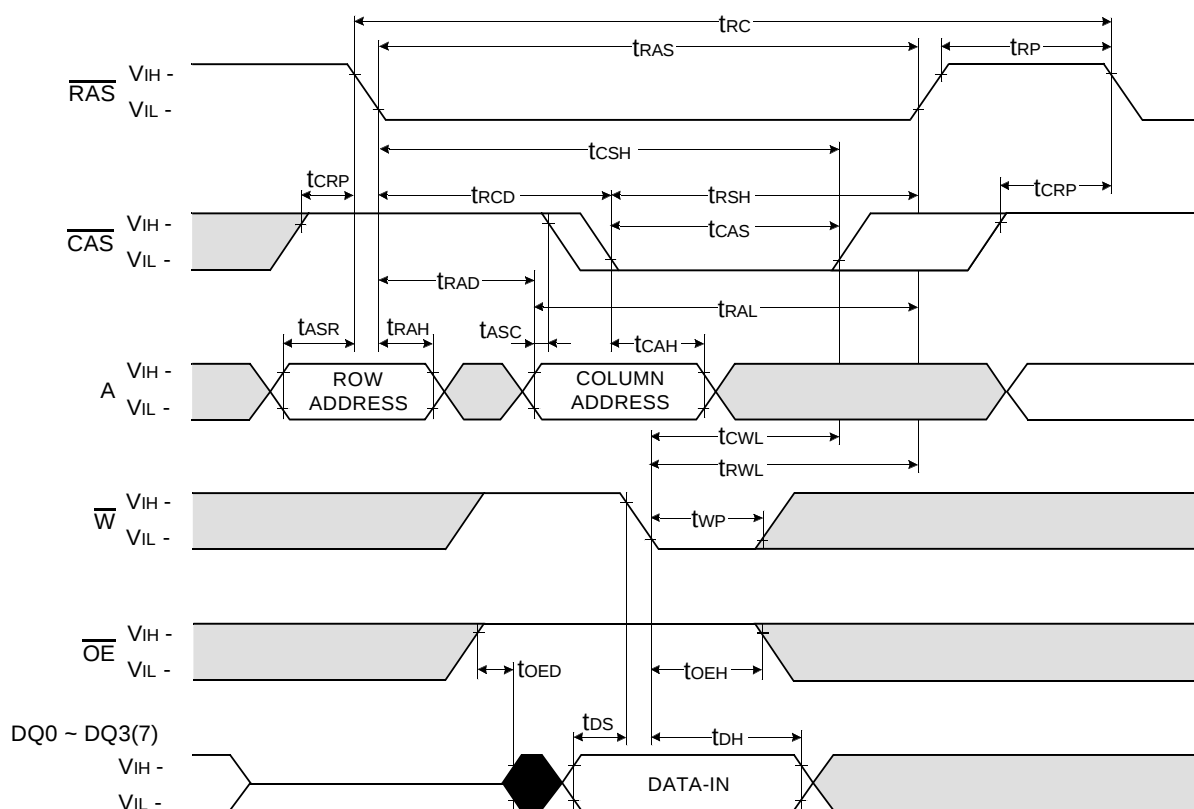


Don't care

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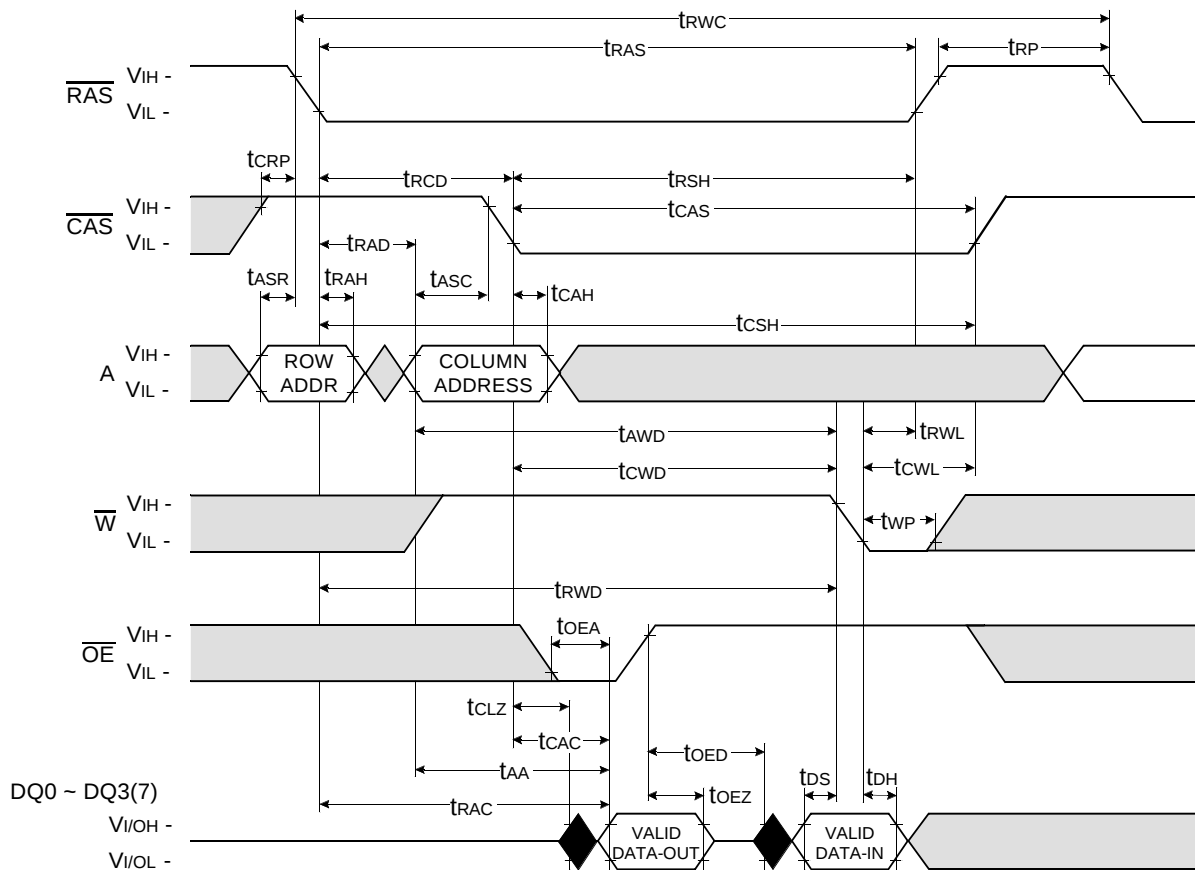
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN

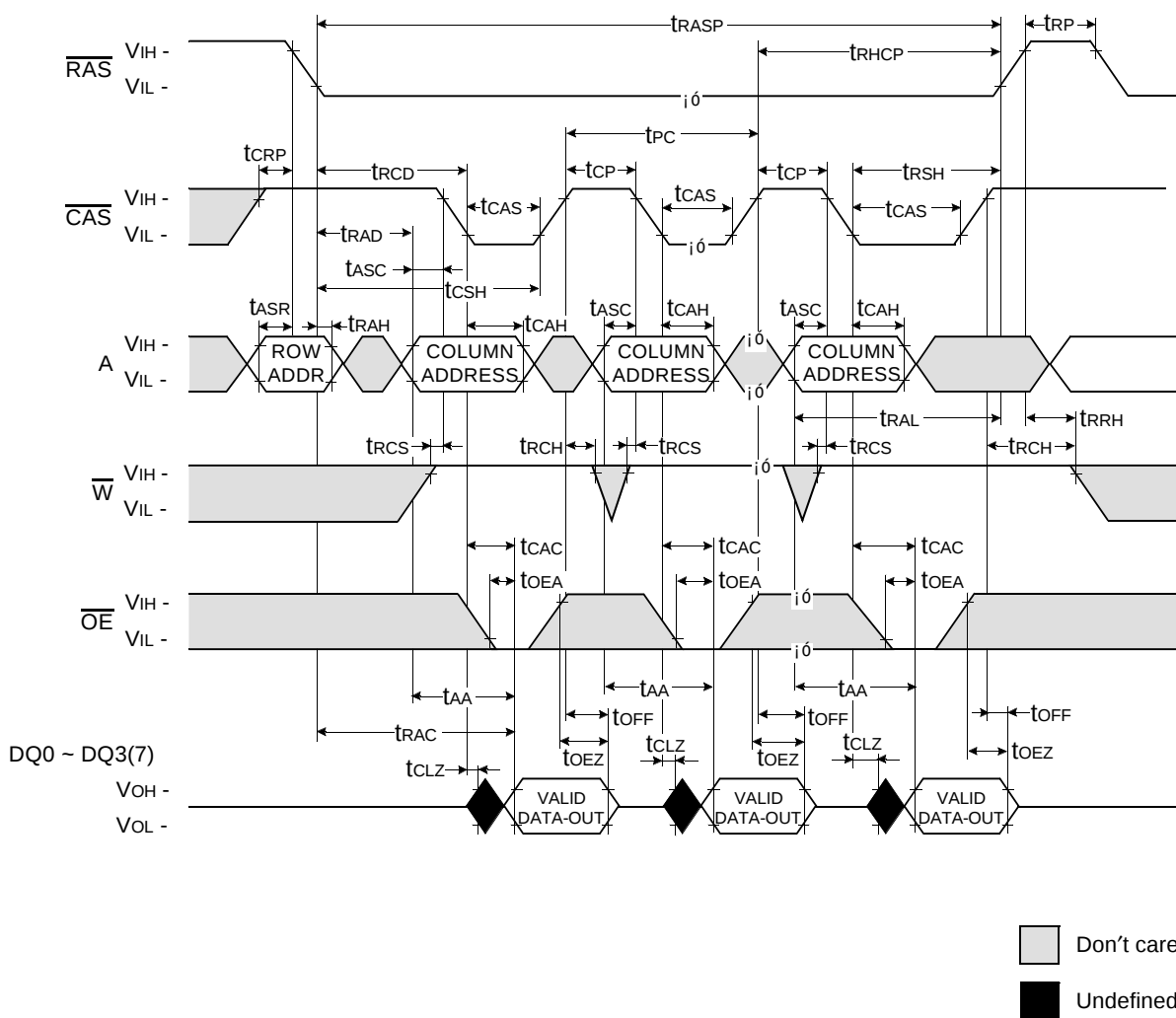


Don't care
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READ - MODIFY - WRITE CYCLE

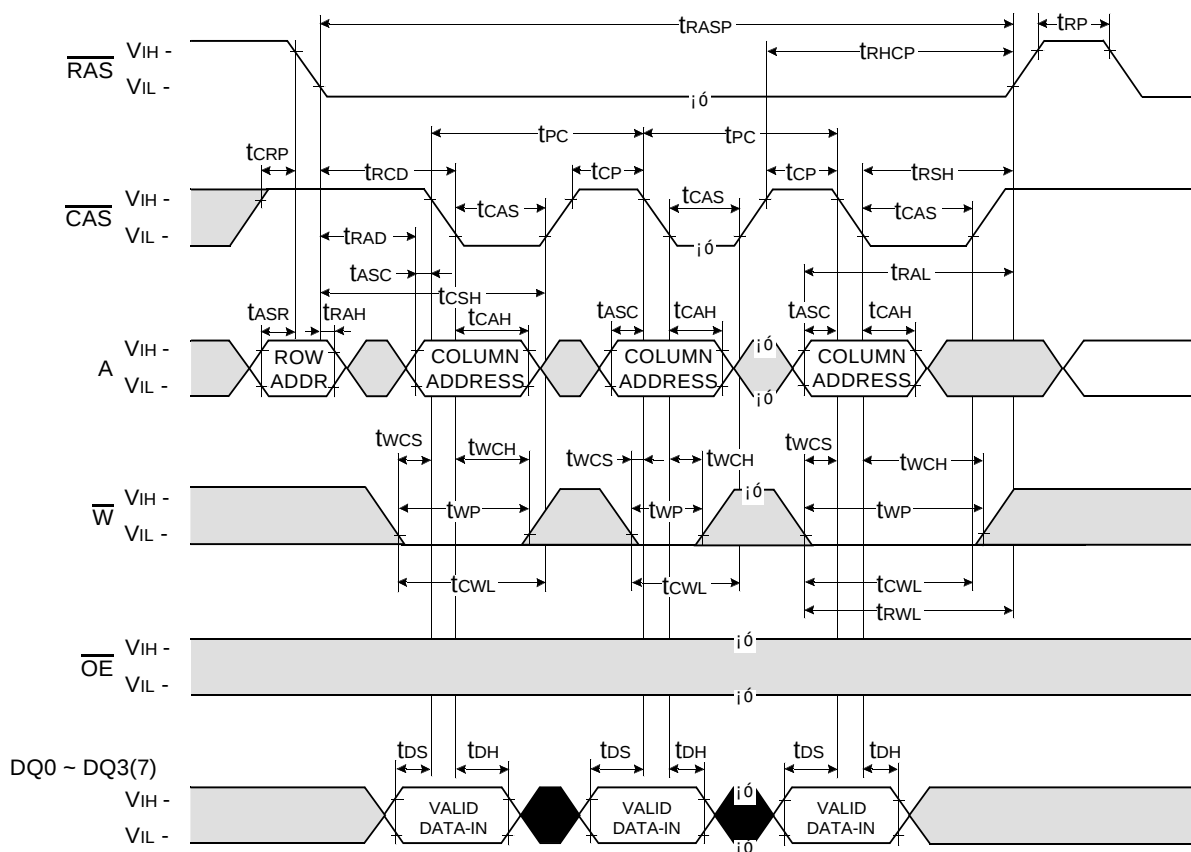


FAST PAGE READ CYCLE



FAST PAGE WRITE CYCLE (EARLY WRITE)

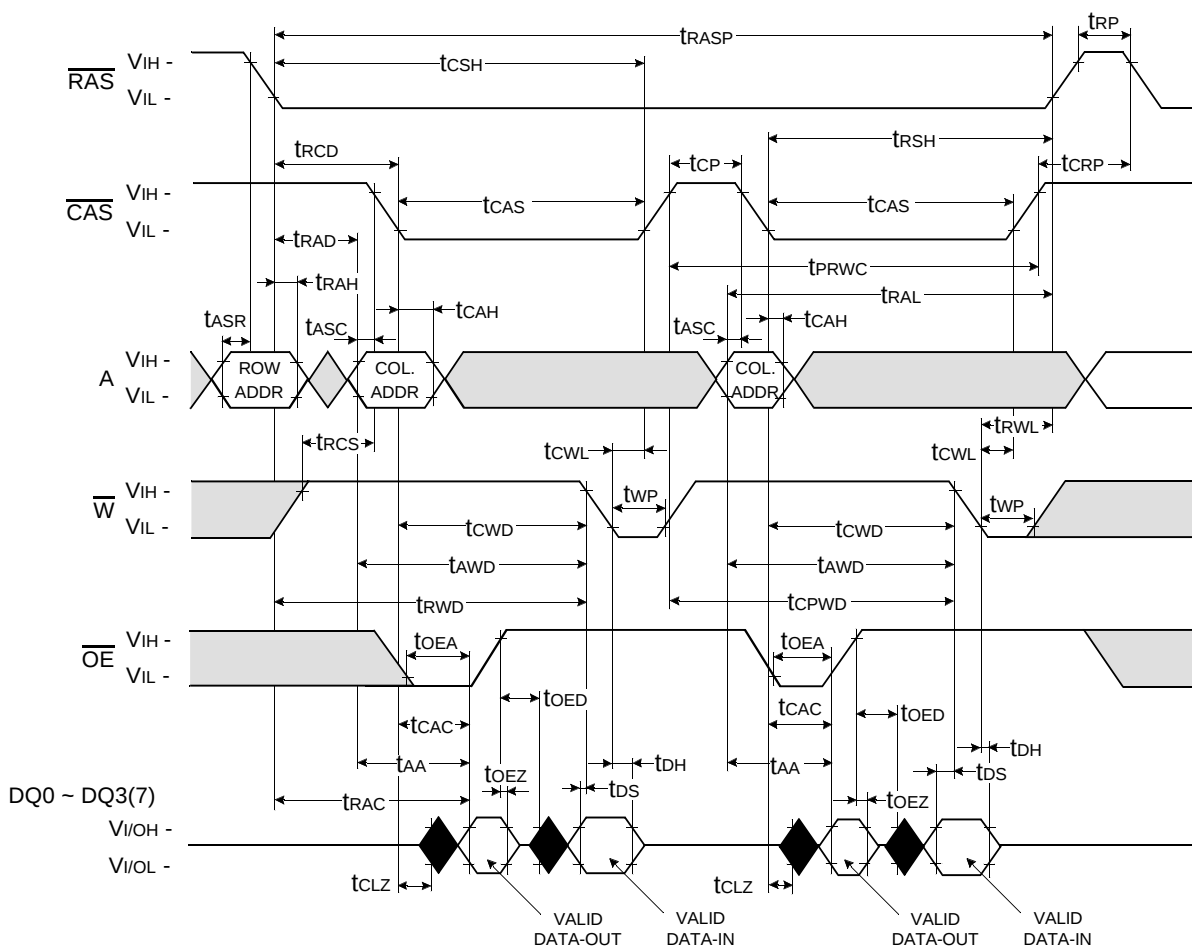
NOTE : DOUT = OPEN



Don't care

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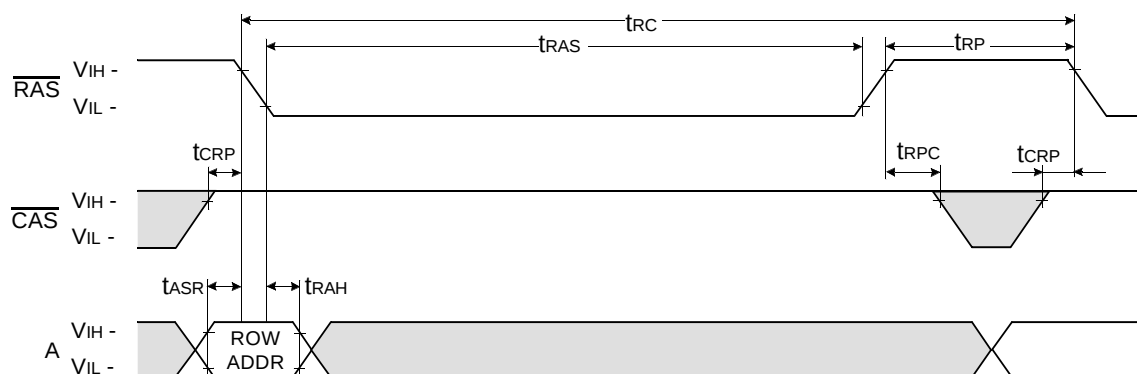
FAST PAGE READ - MODIFY - WRITE CYCLE



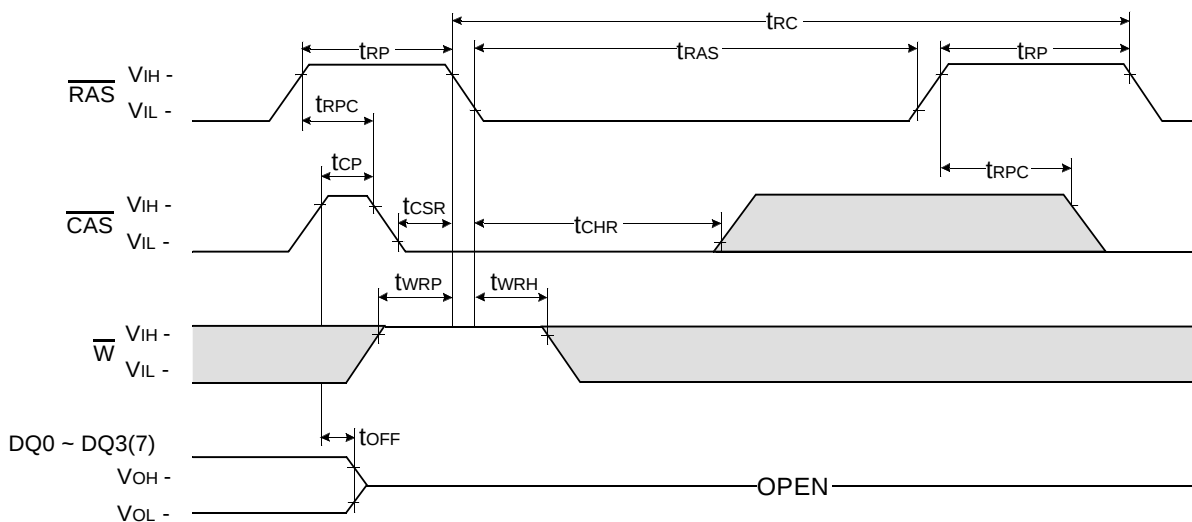
$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN


 $\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

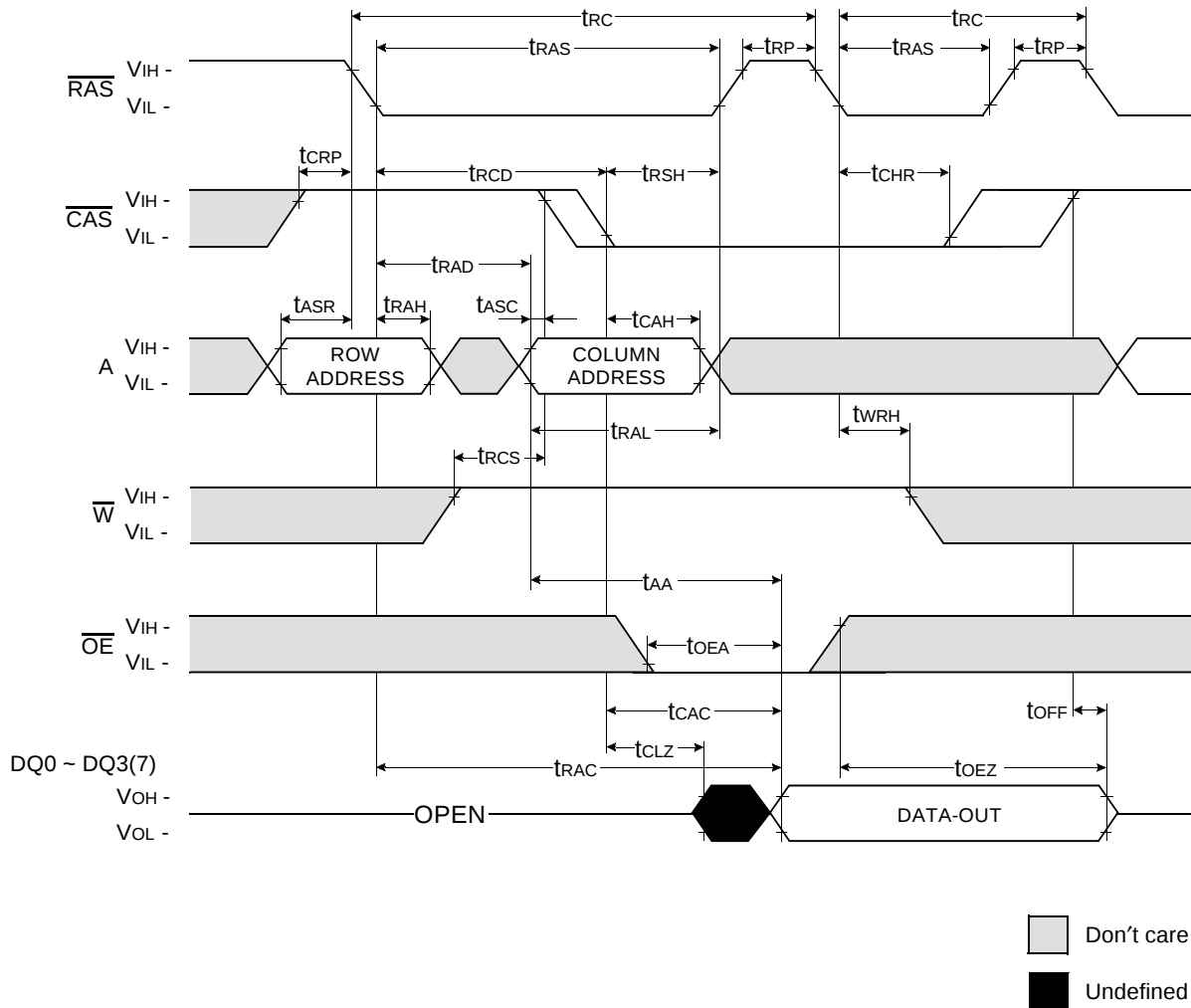
NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care

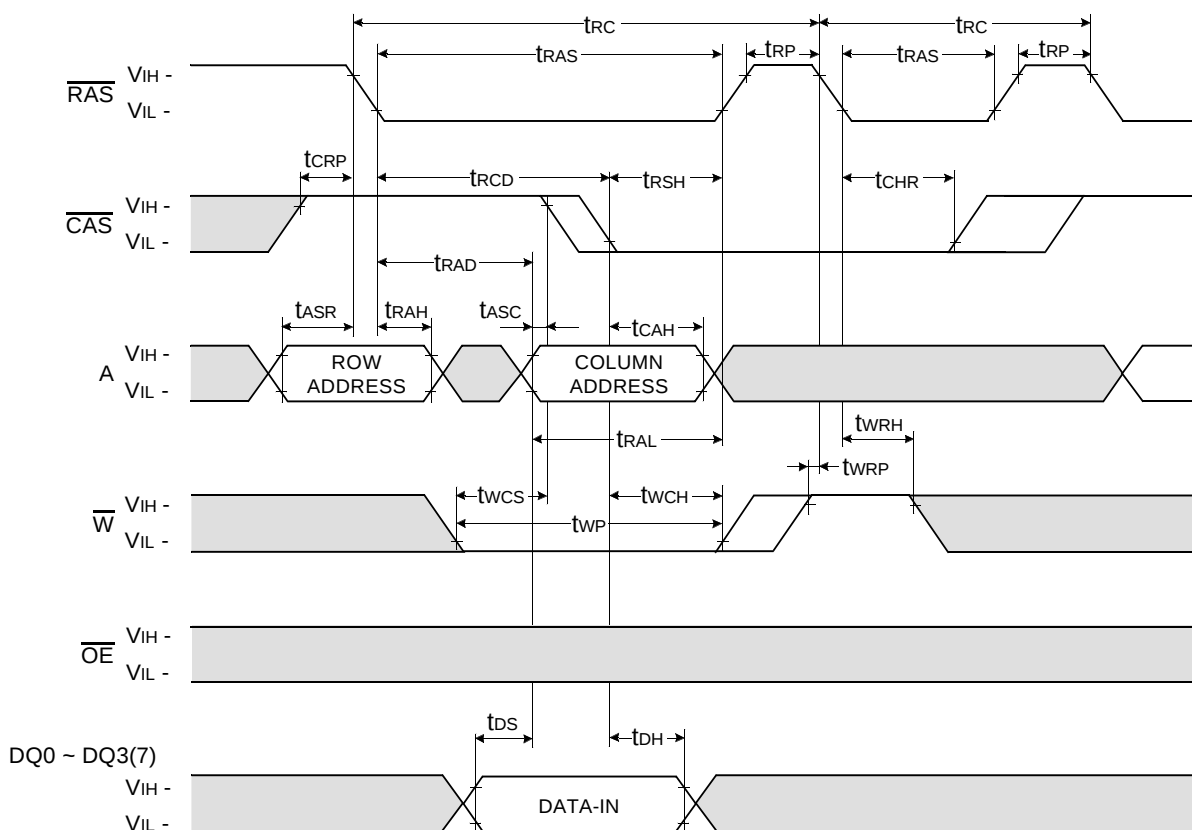
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HIDDEN REFRESH CYCLE (READ)



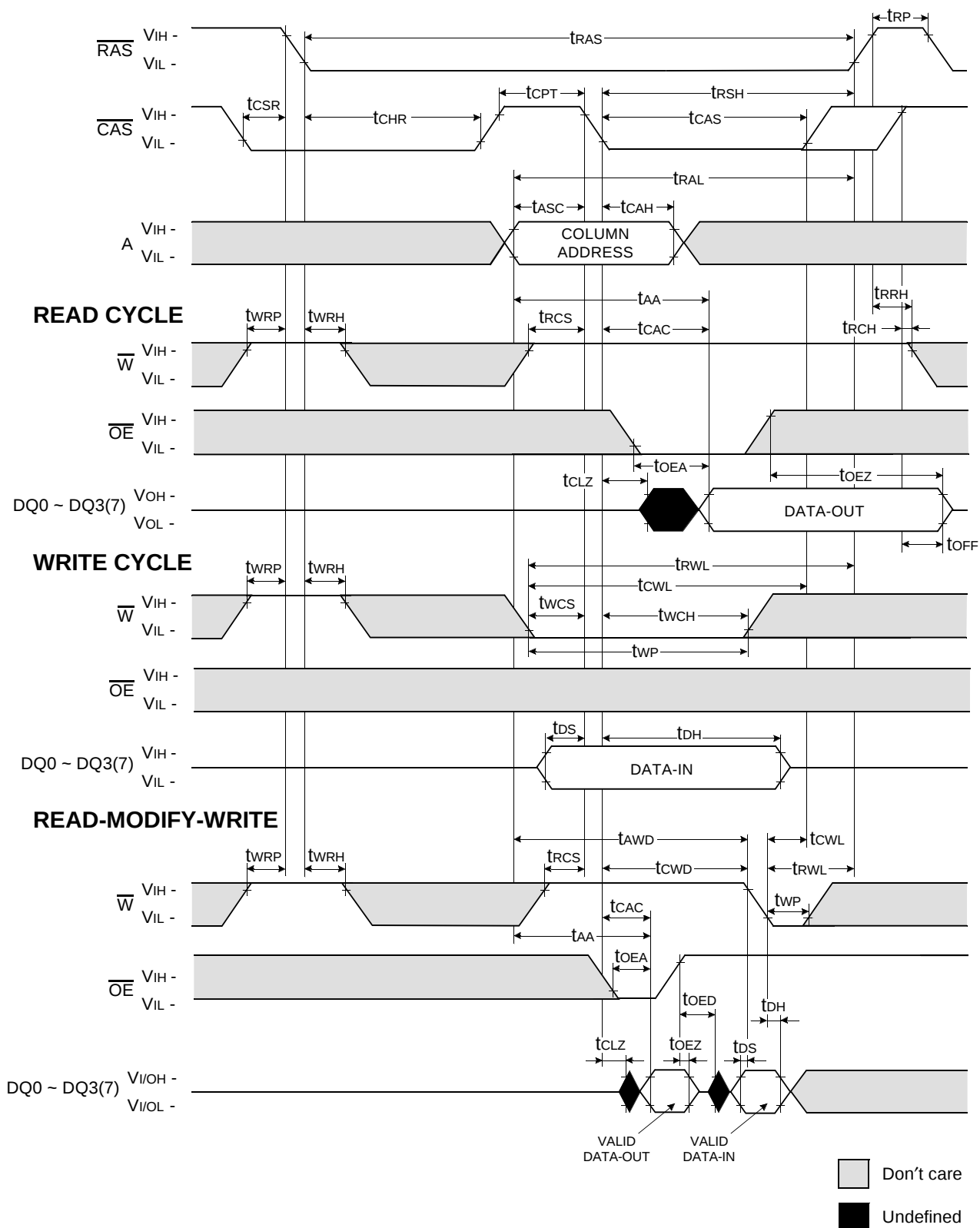
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



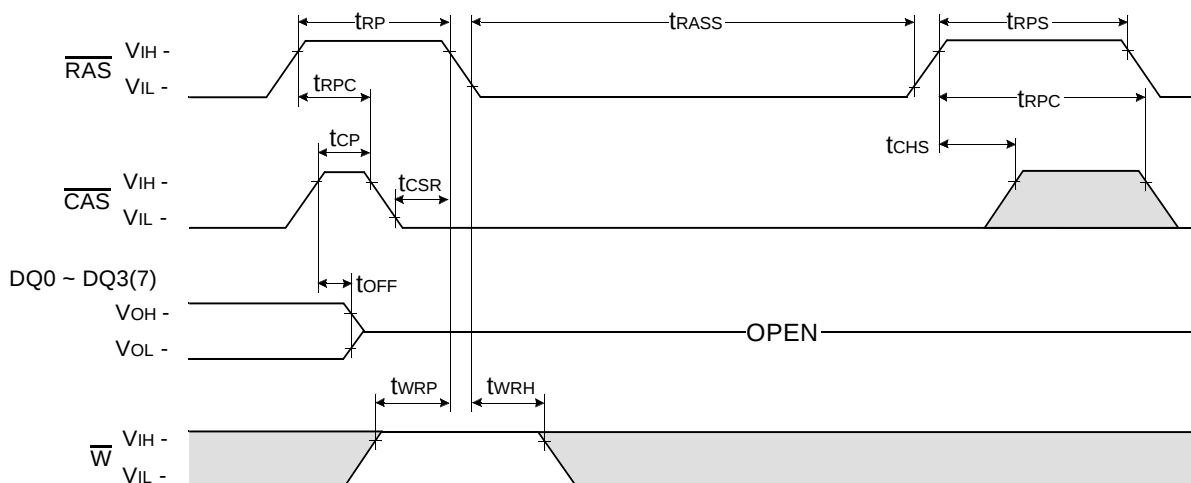
Don't care
Undefined

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



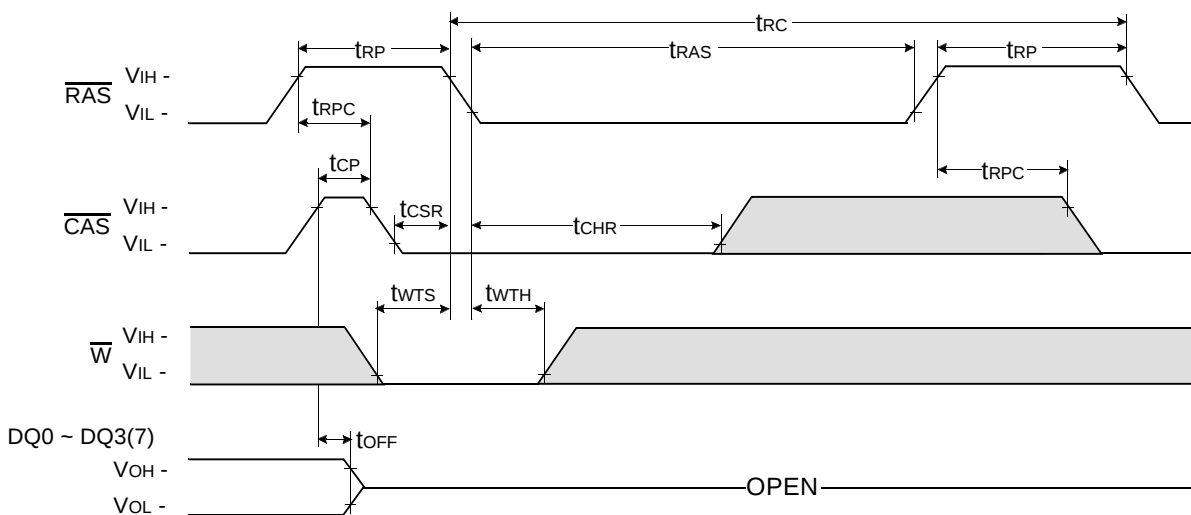
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care



Don't care
Undefined

PACKAGE DIMENSION

