ISSI®

32K x 8 HIGH-SPEED CMOS STATIC RAM

JULY 2002

FEATURES

- High-speed access time: 10, 12, 15, 20 ns
- Low active power: 400 mW (typical)
- Low standby power
  — 250 μW (typical) CMOS standby
  — 55 mW (typical) TTL standby
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
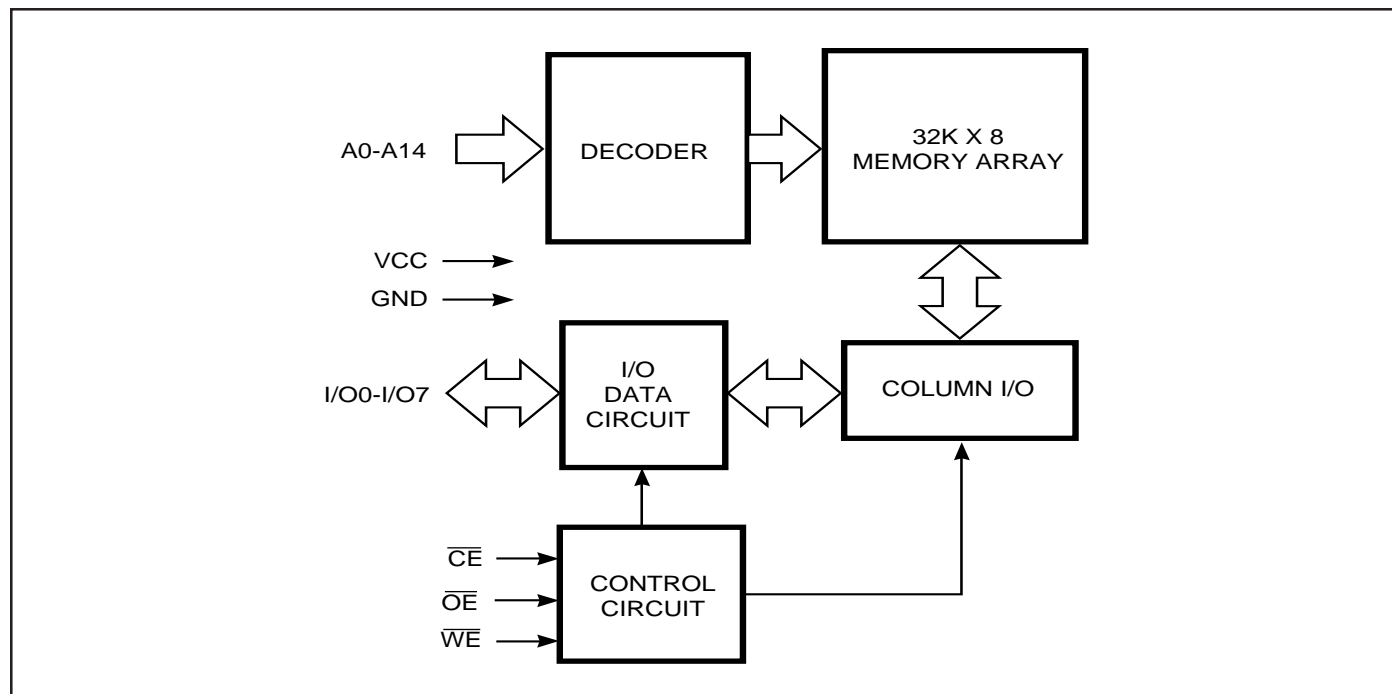- Single 5V power supply

DESCRIPTION

The *ISSI* IS61C256AH is a very high-speed, low power, 32,768 word by 8-bit static RAMs. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 10 ns maximum.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 μW (typical) with CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Enable ($\overline{CE}$) input and an active LOW Output Enable ($\overline{OE}$) input. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61C256AH is pin compatible with other 32K x 8 SRAMs and are available in 28-pin SOJ and TSOP (Type I) packages.
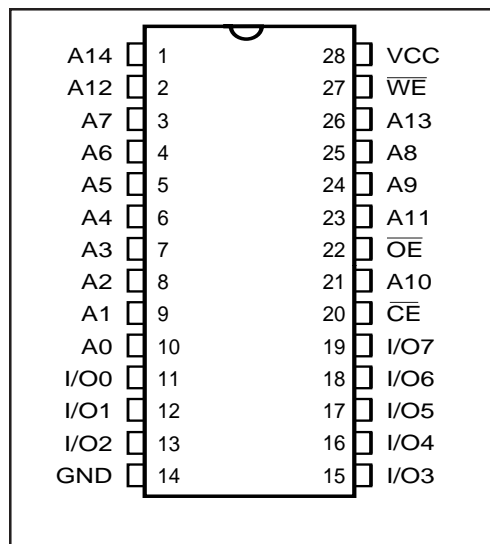
FUNCTIONAL BLOCK DIAGRAM

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SR020-1P
07/17/2002

PIN CONFIGURATION
28-Pin SOJ

```
        A14 ▯  1        28  ▯ VCC
        A12 ▯  2        27  ▯ WE̅
         A7 ▯  3        26  ▯ A13
         A6 ▯  4        25  ▯ A8
         A5 ▯  5        24  ▯ A9
         A4 ▯  6        23  ▯ A11
         A3 ▯  7        22  ▯ OE̅
         A2 ▯  8        21  ▯ A10
         A1 ▯  9        20  ▯ CE̅
         A0 ▯ 10        19  ▯ I/O7
       I/O0 ▯ 11        18  ▯ I/O6
       I/O1 ▯ 12        17  ▯ I/O5
       I/O2 ▯ 13        16  ▯ I/O4
        GND ▯ 14        15  ▯ I/O3
```

PIN CONFIGURATION
28-Pin TSOP

```
       OE̅ ▯ 22        21  ▯ A10
      A11 ▯ 23        20  ▯ CE̅
       A9 ▯ 24        19  ▯ I/O7
       A8 ▯ 25        18  ▯ I/O6
      A13 ▯ 26        17  ▯ I/O5
       WE̅ ▯ 27        16  ▯ I/O4
      VCC ▯ 28        15  ▯ I/O3
      A14 ▯  1        14  ▯ GND
      A12 ▯  2        13  ▯ I/O2
       A7 ▯  3        12  ▯ I/O1
       A6 ▯  4        11  ▯ I/O0
       A5 ▯  5        10  ▯ A0
       A4 ▯  6         9  ▯ A1
       A3 ▯  7         8  ▯ A2
```
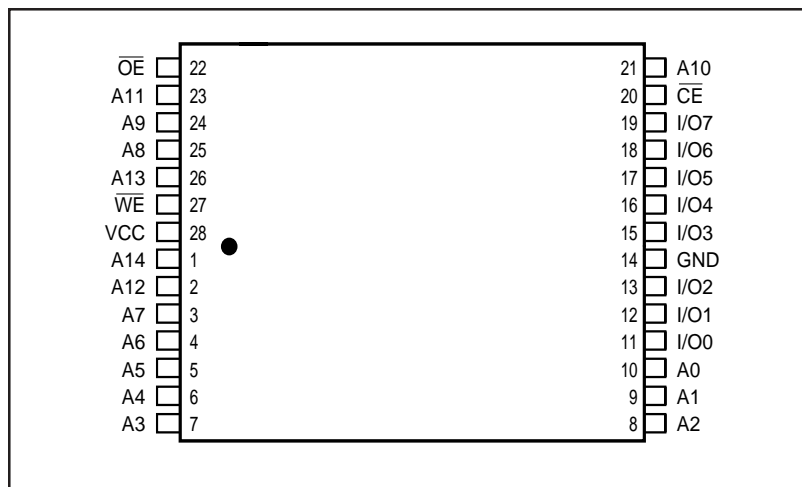
PIN DESCRIPTIONS

A0–A14	Address Inputs
CE̅	Chip Enable Input
OE̅	Output Enable Input
WE̅	Write Enable Input
I/O0–I/O7	Bidirectional Ports
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	WE̅	CE̅	OE̅	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	−55 to +125	℃
T_{STG}	Storage Temperature	−65 to +150	℃
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed	Vcc
Commercial	0°C to +70°C	-10, -12	5V ± 5%
		-15, -20	5V ± 10%
Industrial	−40°C to +85°C	-12	5V ± 5%
		-15, -20	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	V
I_{LI}	Input Leakage	GND - V_{IN} - V_{CC}	Com.	−5	5	µA
			Ind.	−10	10	
I_{LO}	Output Leakage	GND - V_{OUT} - V_{CC}, Outputs Disabled	Com.	−5	5	µA
			Ind.	−10	10	

Note:
1. V_{IL} = −3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	165	—	155	—	145	—	135	mA
			Ind.	—	—	—	165	—	155	—	145	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ • V_{IH}, f = 0	Com.	—	25	—	25	—	25	—	25	mA
			Ind.	—	—	—	30	—	30	—	30	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ • V_{CC} – 0.2V, V_{IN} • V_{CC} – 0.2V, or V_{IN} - 0.2V, f = 0	Com.	—	2	—	2	—	2	—	2	mA
			Ind.	—	—	—	10	—	10	—	10	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	10	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A = 25°C$, f = 1 MHz, Vcc = 5.0V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-10 ns Min.	-10 ns Max	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20	ns
t_{OHA}	Output Hold Time	2	—	2	—	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	—	15	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	5	—	7	—	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	5	—	6	—	7	—	9	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	2	—	3	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	—	5	—	7	—	8	—	9	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	10	—	12	—	15	—	18	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

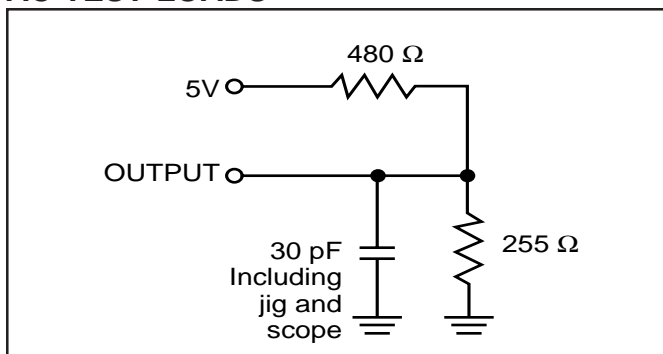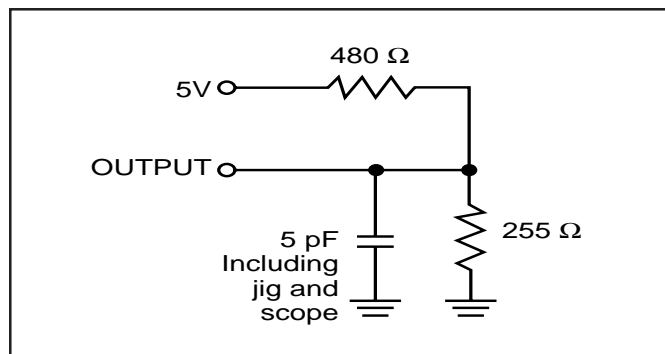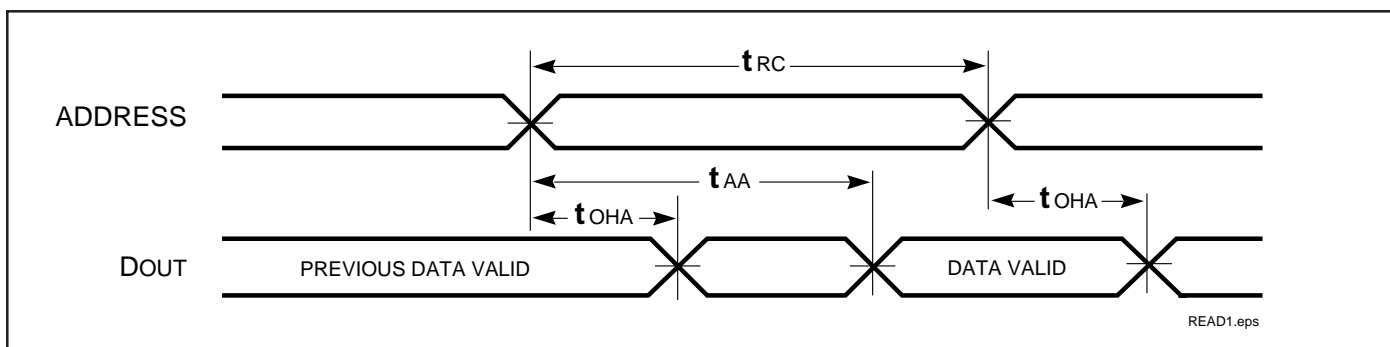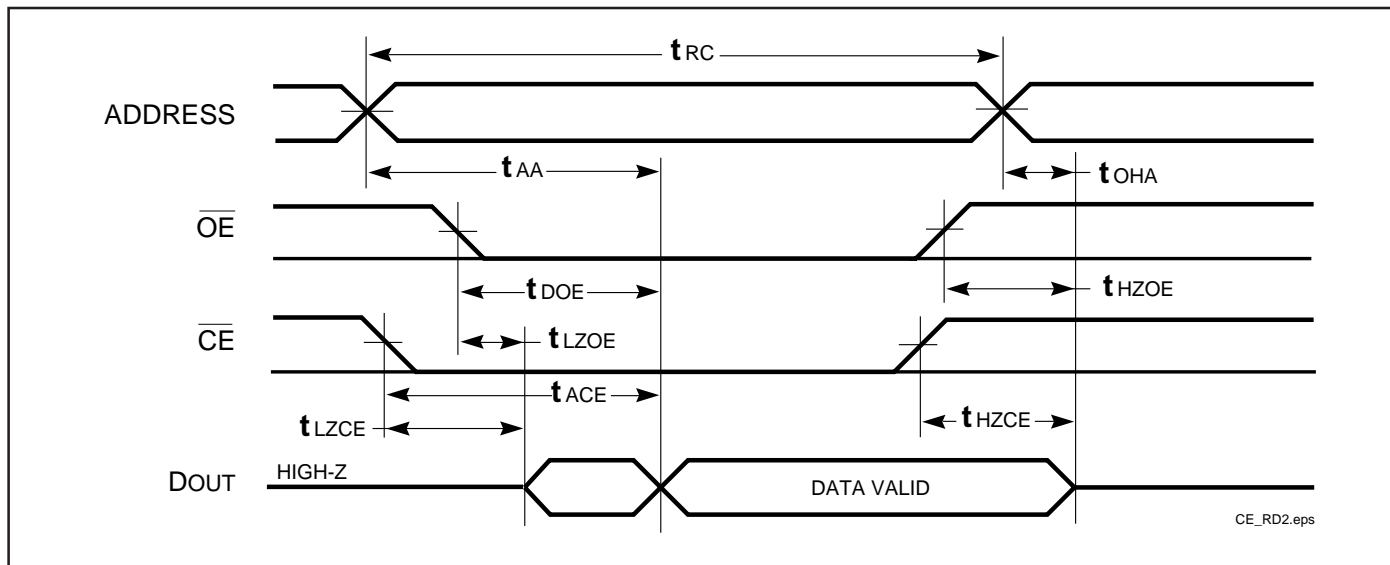| Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

480 Ω
5V
OUTPUT
30 pF
Including
jig and
scope
255 Ω

Figure 1

480 Ω
5V
OUTPUT
5 pF
Including
jig and
scope
255 Ω

Figure 2

AC WAVEFORMS
READ CYCLE NO. 1[1,2]

t_{RC}

ADDRESS

t_{AA}

t_{OHA}

t_{OHA}

DOUT   PREVIOUS DATA VALID   DATA VALID

READ1.eps

READ CYCLE NO. 2[1,3]

t_{RC}

ADDRESS

t_{AA}

t_{OHA}

$\overline{OE}$

t_{DOE}

t_{HZOE}

$\overline{CE}$

t_{LZOE}

t_{ACE}

t_{HZCE}

t_{LZCE}

DOUT   HIGH-Z   DATA VALID

CE_RD2.eps

Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V$_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-10 ns Min.	-10 ns Max	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{SCE}	$\overline{CE}$ to Write End	9	—	10	—	10	—	13	—	ns
t_{AW}	Address Setup Time to Write End	9	—	10	—	12	—	15	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ LOW)	8	—	8	—	10	—	13	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ HIGH)	6.5	—	7	—	8	—	10	—	ns
t_{SD}	Data Setup to Write End	7	—	7	—	9	—	10	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	7	—	8	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]

CE_WR1.eps
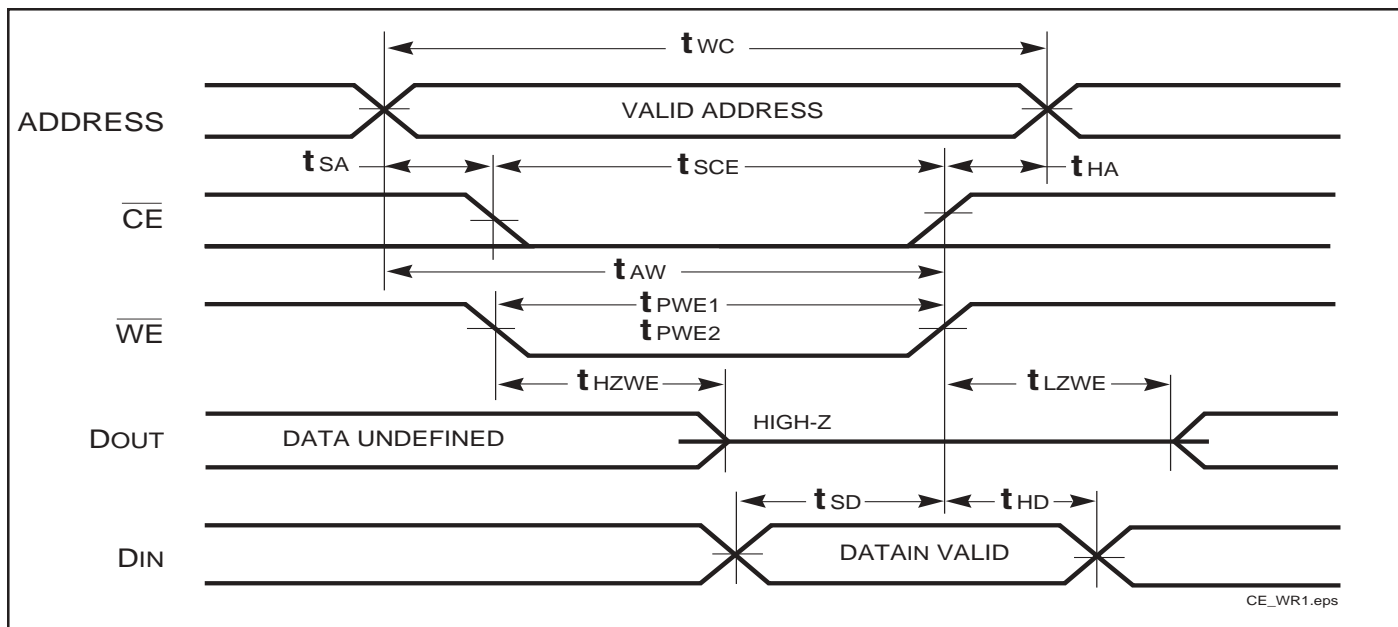
WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]

CE_WR2.eps
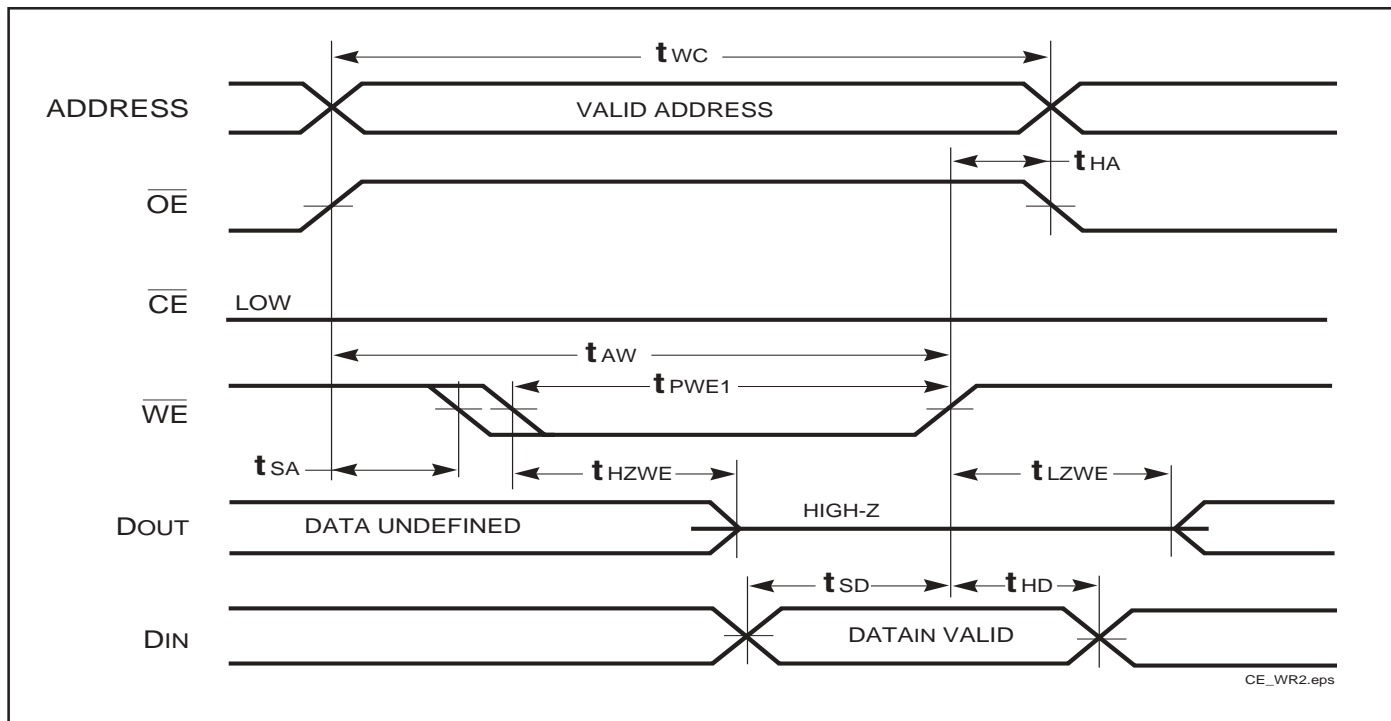
WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]

CE_WR3.eps
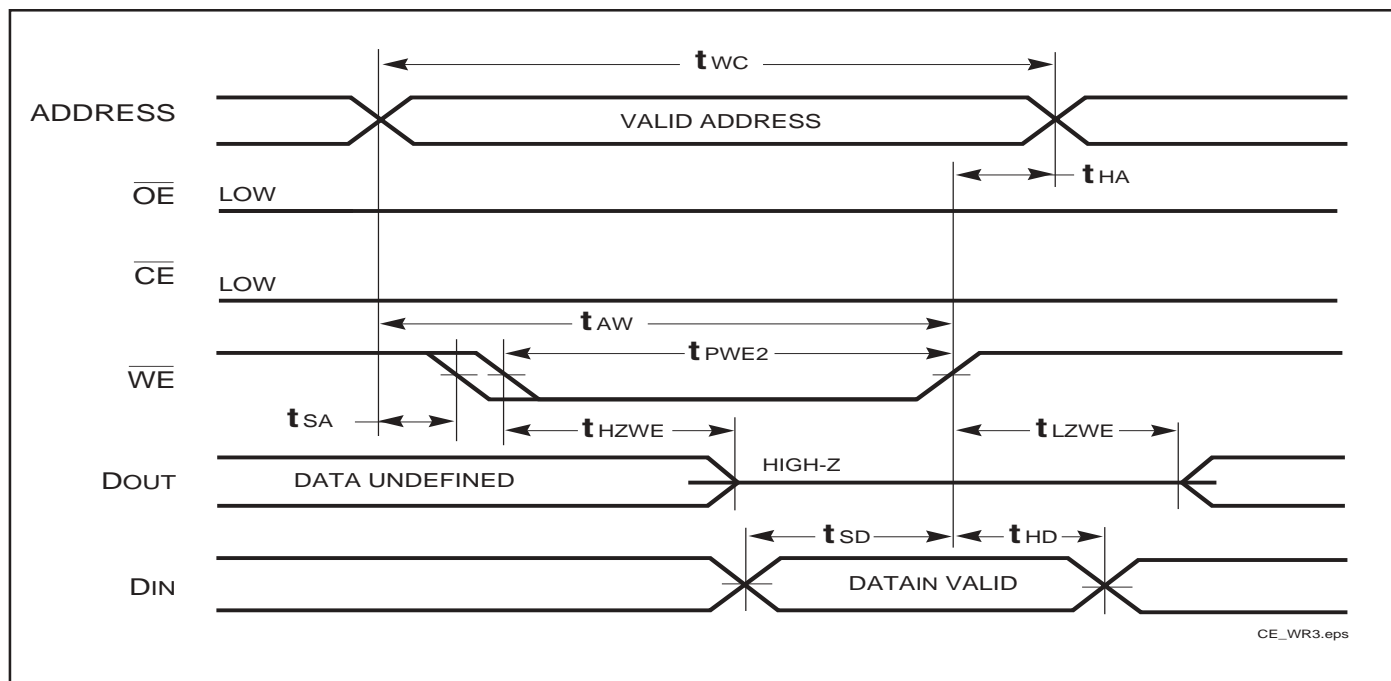
Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \cdot V_{IH}$.

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ORDERING INFORMATION: IS61C256AH
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part Number	Package
10	IS61C256AH-10J	300-mil Plastic SOJ
	IS61C256AH-10T	TSOP (Type 1)
12	IS61C256AH-12J	300-mil Plastic SOJ
	IS61C256AH-12T	TSOP (Type 1)
15	IS61C256AH-15J	300-mil Plastic SOJ
	IS61C256AH-15T	TSOP (Type 1)
20	IS61C256AH-20J	300-mil Plastic SOJ
	IS61C256AH-20T	TSOP (Type 1)

ORDERING INFORMATION: IS61C256AH
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part Number	Package
12	IS61C256AH-12JI	300-mil Plastic SOJ
	IS61C256AH-12TI	TSOP (Type 1)
15	IS61C256AH-15JI	300-mil Plastic SOJ
	IS61C256AH-15TI	TSOP (Type 1)
20	IS61C256AH-20JI	300-mil Plastic SOJ
	IS61C256AH-20TI	TSOP (Type 1)