



Power MOSFET

| PRODUCT SUMMARY | |
|--------------------------|--------------------------------|
| V _{DS} (V) | -200 |
| R _{DS(on)} (Ω) | V _{GS} = -10 V 0.50 |
| Q _g max. (nC) | 44 |
| Q _{gs} (nC) | 7.1 |
| Q _{gd} (nC) | 27 |
| Configuration | Single |

FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN FREE
Available

Note

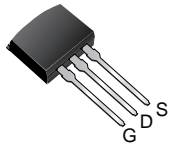
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

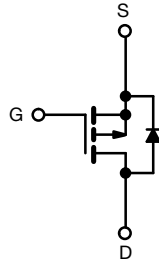
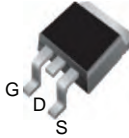
Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRF9640L, SiHF9640L) is available for low-profile applications.

I²PAK (TO-262)



D²PAK (TO-263)



P-Channel MOSFET

| ORDERING INFORMATION | | | | |
|---------------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| Package | D ² PAK (TO-263) | D ² PAK (TO-263) | D ² PAK (TO-263) | I ² PAK (TO-262) |
| Lead (Pb)-free and Halogen-free | SiHF9640S-GE3 | - | - | SiHF9640L-GE3 |
| Lead (Pb)-free | IRF9640SPbF | IRF9640STRLPbF ^a | IRF9640STRRPbF ^a | IRF9640LPbF |
| | SiHF9640S-E3 | SiHF9640STL-E3 ^a | SiHF9640STR-E3 ^a | SiHF9640L-E3 |

Note

a. See device orientation.

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | |
|---|-----------------------------------|-------------------------|-------------|------|
| PARAMETER | SYMBOL | | LIMIT | UNIT |
| Drain-Source Voltage | V _{DS} | | -200 | V |
| Gate-Source Voltage | V _{GS} | | ± 20 | |
| Continuous Drain Current | V _{GS} at -10 V | T _C = 25 °C | -11 | A |
| | | T _C = 100 °C | -6.8 | |
| Pulsed Drain Current ^a | I _{DM} | | -44 | W/°C |
| Linear Derating Factor | | | 1.0 | |
| Linear Derating Factor (PCB mount) ^e | | | 0.025 | |
| Single Pulse Avalanche Energy ^b | E _{AS} | | 700 | mJ |
| Avalanche Current ^a | I _{AR} | | -11 | A |
| Repetitive Avalanche Energy ^a | E _{AR} | | 13 | mJ |
| Maximum Power Dissipation | T _C = 25 °C | | 125 | W |
| | T _A = 25 °C | | 3.0 | |
| Peak Diode Recovery dV/dt ^c | dV/dt | | -5.0 | V/ns |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | | -55 to +150 | °C |
| Soldering Recommendations (Peak temperature) ^d | for 10 s | | 300 | |

Notes

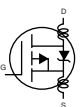

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = -50 V, starting T_J = 25 °C, L = 8.7 mH, R_g = 25 Ω, I_{AS} = -11 A (see fig. 12).
- I_{SD} ≤ -11 A, dI/dt ≤ 150 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).



| THERMAL RESISTANCE RATINGS | | | | |
|--|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W |
| Maximum Junction-to-Ambient (PCB mount) ^a | R_{thJA} | - | 40 | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 1.0 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | |
|---|---------------------|---|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$ | -200 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = -1\text{ mA}$ | - | -0.20 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$ | -2.0 | - | -4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$ | - | - | -100 | μA |
| | | $V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | - | - | -500 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = -10\text{ V}, I_D = 6.6\text{ A}^b$ | - | - | 0.50 | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = -50\text{ V}, I_D = -6.6\text{ A}^b$ | 4.1 | - | - | S |
| Dynamic | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5 | - | 1200 | - | pF |
| Output Capacitance | C_{oss} | | - | 370 | - | |
| Reverse Transfer Capacitance | C_{rss} | | - | 81 | - | |
| Total Gate Charge | Q_g | $V_{GS} = -10\text{ V}, I_D = -11\text{ A}, V_{DS} = -160\text{ V}$, see fig. 6 and 13 ^b | - | - | 44 | nC |
| Gate-Source Charge | Q_{gs} | | - | - | 7.1 | |
| Gate-Drain Charge | Q_{gd} | | - | - | 27 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -100\text{ V}, I_D = -11\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 8.6\text{ }\Omega$, see fig. 10 ^b | - | 14 | - | ns |
| Rise Time | t_r | | - | 43 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 39 | - | |
| Fall Time | t_f | | - | 38 | - | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact  | - | 4.5 | - | nH |
| Internal Source Inductance | L_S | | - | 7.5 | - | |
| Gate Input Resistance | R_g | $f = 1\text{ MHz}$, open drain | 0.3 | - | 1.7 | Ω |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p-n junction diode  | - | - | -11 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | - | - | -44 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = -11\text{ A}, V_{GS} = 0\text{ V}^b$ | - | - | -5.0 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = -11\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$ | - | 250 | 300 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | - | 2.9 | 3.6 | |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

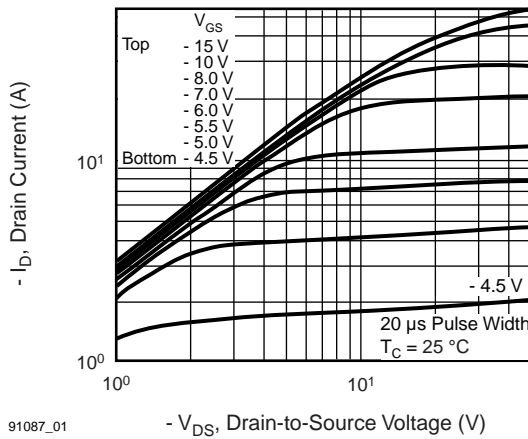


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

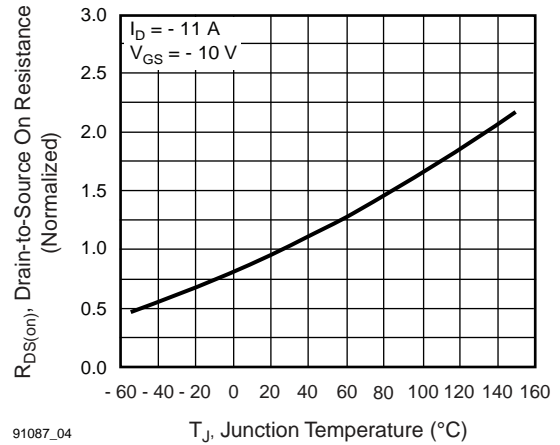


Fig. 4 - Normalized On-Resistance vs. Temperature

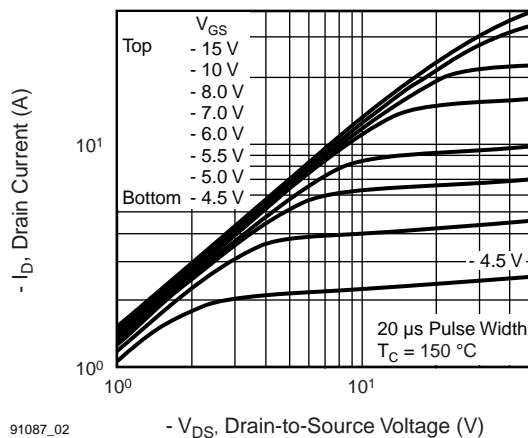


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

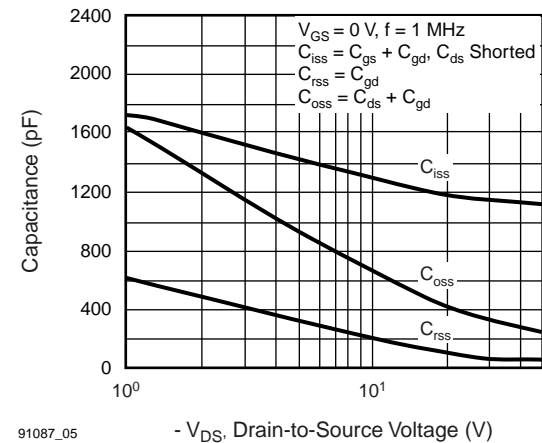


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

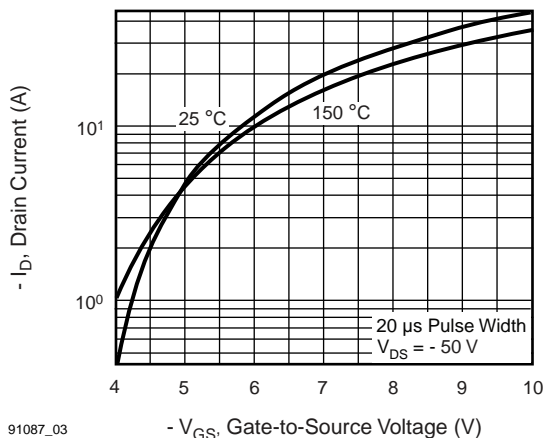


Fig. 3 - Typical Transfer Characteristics

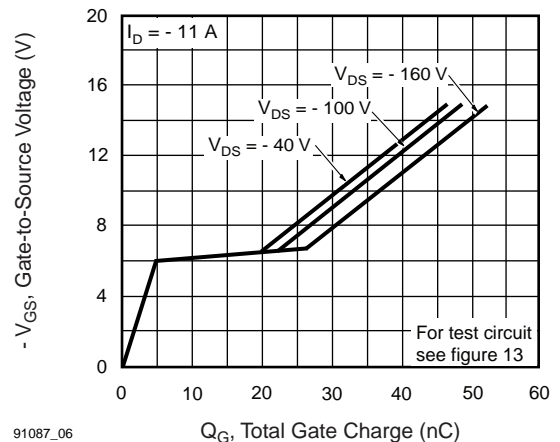
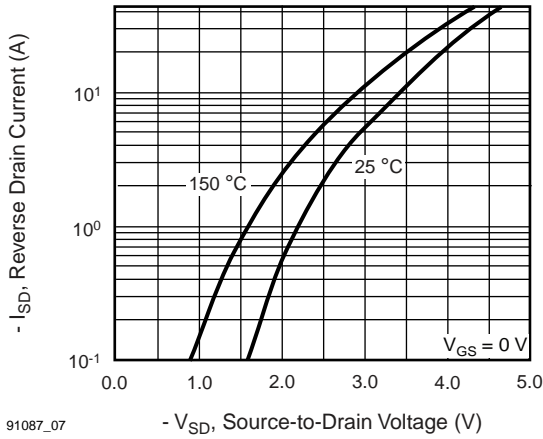
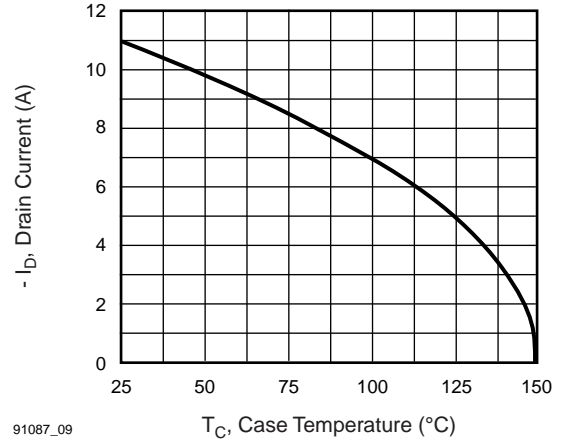


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



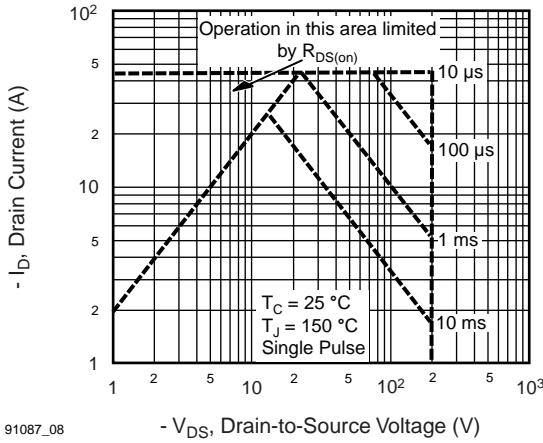
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

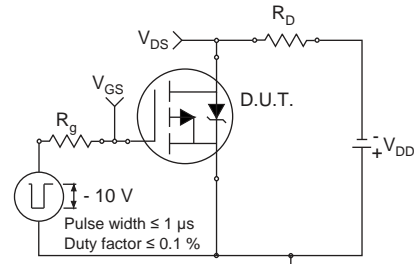


Fig. 10a - Switching Time Test Circuit

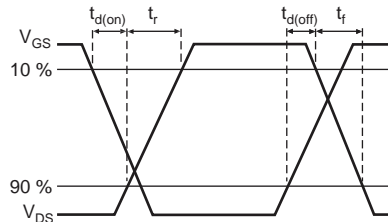
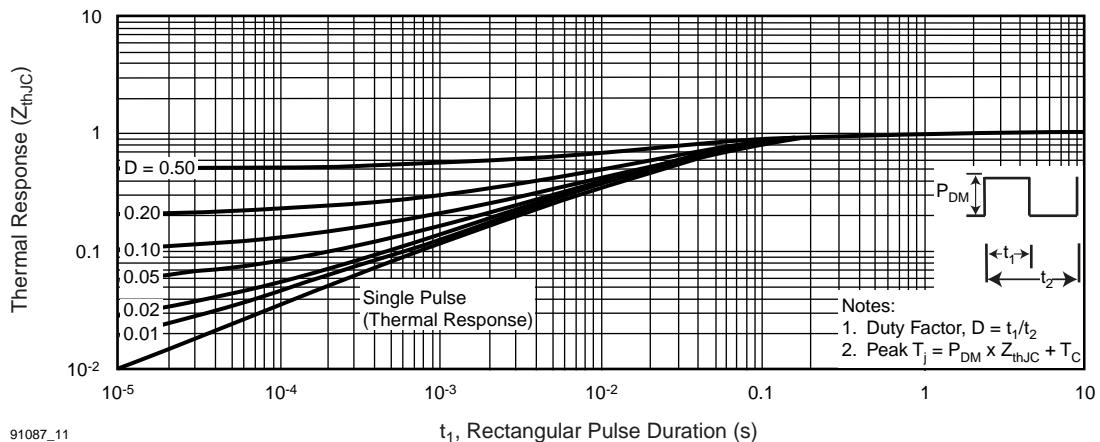


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

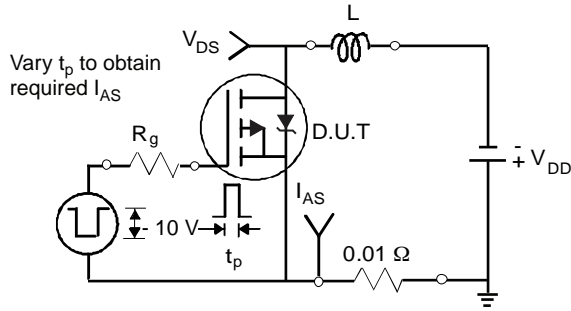


Fig. 12a - Unclamped Inductive Test Circuit

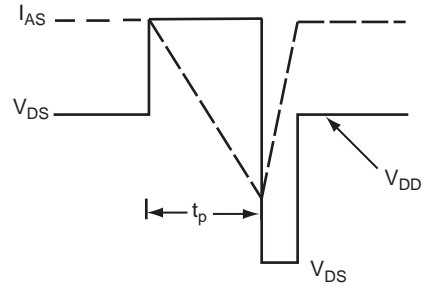


Fig. 12b - Unclamped Inductive Waveforms

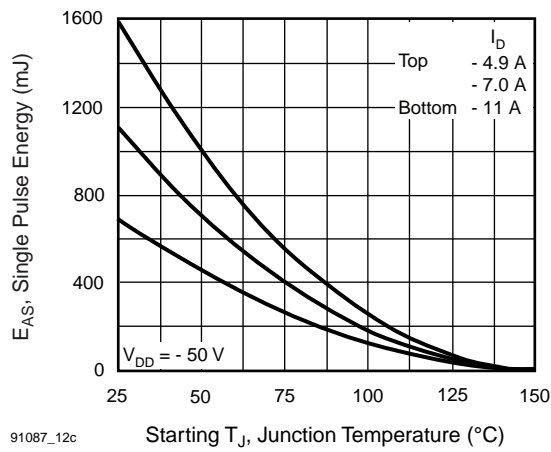


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

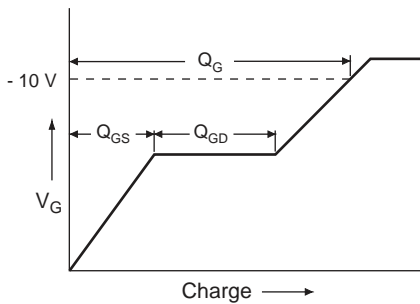


Fig. 13a - Basic Gate Charge Waveform

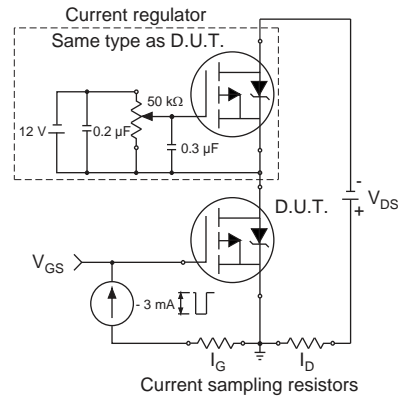


Fig. 13b - Gate Charge Test Circuit

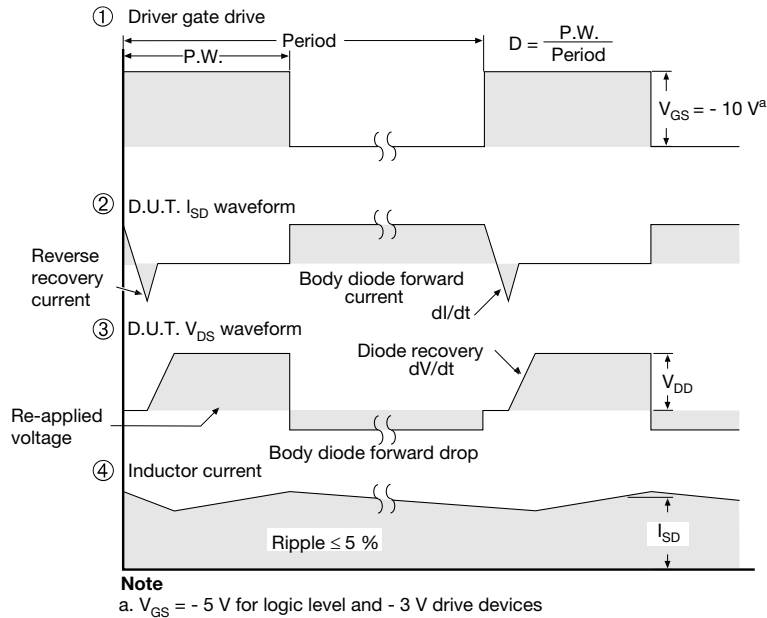
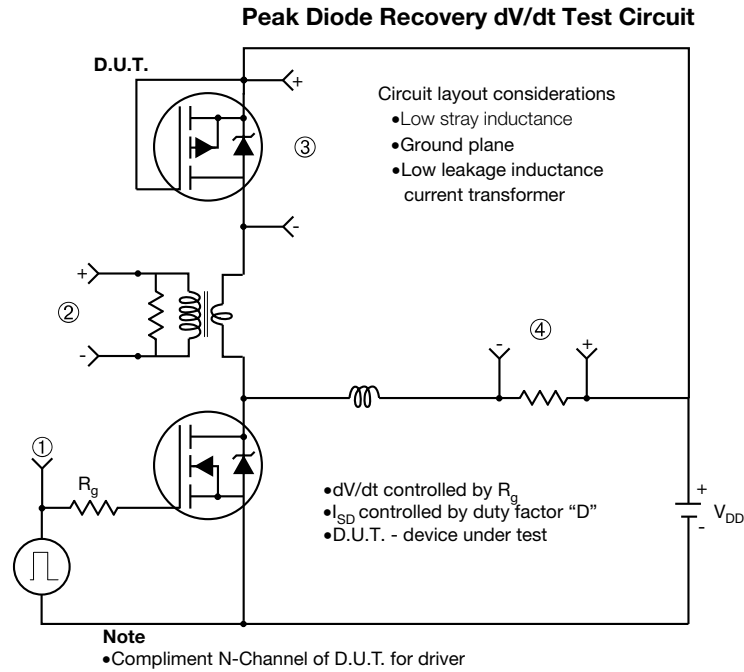
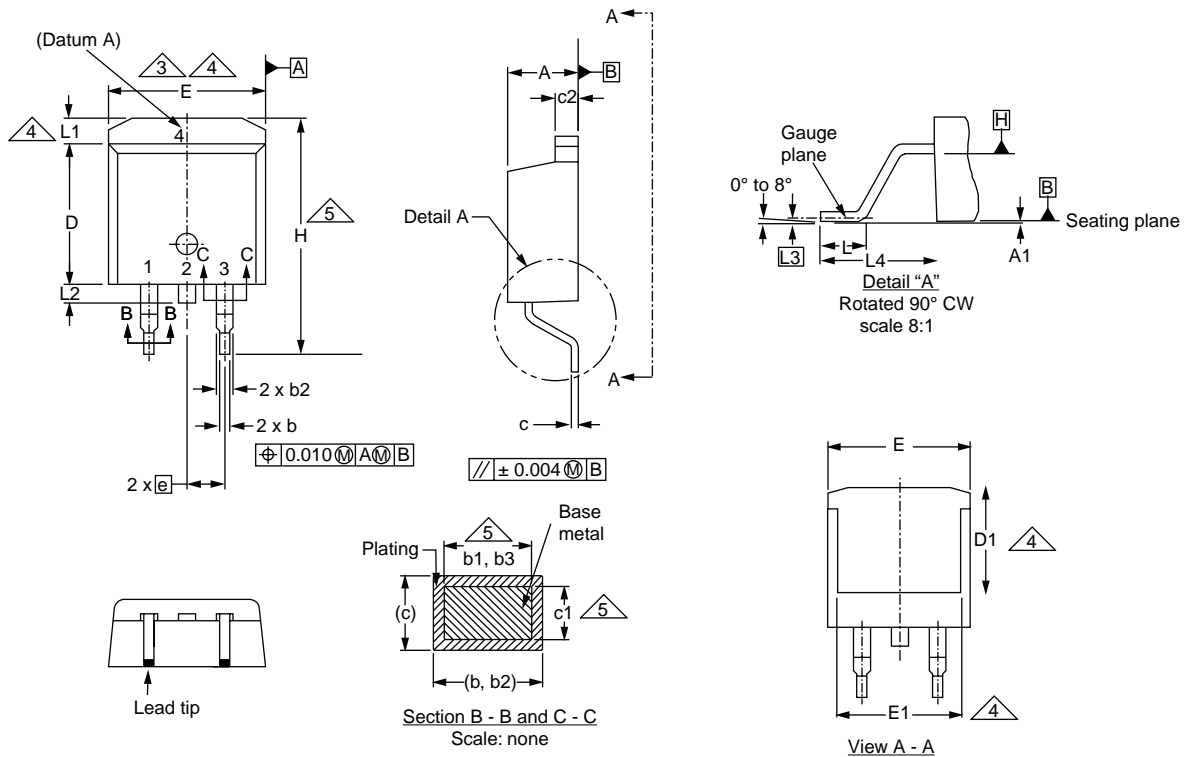


Fig. 14 - For P-Channel

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TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

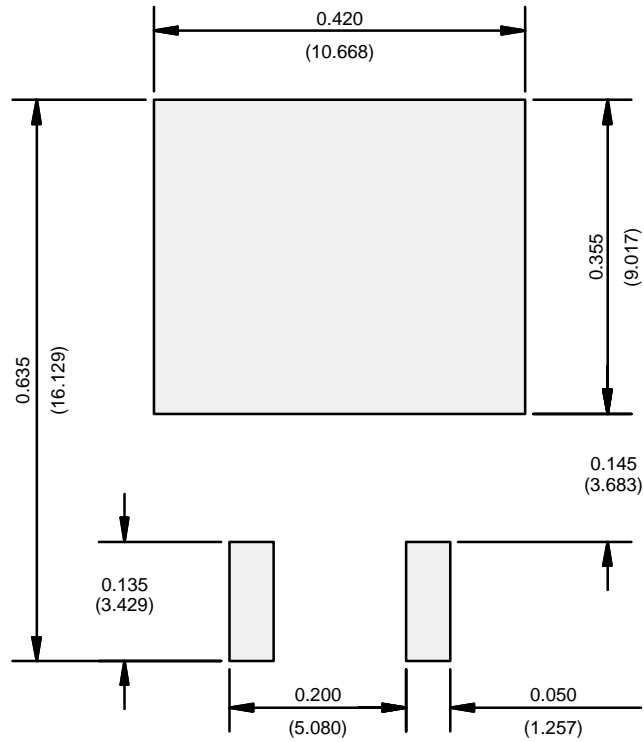
| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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