IH6108

JAN QUALIFIED

High Reliability 8-Channel CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH6108 is a CMOS one of 8 multiplexer. The part is a plug-in replacement for the DG508. Three line decoding is used so that the 8 channels can be controlled by 3 Address inputs; additionally a fourth input is provided for use as a system enable. When the ENable input is high (5V), a channel is selected by the three Address inputs, and when low (0V) all channels are off. The 3 Address inputs are TTL and CMOS logic compatible, with a "1" corresponding to any voltage greater than 2.4V.

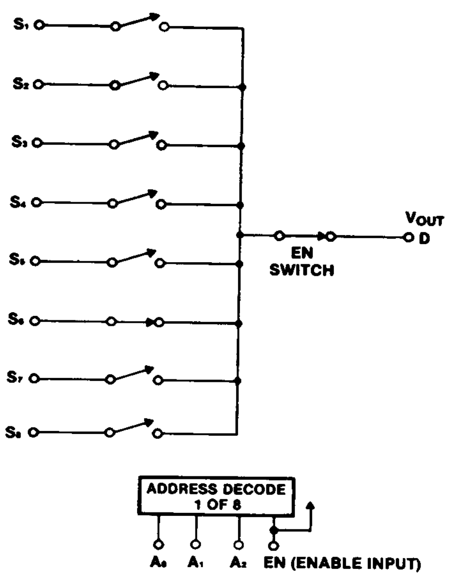
ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6108MJE	−55°C to +125°C	16 pin CERDIP

Ceramic package available as special order only (IH6108MDE)

FEATURES

- **Ultra Low Leakage — $I_{D(off)} \leq 100pA$ Typical**
- **$r_{DS(on)} < 400$ Ohms Over Full Signal and Temperature Range**
- **Power Supply Quiescent Current Less Than 100μA**
- **±14V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **Binary Address Control (3 Address Inputs Control 8 Channels)**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With DG508, HI-508 & AD7508**
- **Internal Diode In Series With V+ for Fault Protection**
- **JAN 38510 Approved**



3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

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Figure 1: Functional Diagram

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	On Switch
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2
Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
Logic "0" = $V_{AL} \leq 0.8V$

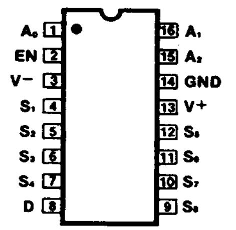

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Figure 2: Pin Configuration

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ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground .... −15V to 15V
V_S or V_D to V+ .... 0, −36V
V_S or V_D to V− 0, 36V
V+ to Ground 16V
V− to Ground .... −16V
Current (Any Terminal) 30mA

Current (Analog Source or Drain) 20mA
Operating Temperature .... −55 to 125°C
Storage Temperature .... −65 to 150°C
Lead Temp (Soldering, 10sec) .... 300°C
Power Dissipation (Package)* 1200mW

* All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

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NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions		Max Limits M Suffix −55°C	Max Limits M Suffix 25°C	Max Limits M Suffix 125°C	Units
SWITCH									
$r_{DS(ON)}$	S to D	8	150	$V_D = -10V$, $I_S = -1.0mA$	Sequence each switch on	300	300	400	Ω
		8	150	$V_D = -10V$, $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	300	300	400	
$\Delta r_{DS(ON)}$			20	$\Delta R_{DS(on)} = \frac{\Delta r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$					%
$I_{S(OFF)}$	S	8	0.002	$V_S = 10V$, $V_D = -10V$			±.5	50	nA
		8	0.002	$V_S = -10V$, $V_D = 10V$	$V_{EN} = 0.8V$		±.5	50	
$I_{D(OFF)}$	D	1	0.03	$V_D = 10V$, $V_S = -10V$			±2	100	
		1	0.03	$V_D = -10V$, $V_S = 10V$			±2	100	
$I_{D(ON)}$	D	8	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on		±2	100	
		8	0.1	$V_{S(ALL)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$		±2	100	
INPUT									
$I_{AN(ON)}$ or $I_{A(on)}$	A_0, A_1 or A_2 Inputs	3	0.01	$V_A = 2.4V$ or 0V			−10	−30	μA
$I_{AN(OFF)}$ $I_{A(off)}$		3	0.01	$V_A = 14V$ or 0V			10	30	
I_A	A_0, A_1, A_2	3		$V_{EN} = 5V$	All $V_A = 0$ (Address pins)		−10	−30	
	EN	1		$V_{EN} = 0$			−10	−30	
DYNAMIC									
$t_{transition}$	D		0.3	See Fig. 1			1		μs
t_{open}	D		0.2	See Fig. 2					
$t_{on(EN)}$	D		0.6	See Fig. 3			1.5		
$t_{off(EN)}$	D		0.4				1		
"OFF" Isolation	D		60	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, f = 500kHz					dB
$C_{s(off)}$	S		5	$V_S = 0$	$V_{EN} = 0V$, f = 140kHz to 1MHz				pF
$C_{d(off)}$	D		25	$V_D = 0$					
$C_{DS(off)}$	D to S		1	$V_S = 0$, $V_D = 0$					
SUPPLY									
Supply Current +	V+	1	40	$V_{EN} = 5V$	All $V_A = 0$ or 5V		200		μA
Supply Current −	V−	1	2				100		
Standby Current +	V+	1	1	$V_{EN} = 0$			100		
Standby Current −	V−	1	1				100		

NOTE 1: See Enable Input Strobing Levels, in Application Section.

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SWITCHING INFORMATION

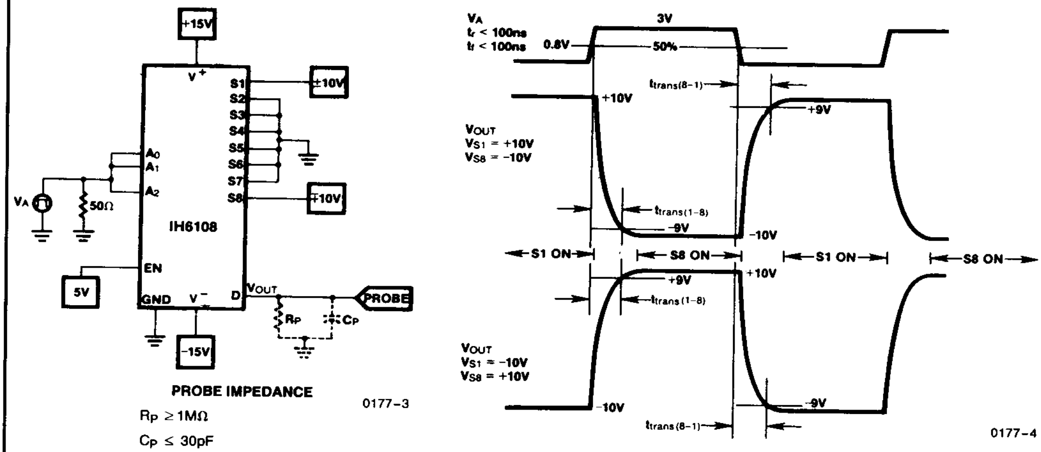

Figure 3: $t_{transition}$ Switching Test

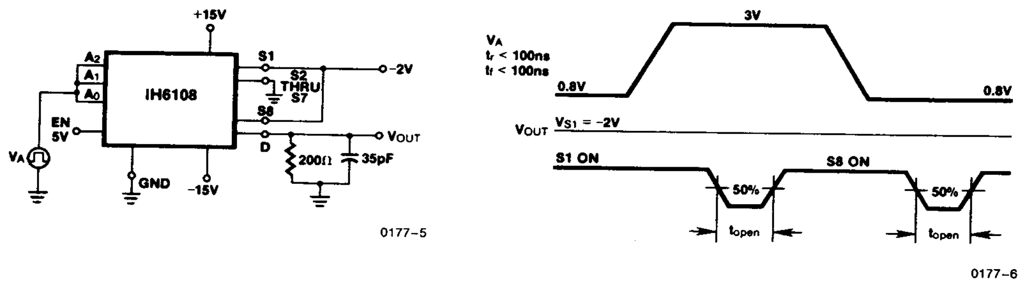

Figure 4: t_{open} (Break-Before-Make) Switching Test

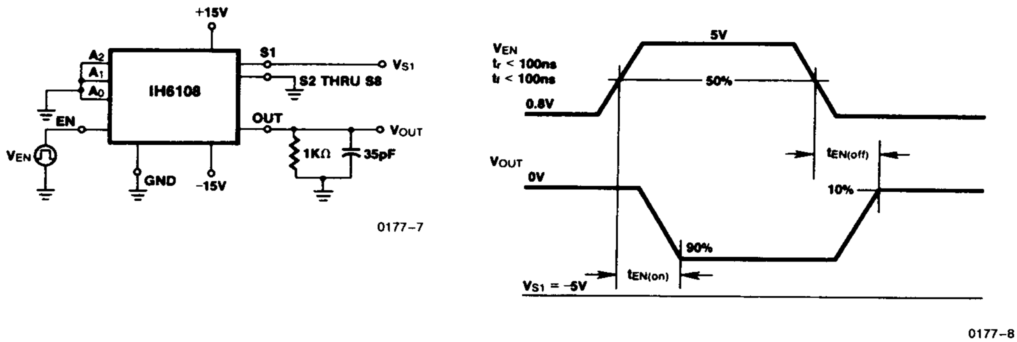

Figure 5: t_{on} and t_{off} Switching Test

IH6108 APPLICATION INFORMATION

ENable Input Strobing Levels

The ENable input on the IH6108 requires a minimum of +4.5V to trigger to the "1" state and a maximum of +0.8V to trigger to the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 6)

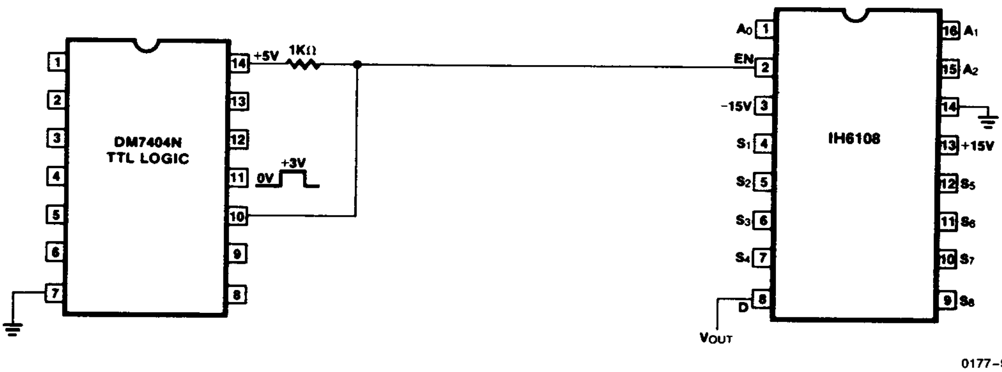

Figure 6: ENable Input Strobing from TTL Logic

When the EN input is driven from CMOS logic, no pullup is necessary, see Fig. 7.

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IH6108 APPLICATION INFORMATION (Continued)

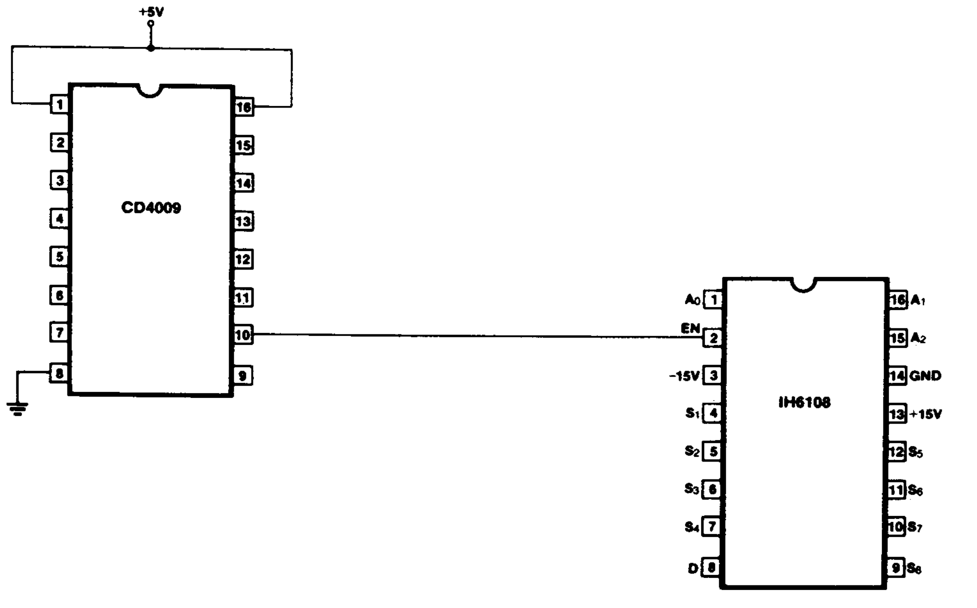

Figure 7: ENable Input Driven from CMOS Logic

The supply voltage of the CD4009 affects the switching speed of the IH6108; the same is true for TTL supply voltage levels. The following chart shows the effect, on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS or TTL Supply Voltage	Typical t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 6 and 7 deal with ENable strobing when expansion to more than eight channels is required. In these cases the EN terminal acts as a fourth address input. If eight channels or less are being multiplexed, the EN terminal can be directly connected to +5V logic supply to enable the IH6108 at all times.

Using the IH6108 with supplies other than ±15V

The IH6108 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however, the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done, the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 13) via a silicon diode as shown in Figure 8. When using this type of configuration, a further requirement must be met: the strobe levels of A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 8 the EN voltage is 11.3V which means that logic high at A0 and A1 is= +8.8V (logic low continues to be=0.8V). In this configuration the IH6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6108 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN, (See Figure 9). A 1μF capacitor can be placed across the diode to minimize switching glitches.

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IH6108 APPLICATION INFORMATION (Continued)

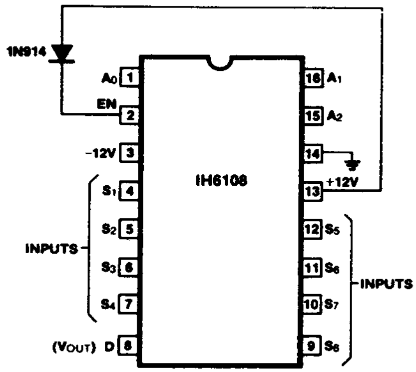

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Figure 8: IH6108 Connection Diagram for less than ± 15V Supply Operation

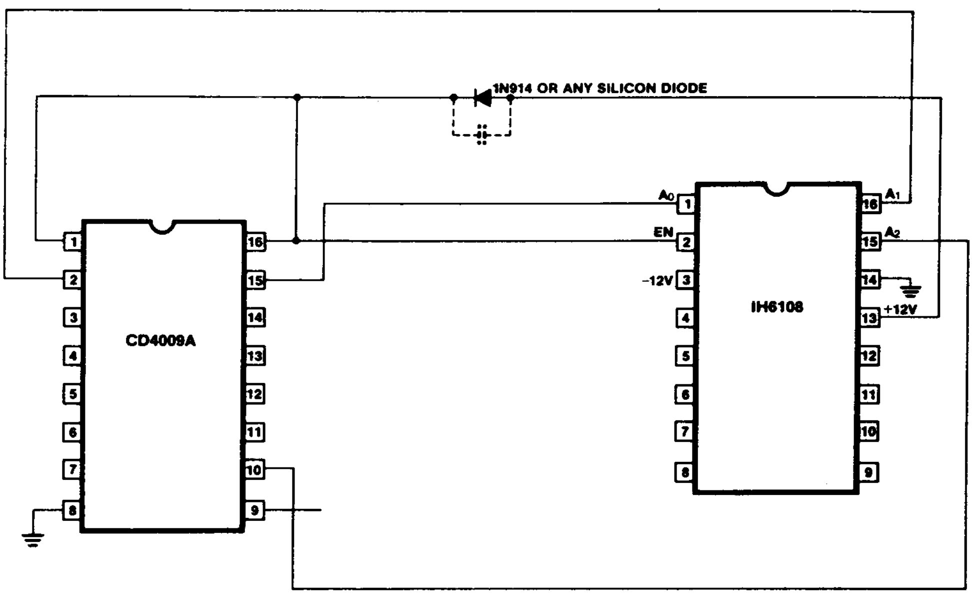

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Figure 9: IH6108 Connection Diagram with ENable Input Strobing for less than ± 15V Supply Operation

Peak-to-Peak Signal Handling Capability

The IH6108 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6108 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.