Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (4K x 16-BIT) LATCHED CacheRAM™

IDT71586

FEATURES:

- Wide 4K x 16 Organization
- High-speed access
  - — Commercial: 25/35/45ns (max.)
  - — Military: 35/45/55ns (max.)
- Internal fast 12-bit address latch (5ns set-up and hold times)
- Best fit for popular cache configurations:
  - — Intel 82385 cache controller (for 80386)
  - — IDT79R3000 RISC CPU instruction & data caches
  - — Chips & Technologies 82C307 cache controller (for 80386)
- Fast Output Enable — 10ns (max.)
- Separate enables for upper and lower bytes
- Packaged in 40-pin, 600 mil ceramic or plastic DIP, or 44-pin PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71586 is a fast 4K x 16 latched address CeMOS static RAM designed to enhance cache memory designs. This device offers improved circuit board densities over designs using traditional RAM architectures in caches for the Intel 80386/82385, the Chips & Technologies 82C307, and the IDT79R3000 RISC CPU.

The IDT71586 boasts a fast address access time down to 24ns (max.), a very fast 10ns (max.) Output Enable pin, and short set-up and hold times (5ns max.) on the address input latch. All of these features help the IDT71586 to make the most efficient use of CPU-local buses.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT71586 achieves this high throughput at a typical operating power of only 300mW.

All inputs and outputs of the IDT71586 are TTL-compatible, and the device operates from a standard 5V supply, simplifying system design. The IDT71586 is offered in a 40 pin ceramic or plastic DIP or a 44 pin plastic leadless chip carrier, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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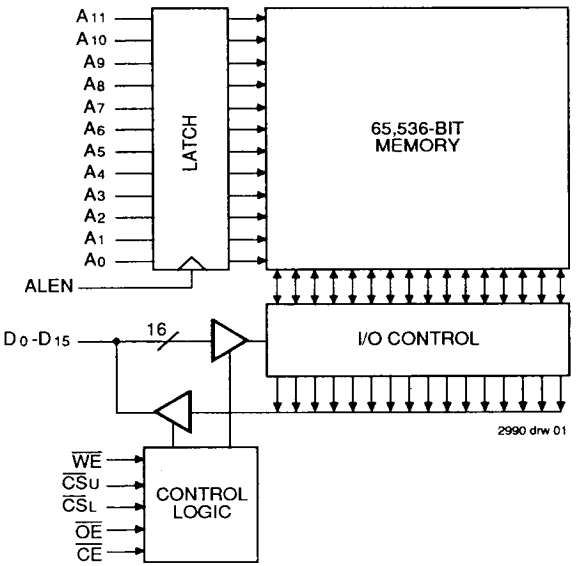
FUNCTIONAL BLOCK DIAGRAM



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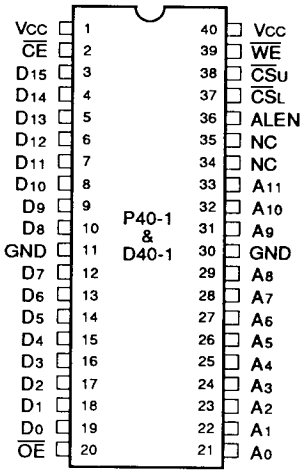
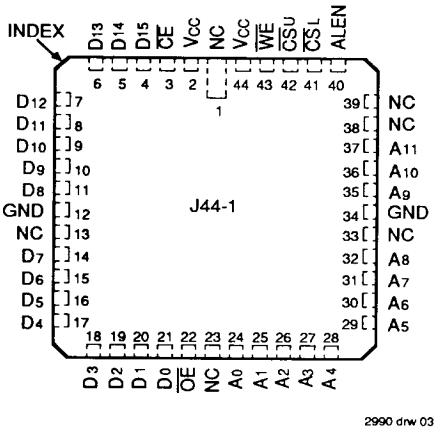
PIN CONFIGURATIONS



2990 drw 02

DIP
TOP VIEW



2990 drw 03

PLCC
TOP VIEW

TRUTH TABLE(1)

Inputs						Outputs		
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{CS_U}$	$\overline{CS_L}$	ALEN	D8–D15	D0–D7	Mode
H	X	X	X	X	—	Hi-Z	Hi-Z	Deselected, powered-down (I_{SB})
X	X	X	H	H	—	Hi-Z	Hi-Z	Deselected.
—	—	H	—	—	—	Hi-Z	Hi-Z	Outputs disabled
—	—	—	—	—	H	—	—	Address latch transparent
X	X	—	—	—	L	—	—	Address latch closed
L	L	X	L	H	H	$DATA_{IN}$	Hi-Z	Write to upper byte of current address
L	L	X	L	H	L	$DATA_{IN}$	Hi-Z	Write to upper byte of latched address
L	L	X	H	L	H	Hi-Z	$DATA_{IN}$	Write to lower byte of current address
L	L	X	H	L	L	Hi-Z	$DATA_{IN}$	Write to lower byte of latched address
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to both bytes of current address (Word Write)
L	L	X	L	L	L	$DATA_{IN}$	$DATA_{IN}$	Write to both bytes of latched address (Word Write)
L	H	L	L	H	H	$DATA_{OUT}$	Hi-Z	Read upper byte of current address
L	H	L	L	H	L	$DATA_{OUT}$	Hi-Z	Read upper byte of latched address
L	H	L	H	L	H	Hi-Z	$DATA_{OUT}$	Read lower byte of current address
L	H	L	H	L	L	Hi-Z	$DATA_{OUT}$	Read lower byte of latched address
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read both bytes of current address (Word Read)
L	H	L	L	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Read both bytes of latched address (Word Read)

NOTE:
1. H = HIGH
   L = LOW
   X = Don't Care
   — = Unrelated
   Hi-Z = High Impedance

2990 tbl 01

PIN DESCRIPTIONS

A_{0-11}	Address Inputs
D_{0-15}	Data Input/Output
$\overline{CE}$	Chip Enable/Power Down
$\overline{CS_U}$	Upper Byte Select
$\overline{CS_L}$	Lower Byte Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
ALEN	Address Latch Enable
GND	Ground
V_{CC}	Power

2990 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation Plastic Hermetic	1.5 2.0	W W
I_{OUT}	DC Output Current	50	mA

NOTE: 2990 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	12	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2990 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2990 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2990 tbl 06

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

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SPEED SELECTION

IDT79R3000 SPEED	80386 SPEED	SUGGESTED IDT71586
—	16MHZ	71586S55
12MHz	20MHz	71586S45
16MHz	25MHz	71586S35
20-25MHz	33MHz	71586S25

2990 tbl 12

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage (D_0–D_{15})	I_{OL} = 6mA, V_{CC} = Min.	—	0.4	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.5	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.	2.4	—	V

2990 tbl 07

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71586S25		71586S35		71586S45		71586S55		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Operating Power Supply Current $\overline{CE}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(2)	130	—	130	150	130	150	—	150	mA
I_{CC2}	Dynamic Operating Current $\overline{CE}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	240	—	240	290	240	290	—	290	mA
I_{SB}	Standby Power Supply Current (TTL Level Inputs) $\overline{CE}$ ≥ V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	70	—	70	70	70	70	—	70	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level Inputs) $\overline{CE}$≥V_{HC}, V_{IN}≤V_{LC} or V_{IN}≥V_{HC}, V_{CC}= Max., f = 0(2)	15	—	15	20	15	20	—	20	mA

2990 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2990 tbl 09

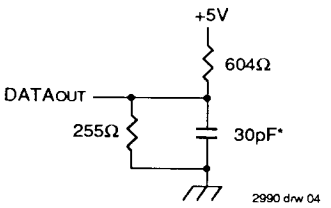

Figure 1. Output Load

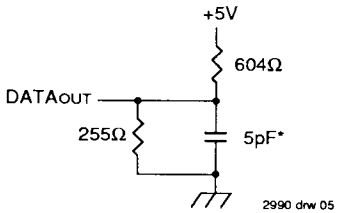

Figure 2. Output Load
(for t_{OHZ}, t_{BHZ}, t_{CHZ}, t_{OLZ}, t_{BLZ}, t_{CLZ}, t_{WHZ}, and t_{OW})

*Includes scope and jig.

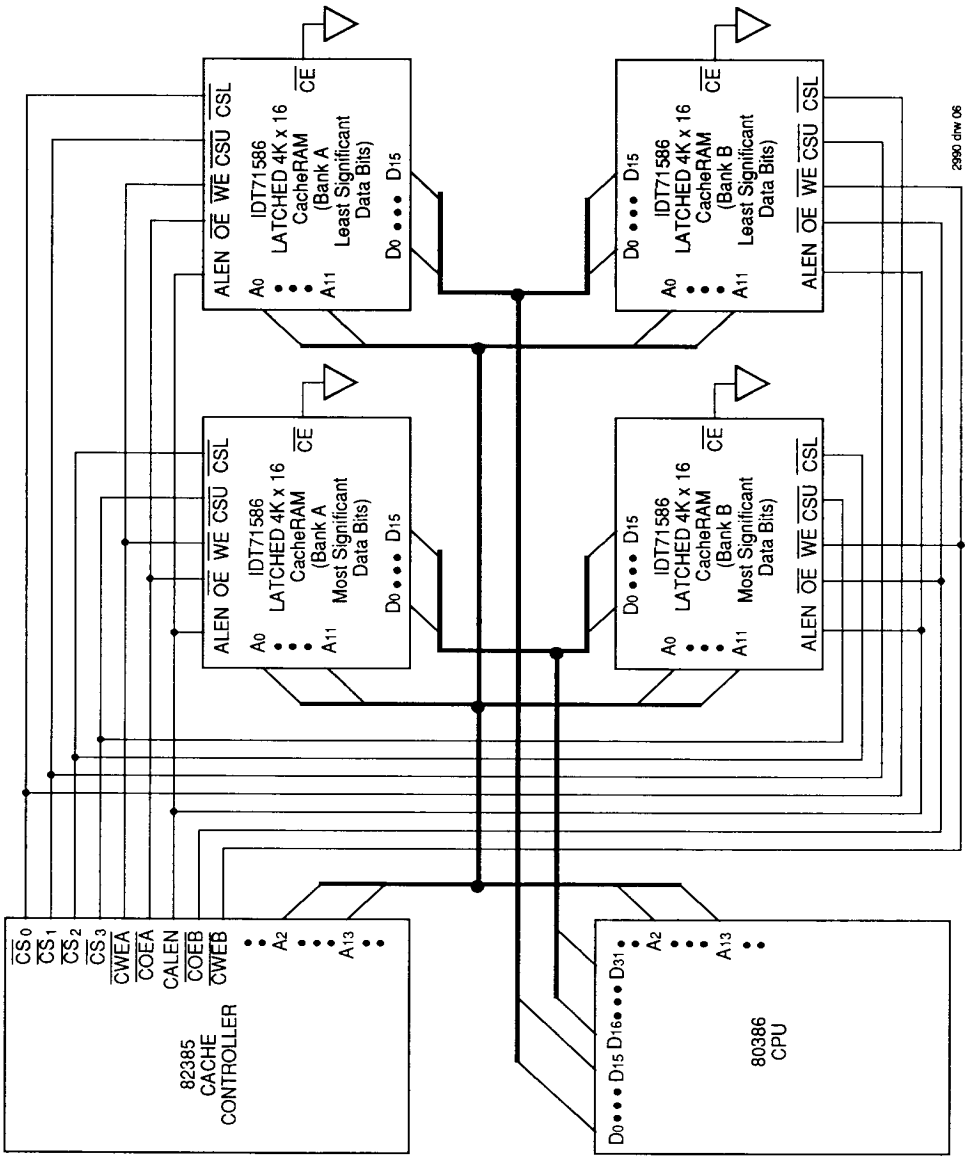

Figure 3. Example Cache for Intel 80386 using IDT71586 Latched CacheRAM and Intel 82385

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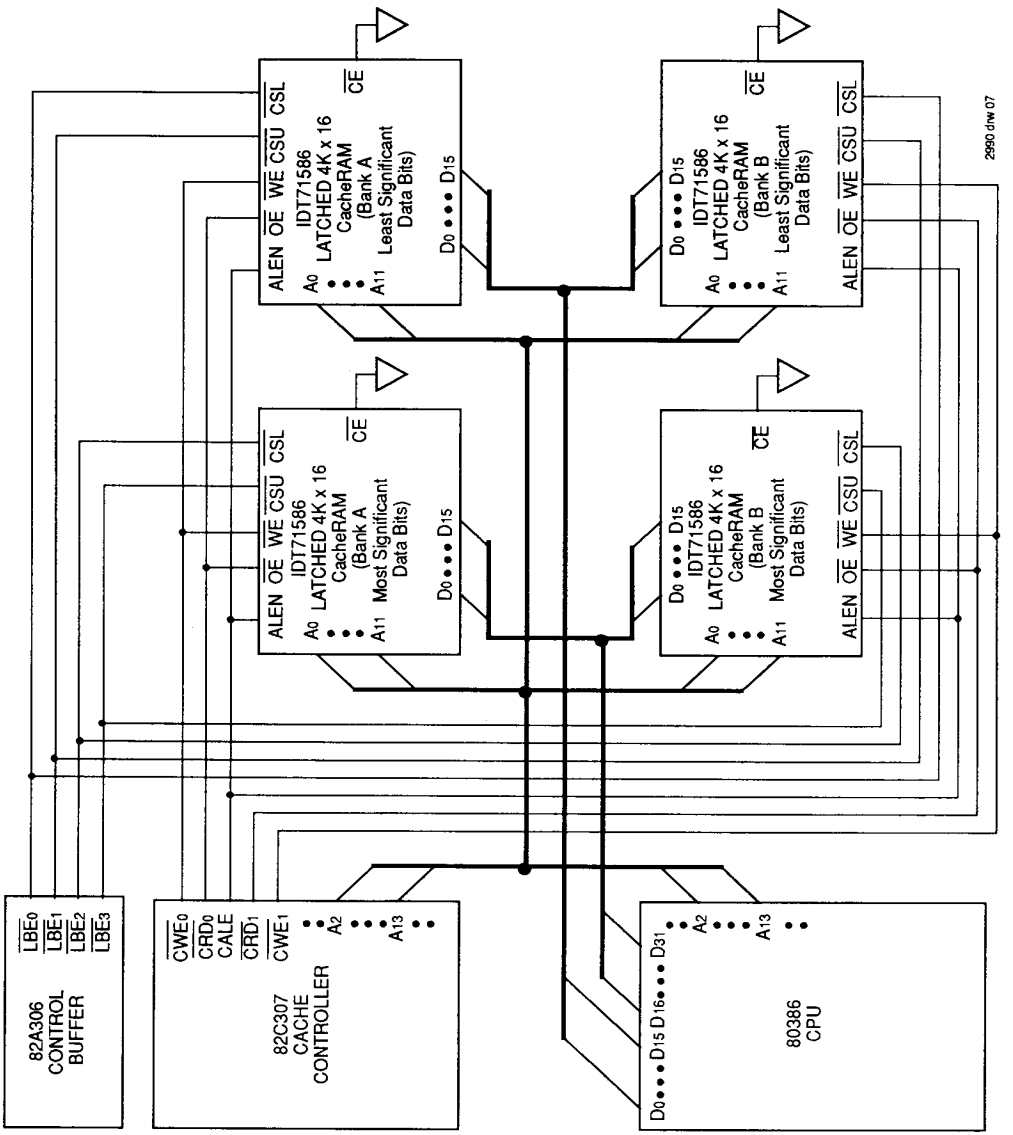

Figure 4. Example Cache for Intel 80386 using IDT71586 Latched CacheRAM and Chips & Technologies 82C307

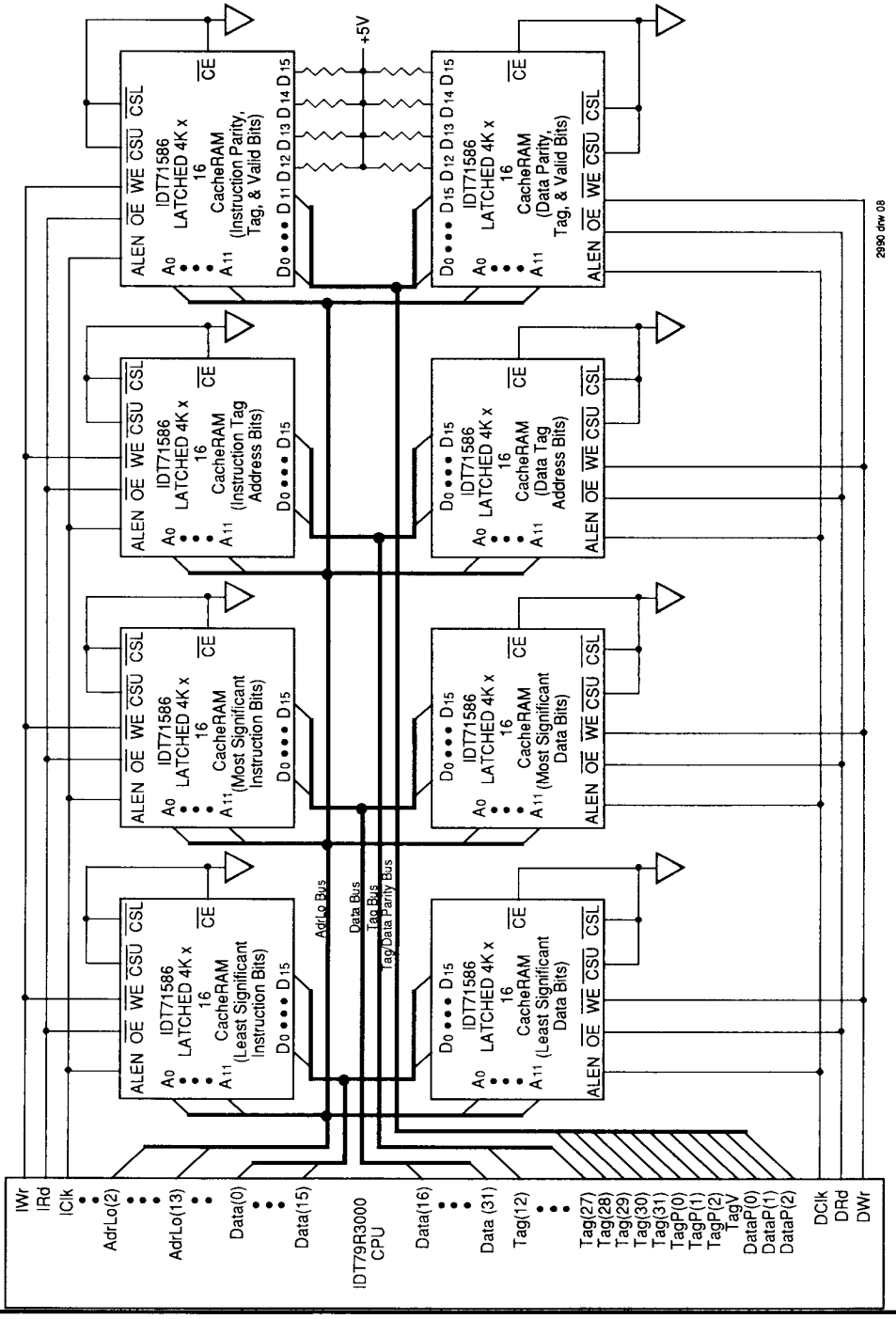

Figure 5. Example Instruction and Data Caches for IDT79R3000 using IDT71586 Latched Cache Ram

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71586S25[1]		71586S35		71586S45		71586S55[5]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	ns
tCH	ALEN High Time[3]	10	—	10	—	12	—	15	—	ns
tCL	ALEN Low Time[3]	10	—	10	—	12	—	15	—	ns
tAS	Address Latch Set-Up Time	5	—	5	—	5	—	5	—	ns
tAH	Address Latch Hold Time	4	—	5	—	5	—	5	—	ns
tAA	Address Access Time[4]	—	24	—	35	—	45	—	55	ns
tACE	Chip Enable Access Time[4]	—	25	—	35	—	45	—	55	ns
tAB	Upper/Lower Byte Chip Select Access Time	—	13	—	15	—	20	—	25	ns
tOE	Output Enable to Output Valid	—	10	—	13	—	15	—	18	ns
tCLZ	Chip Enable to Output in Low $Z^{(2,3)}$	3	—	3	—	3	—	3	—	ns
tBLZ	Upper/Lower Byte Chip Select to Output in Low $Z^{(2,3)}$	3	—	3	—	3	—	3	—	ns
tOLZ	Output Enable to Output in Low $Z^{(2,3)}$	2	—	2	—	2	—	2	—	ns
tCHZ	Chip Disable to Output in High $Z^{(2,3)}$	—	20	—	25	—	30	—	35	ns
tBHZ	Upper/Lower Byte Chip Select to Output in High $Z^{(2,3)}$	—	20	—	25	—	30	—	35	ns
tOHZ	Output Disable to Output in High $Z^{(2,3)}$	—	4	—	9	—	13	—	15	ns
tOH	Output Hold from Address Change[4]	3	—	3	—	3	—	3	—	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	ns
tPD	Chip Select to Power Down Time[3]	—	25	—	35	—	45	—	55	ns

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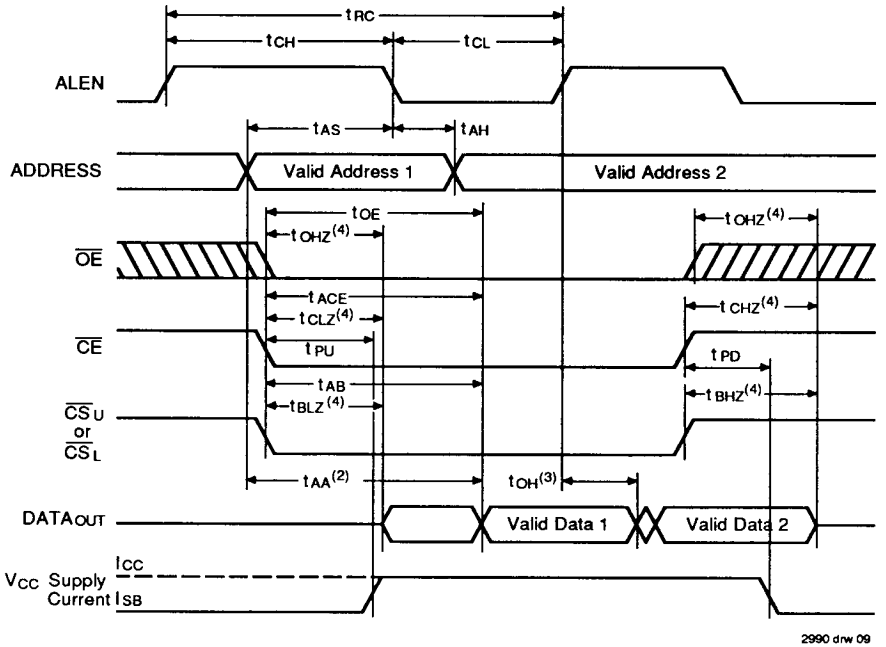
NOTES:
1. 0° to +70°C temperature range only.
2. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1&2).
3. This parameter is guaranteed, but not tested..
4. This measurement depends on the combination of ALEN high plus an address change. This combination may either happen at the rising edge of ALEN, or during an address change after ALEN has become high.
5. -55°C to +125°C temperature range only.

TIMING WAVEFORM OF READ CYCLE(1)



NOTES:
1. $\overline{WE}$ is high throughout a read cycle.
2. The parameter t_{AA} is measured either from the first low to high transition of ALEN after the read address has become valid, or from the stabilization of the read address during the period when ALEN is high, whichever occurs last.
3. The parameter t_{OH} is measured either from the first low to high transition of ALEN after an address change, or from an address change during the period when ALEN is high, whichever occurs first.
4. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

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AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71586S25[1]		71586S35		71586S45		71586S55[4]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tWC	Write Cycle Time	25	—	35	—	45	—	55	—	ns
tCH	ALEN High Time	10	—	10	—	12	—	15	—	ns
tCL	ALEN Low Time	10	—	10	—	12	—	15	—	ns
tAS	Address Latch Set-up Time	5	—	5	—	5	—	5	—	ns
tAH	Address Latch Hold Time	4	—	5	—	5	—	5	—	ns
tAW	Address Valid to End of Write[3]	25	—	35	—	45	—	55	—	ns
tASW	Address Set-Up Time[3]	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	17	—	25	—	30	—	40	—	ns
tCW	Chip Enable to End of Write	20	—	25	—	30	—	40	—	ns
tBW	Upper/Lower Byte Chip Select to End of Write	20	—	25	—	30	—	40	—	ns
tWR	Write Recovery Time[3]	0	—	0	—	0	—	0	—	ns
tWHZ	Write to Output in High Z[2]	—	13	—	15	—	20	—	25	ns
tDW	Data Set-Up Time	11	—	13	—	15	—	18	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write[2]	5	—	5	—	5	—	5	—	ns

NOTES:

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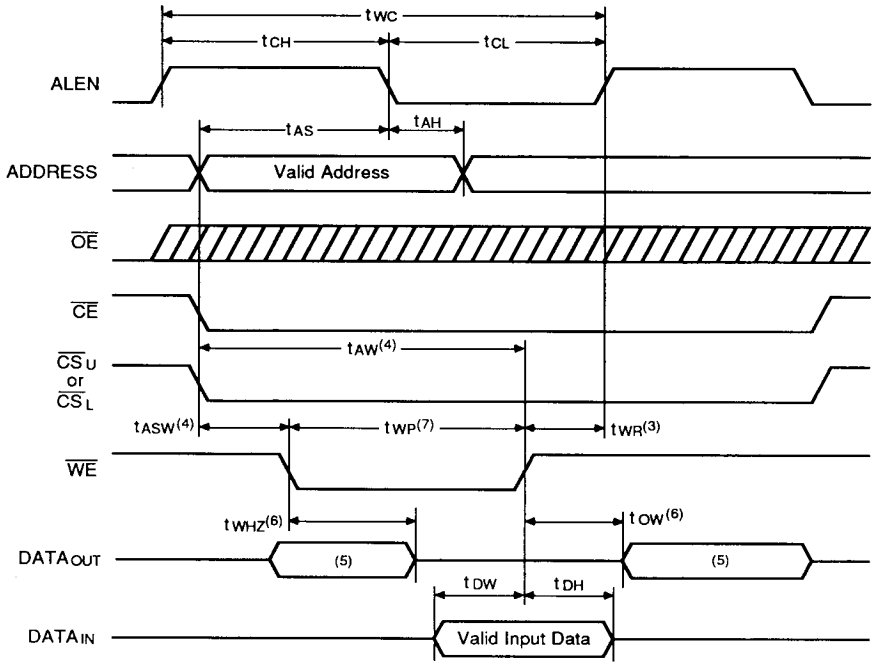
1. 0° to +70°C temperature range only.
2. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1&2). This parameter is guaranteed, but not tested.
3. This measurement depends on the combination of ALEN high plus an address change. This combination may either happen at the rising edge of ALEN, or during an address change after ALEN has become high.
4. -55°C to +125°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2)



NOTES:
1. $\overline{WE}$, $\overline{CE}$ or both $\overline{CS}_U$ and $\overline{CS}_L$ must be inactive during all address transitions.
2. A write occurs during the overlap (tBW, tCW or tWP) of a low $\overline{CS}_U$ or $\overline{CS}_L$, a low $\overline{CE}$ and a low $\overline{WE}$.
3. The parameter tWR is measured from the earlier of $\overline{CS}_U$, $\overline{CS}_L$, $\overline{CE}$, or $\overline{WE}$ going high either to the first low to high transition of ALEN after an address change, or to an address change during the period when ALEN is high, whichever occurs first.
4. The parameters tASW and tAW are measured either from the first low to high transition of ALEN after the write address has become valid, or from the stabilization of the valid write address during the period when ALEN is high, whichever occurs first.
5. During this period, I/O pins are in the output state, and xinput signals must not be applied.
6. This transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ +tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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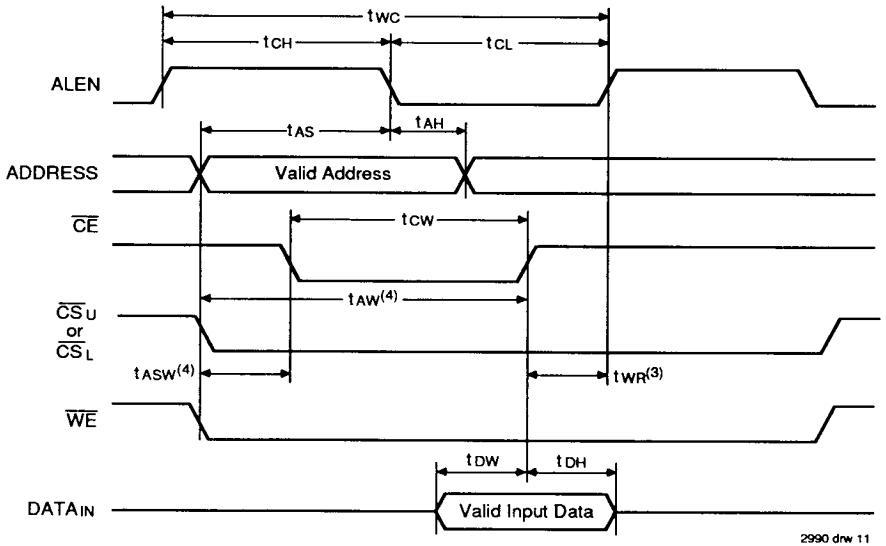
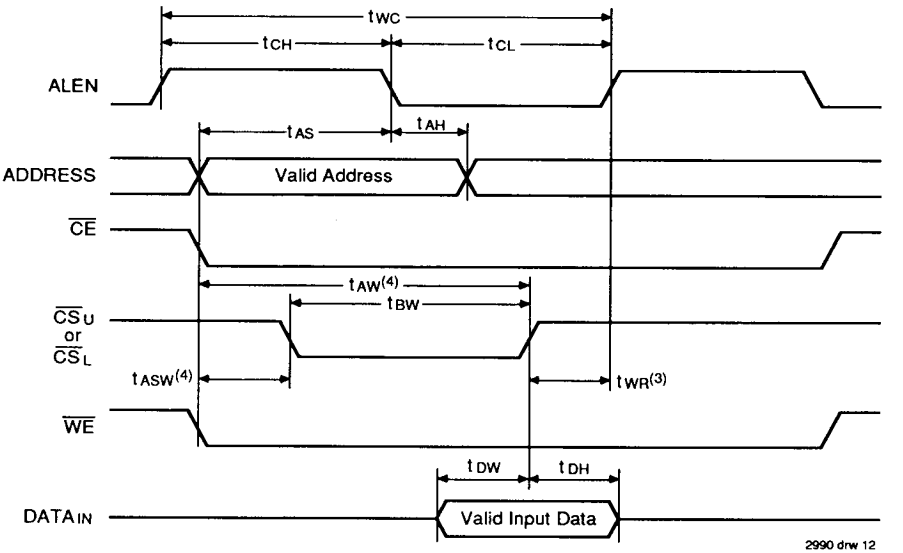
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING)(1, 2)

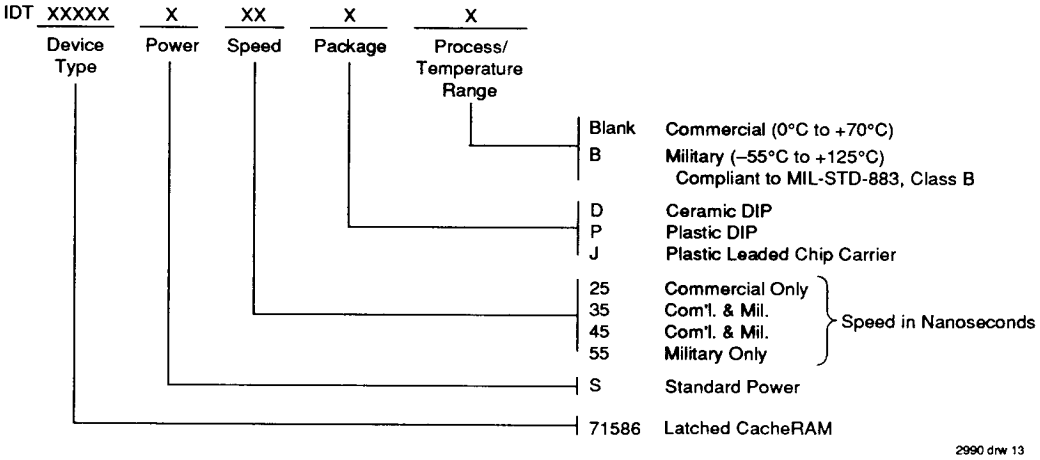


TIMING WAVEFORM OF WRITE CYCLE NO.3 ($\overline{CS}_U$ or $\overline{CS}_L$ CONTROLLED TIMING)(1, 2)



NOTES:
1. $\overline{WE}$, $\overline{CE}$ or both $\overline{CS}_U$ and $\overline{CS}_L$ must be high during all address transitions.
2. A write occurs during the overlap (tBW, tCW or tWP) of a low $\overline{CS}_U$ or $\overline{CS}_L$, a low $\overline{CE}$ and a low $\overline{WE}$.
3. The parameter tWR is measured from the earlier of $\overline{CS}_U$, $\overline{CS}_L$, $\overline{CE}$, or $\overline{WE}$ going high either to the first low to high transition of ALEN after an address change, or to an address change during the period when ALEN is high, whichever occurs first.
4. The parameters tASW and tAW are measured either from the first low to high transition of ALEN after the write address has become valid, or from the stabilization of the valid write address during the period when ALEN is high, whichever occurs first.

ORDERING INFORMATION



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